STP4NM60
STD3NM60, STD3NM60-1

N-channel 600 V, 1.3 Ω, 3 A TO-220, DPAK, IPAK Zener-protected MDmesh™ Power MOSFET

Features

Type	V_{DSS} (@T_{jmax})	$R_{DS(on)}$ max	I_D	P_W
STD3NM60	650	< 1.5 Ω	3 A	42 W
STD3NM60-1				
STP4NM60			4 A	69 W

- High dv/dt and avalanche capabilities
- Improved ESD capability
- Low input capacitance and gate charge
- Low gate input resistance
- Tight process control and high manufacturing yields

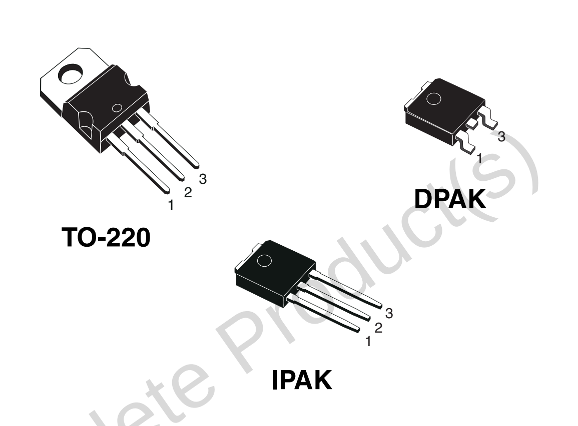
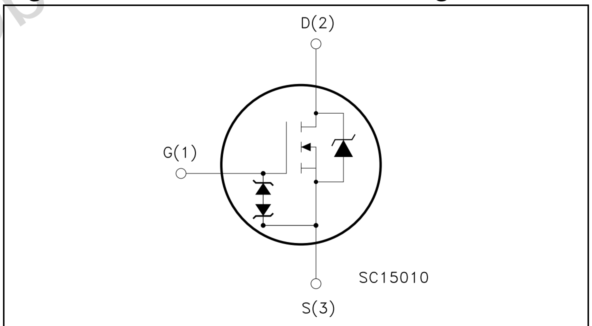


Figure 1. Internal schematic diagram



Applications

- Switching

Description

Modems technology applies the benefits of the multiple drain process to STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product offers low on-resistance, high dv/dt capability and excellent avalanche characteristics.

Table 1. Device summary

Order code	Marking	Package	Packing
STD3NM60	D3NM60	DPAK	Tape and reel
STD3NM60-1	D3NM60	IPAK	Tube
STP4NM60	P4NM60	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		STP4NM60	STD3NM60 STD3NM60-1	
V_{DS}	Drain-source voltage (V_{GS}= 0)	600		V
V_{GS}	Gate- source Voltage	± 30		V
I_D	Drain current (continuous) at T_C= 25°C	4	3	A
I_D	Drain current (continuous) at T_C= 100°C	2.52	1.9	A
I_{DM} (1)	Drain current (pulsed)	16	12	A
P_{TOT}	Total dissipation at T_C= 25°C	69	42	W
	Derating factor	0.55	0.33	W/°C
dv/dt (2)	Peak diode recovery voltage slope	15		V/ns
T_j	Operating junction temperature	-65 to 150		°C
T_{stg}	Storage temperature			°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 3$ A, di/dt ≤ 400 µA, $V_{DD} \leq V_{(BR)DSS}$, Tj $\leq T_{JMAX}$.

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		To-220	DPAK / IPAK	
Rthj-case	Thermal resistance junction-case max	1.82	3	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5		°C/W
T_l	Maximum lead temperature for soldering purpose	300		°C

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{jmax})	1.5	A
E_{AS}	Single pulse avalanche energy (starting T_j= 25 °C, I_D= I_{AR}, V_{DD}= 50 V)	200	mJ

2 Electrical characteristics

(T_{CASE}= 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} =0	600			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max rating V_{DS} = max rating, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±5	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 1.5 A		1.3	1.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V , I_D = 1.5 A	-	2.7	-	S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	324 132 7.4	-	pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 300 V, I_D = 1.5 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 15*)	-	9 4 16.5 10.5	-	ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 480 V, I_D = 3 A, V_{GS} = 10V (see *Figure 21*)	-	10 3 4.7	14	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		3 12	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 3 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 3 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 25°C (see *Figure 17*)	-	224 1 9		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 3 A, di/dt = 100 A/µs, V_{DD} = 100 V, T_j = 150°C (see *Figure 17*)	-	296 1.4 9.3		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

Table 8. Gate-source Zener diode (1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	I_{gs}=± 1mA (open drain)	30	-	-	V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-220

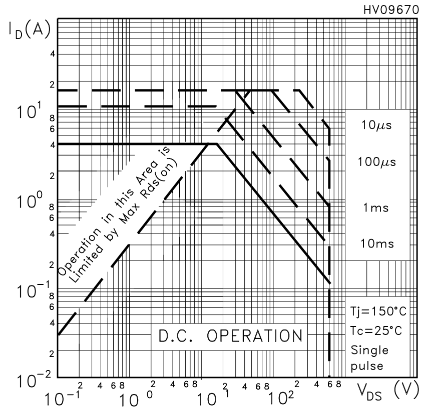


Figure 3. Thermal impedance for TO-220

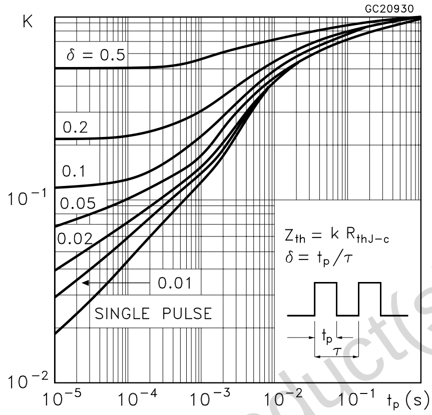


Figure 4. Safe operating area for DPAK and IPAK

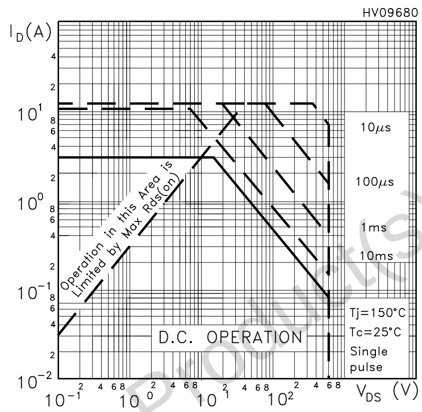


Figure 5. Thermal impedance for DPAK and IPAK

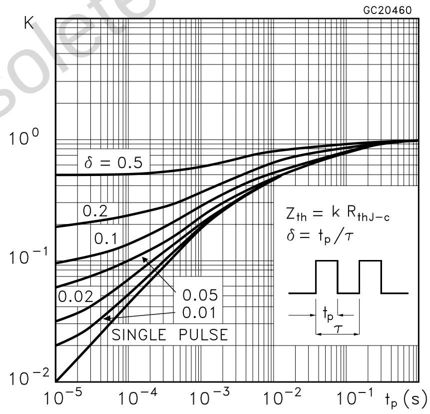


Figure 6. Output characterisics

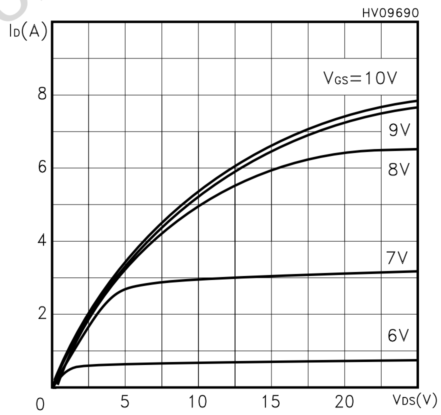


Figure 7. Transfer characteristics

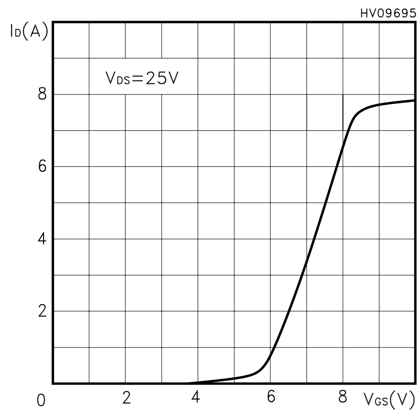


Figure 8. Transconductance

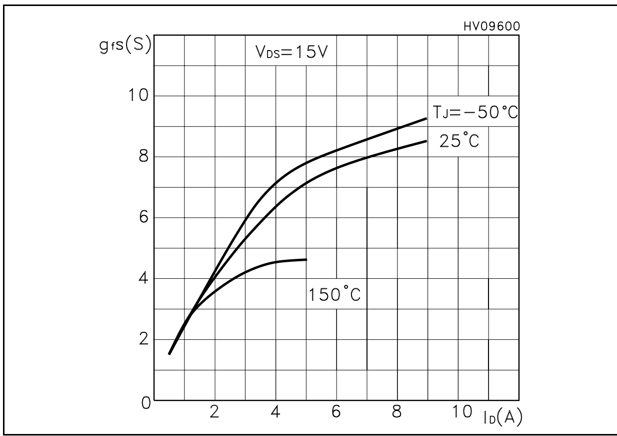


Figure 9. Static drain-source on resistance

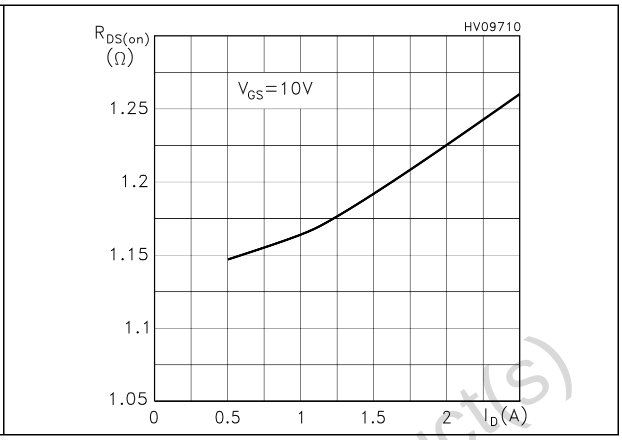


Figure 10. Gate charge vs gate-source voltage

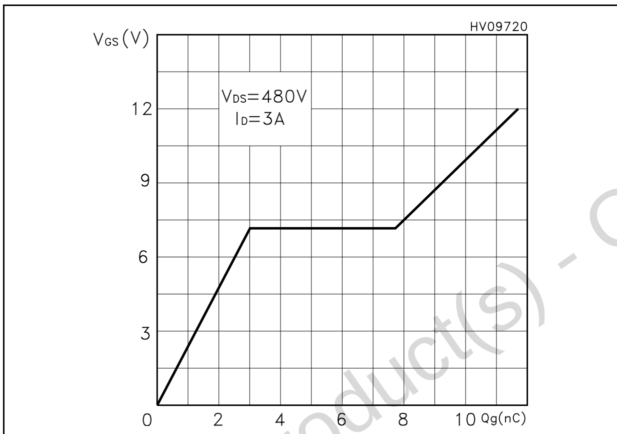


Figure 11. Capacitance variations

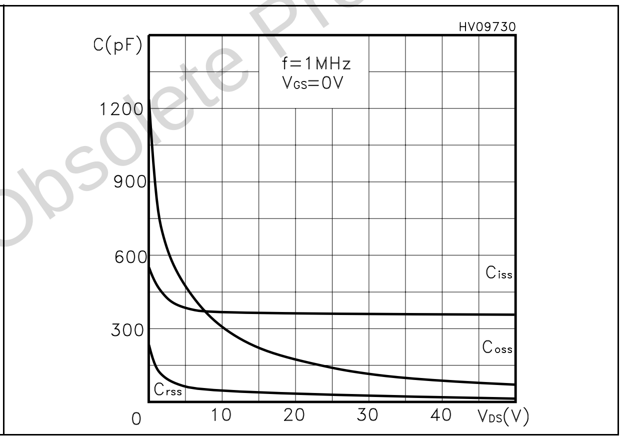


Figure 12. Normalized gate threshold voltage vs temperature

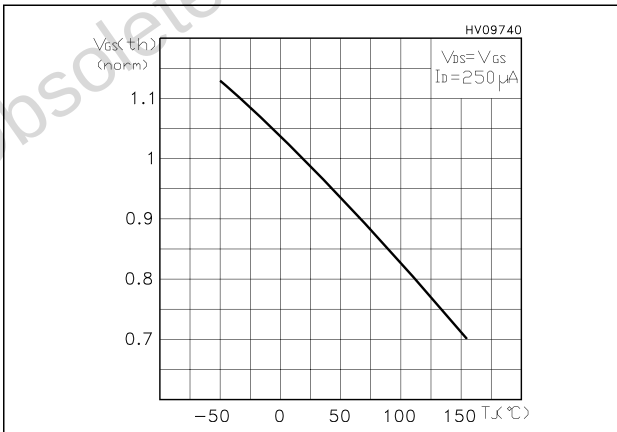


Figure 13. Normalized on resistance vs temperature

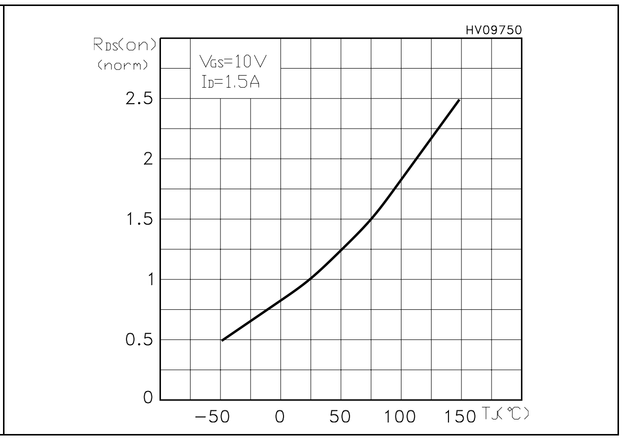
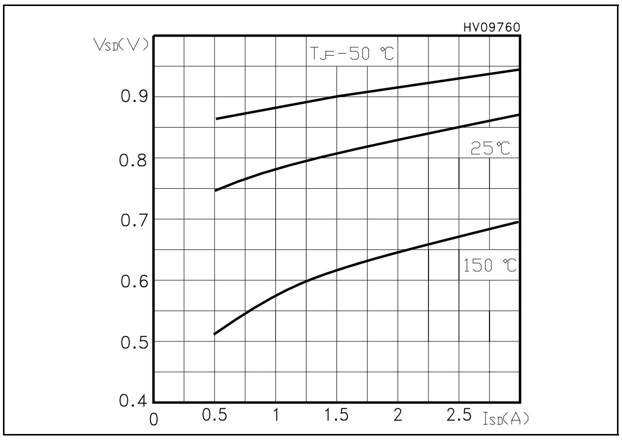


Figure 14. Source-drain diode forward characteristics



3 Test circuits

Figure 15. Switching times test circuit for resistive load

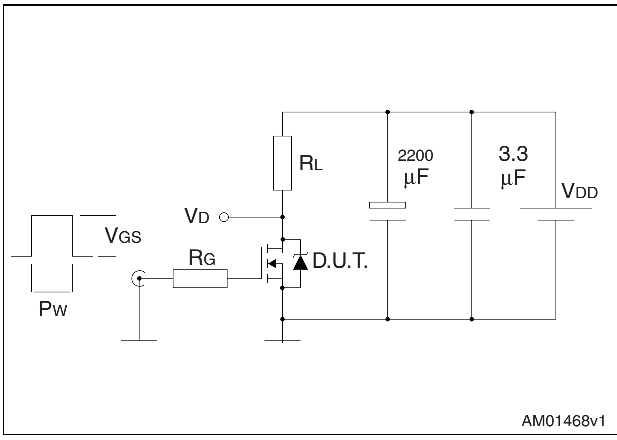


Figure 16. Gate charge test circuit

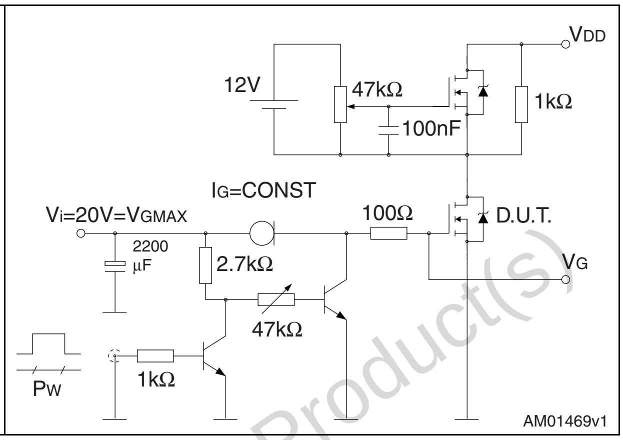


Figure 17. Test circuit for inductive load switching and diode recovery times

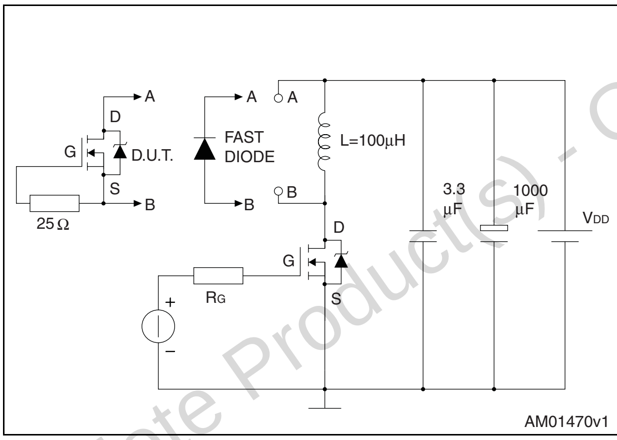


Figure 18. Unclamped inductive load test circuit

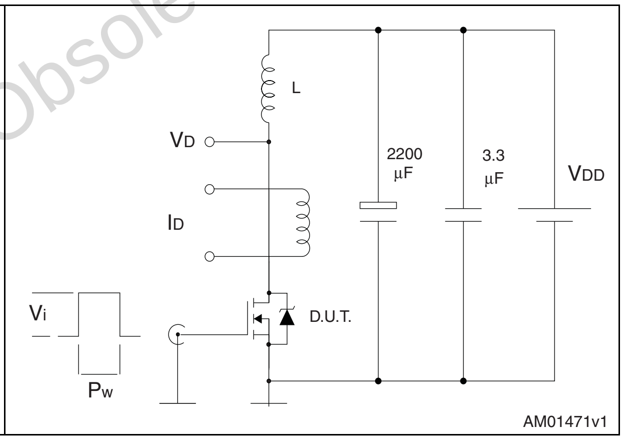


Figure 19. Unclamped inductive waveform

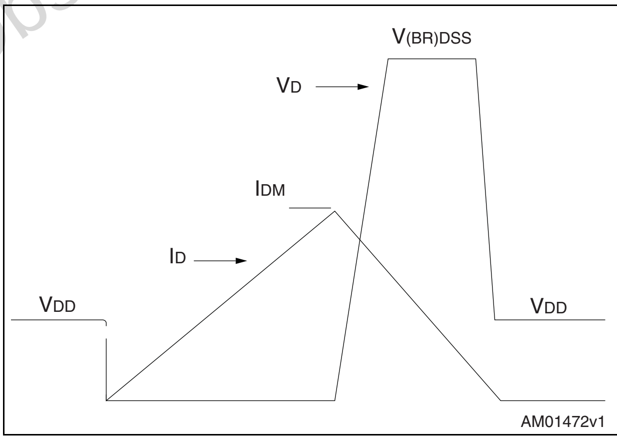


Figure 20. Switching time waveform

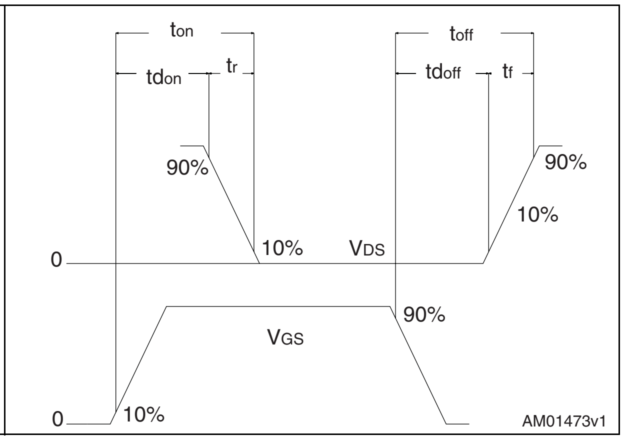
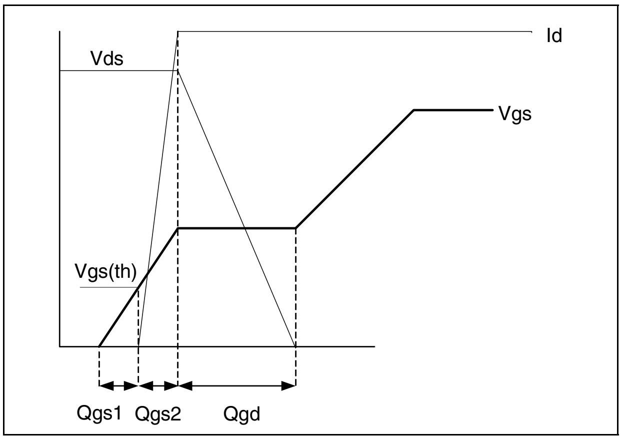


Figure 21. Gate charge waveform

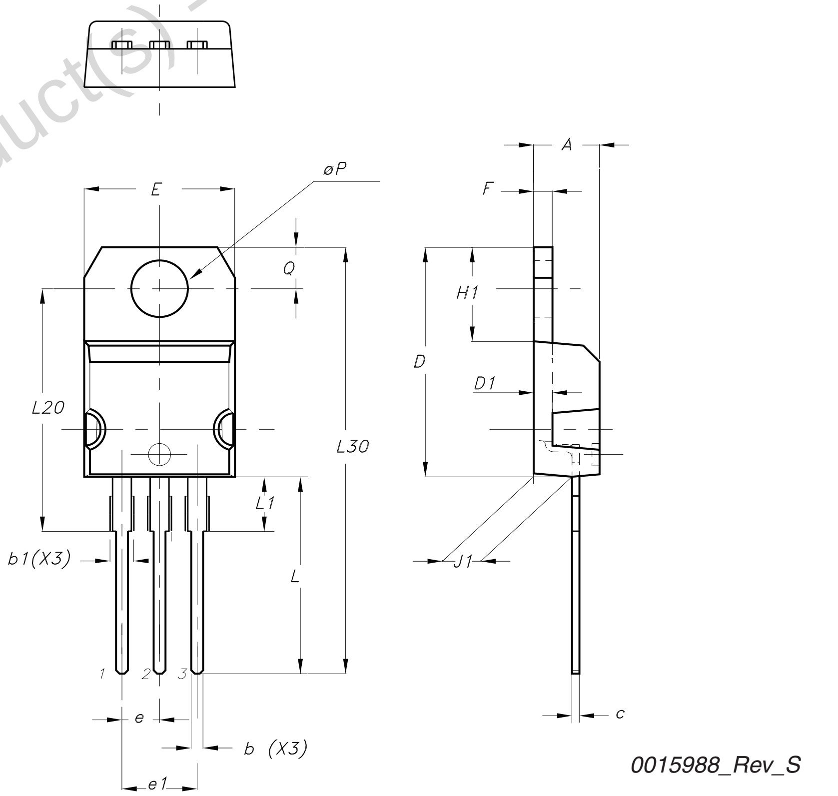


4 Package mechanical data

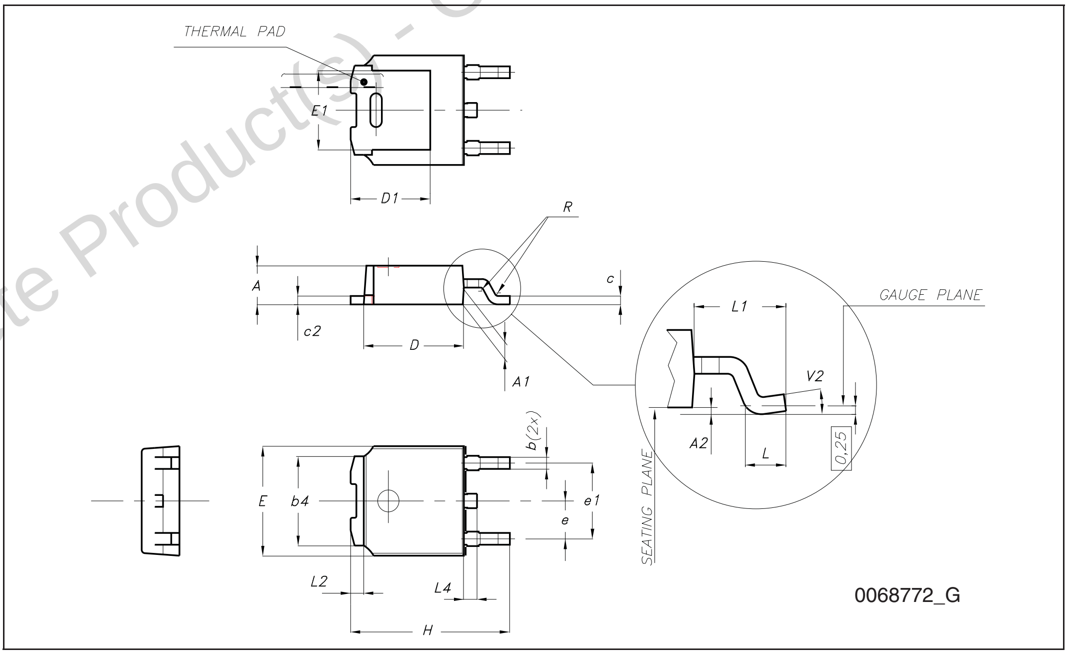
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95

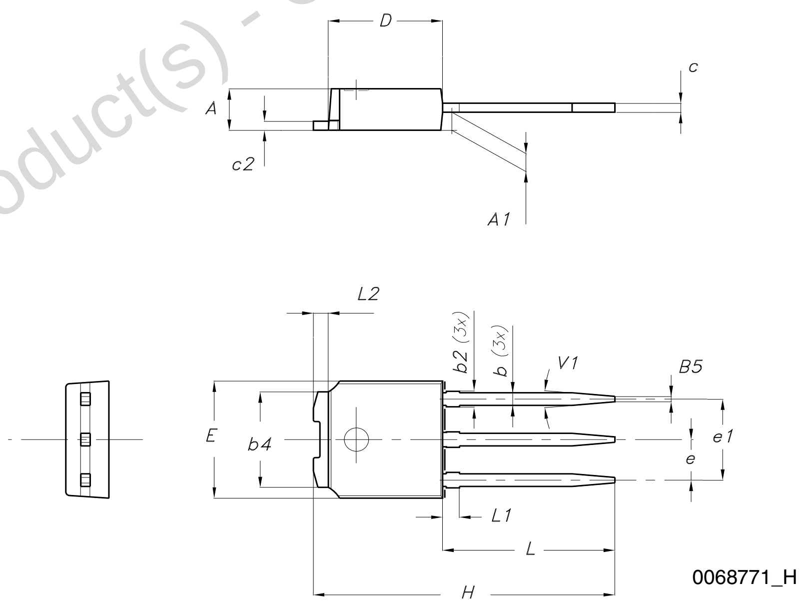


TO-252 (DPAK) mechanical data			
DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



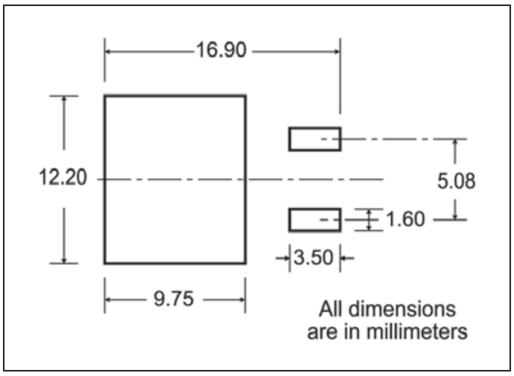
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 °	

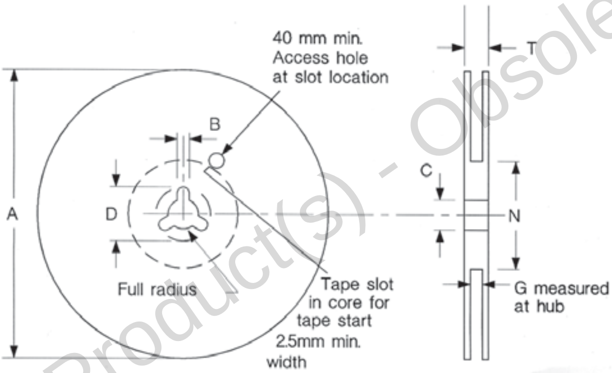


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



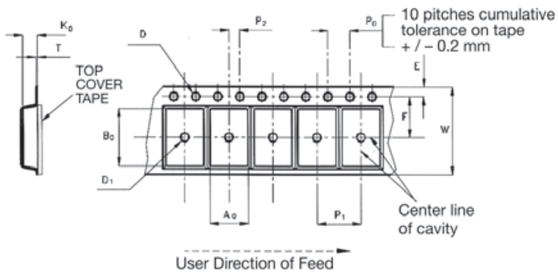
REEL MECHANICAL DATA

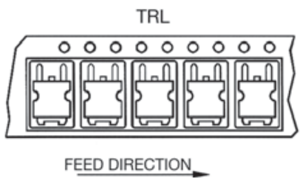
DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

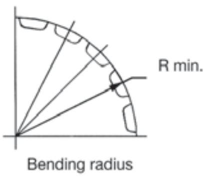
BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956







6 Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Jan-2004	3	
02-Sep-2009	4	Inserted V_{DSS} value @ T_{jmax} = 150 °C on cover page Document reformatted to improve readability