2N5088, 2N5089

Amplifier Transistors

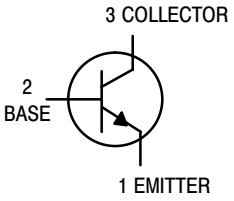
NPN Silicon

ON Semiconductor®

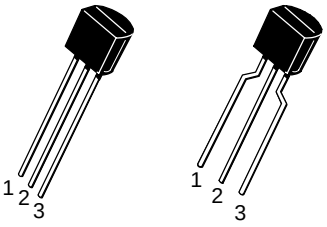
http://onsemi.com

Features

- Pb−Free Packages are Available*



TO−92
CASE 29
STYLE 1



STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector − Emitter Voltage 2N5088 2N5089	V_{CEO}	 30 25	Vdc
Collector − Base Voltage 2N5088 2N5089	V_{CBO}	 35 30	Vdc
Emitter − Base Voltage	V_{EBO}	3.0	Vdc
Collector Current − Continuous	I_C	50	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

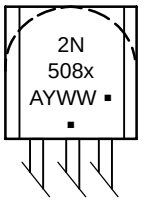
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83.3	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $R_{\theta JA}$ is measured with the device soldered into a typical printed circuit board.

MARKING DIAGRAM



x = 8 or 9
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
2N5088G	TO−92 (Pb−Free)	5000 Units/Bulk
2N2088RLRAG	TO−92 (Pb−Free)	2000/Tape & Reel
2N5089G	TO−92 (Pb−Free)	5000 Units/Bulk
2N2089RLRE	TO−92	2000/Tape & Reel

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (Note 2)		$V_{(BR)CEO}$			Vdc
(I_C = 1.0 mAdc, I_B = 0)	2N5088		30	−	
	2N5089		25	−	
Collector−Base Breakdown Voltage		$V_{(BR)CBO}$			Vdc
(I_C = 100 μAdc, I_E = 0)	2N5088		35	−	
	2N5089		30	−	
Collector Cutoff Current		I_{CBO}			nAdc
(V_{CB} = 20 Vdc, I_E = 0)	2N5088		−	50	
(V_{CB} = 15 Vdc, I_E = 0)	2N5089		−	50	
Emitter Cutoff Current		I_{EBO}			nAdc
($V_{EB(off)}$ = 3.0 Vdc, I_C = 0)			−	50	
($V_{EB(off)}$ = 4.5 Vdc, I_C = 0)			−	100	
ON CHARACTERISTICS					
DC Current Gain		h_{FE}			−
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc)	2N5088		300	900	
	2N5089		400	1200	
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc)	2N5088		350	−	
	2N5089		450	−	
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc) (Note 2)	2N5088		300	−	
	2N5089		400	−	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$	−	0.5	Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)					
Base−Emitter On Voltage		$V_{BE(on)}$	−	0.8	Vdc
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc) (Note 2)					
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product		f_T	50	−	MHz
(I_C = 500 μAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)					
Collector−Base Capacitance		C_{cb}	−	4.0	pF
(V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)					
Emitter−Base Capacitance		C_{eb}	−	10	pF
(V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)					
Small−Signal Current Gain		h_{fe}			−
(I_C = 1.0 mAdc, V_{CE} = 5.0 Vdc, f = 1.0 kHz)	2N5088		350	1400	
	2N5089		450	1800	
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)	2N5088		−	3.0	
	2N5089		−	2.0	

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

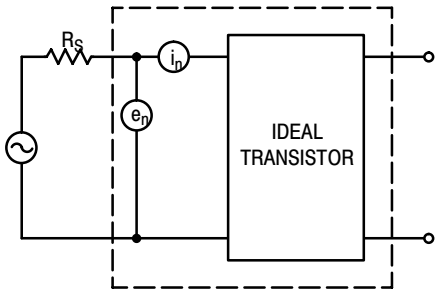


Figure 1. Transistor Noise Model

NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

NOISE VOLTAGE

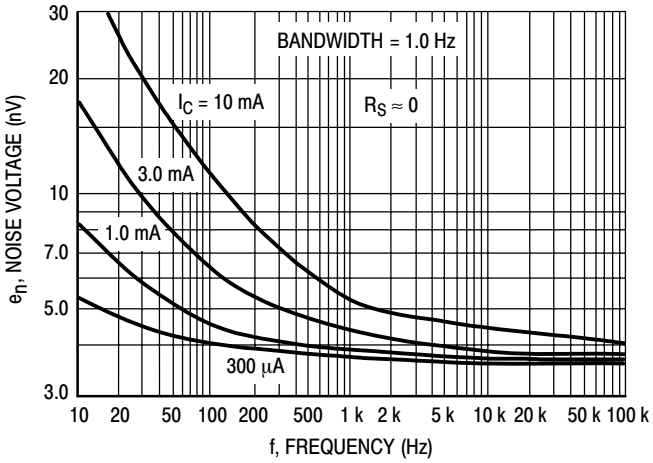


Figure 2. Effects of Frequency

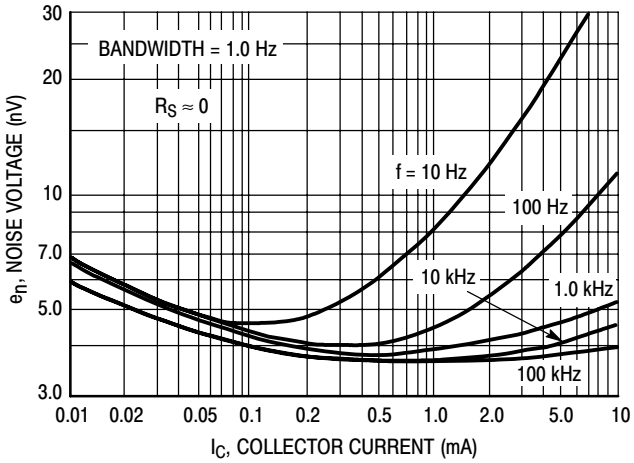


Figure 3. Effects of Collector Current

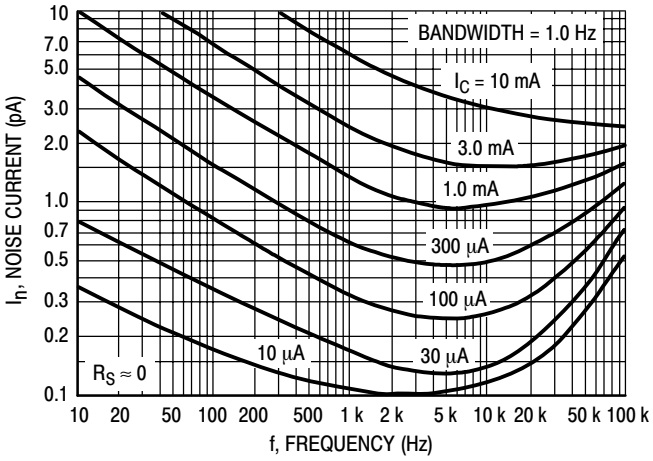


Figure 4. Noise Current

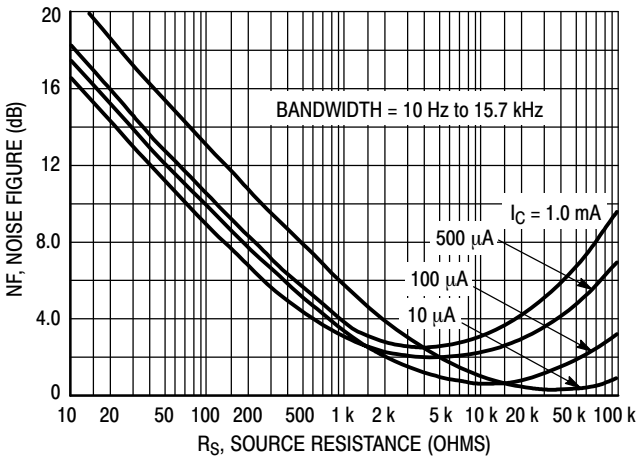


Figure 5. Wideband Noise Figure

100 Hz NOISE DATA

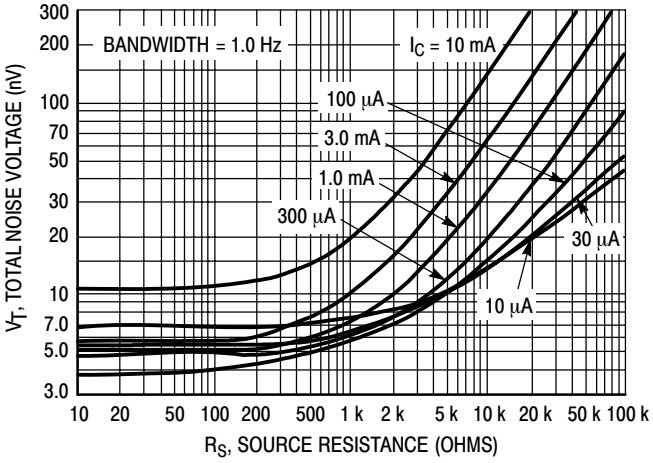


Figure 6. Total Noise Voltage

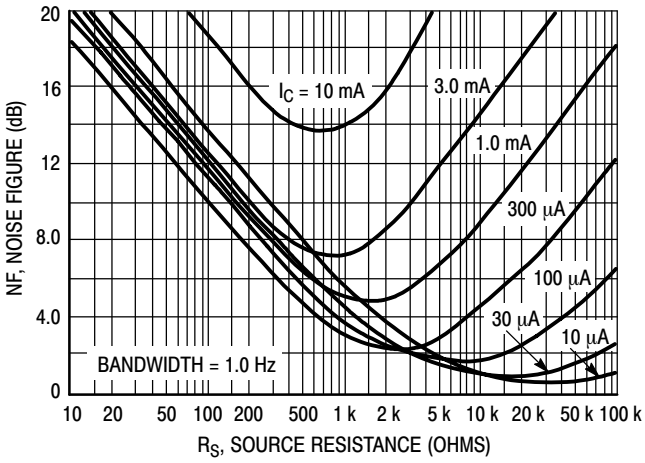


Figure 7. Noise Figure

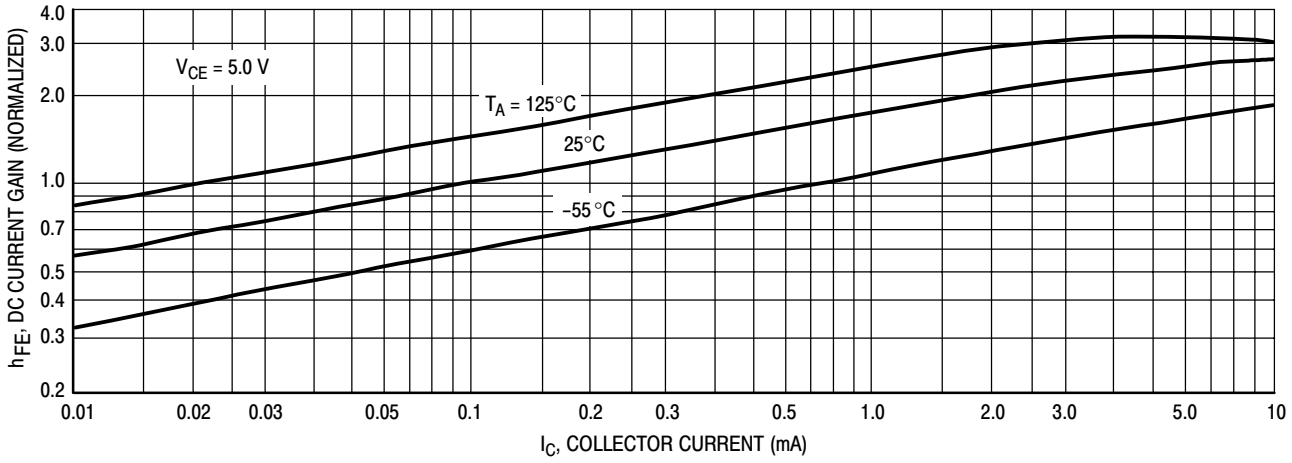


Figure 8. DC Current Gain

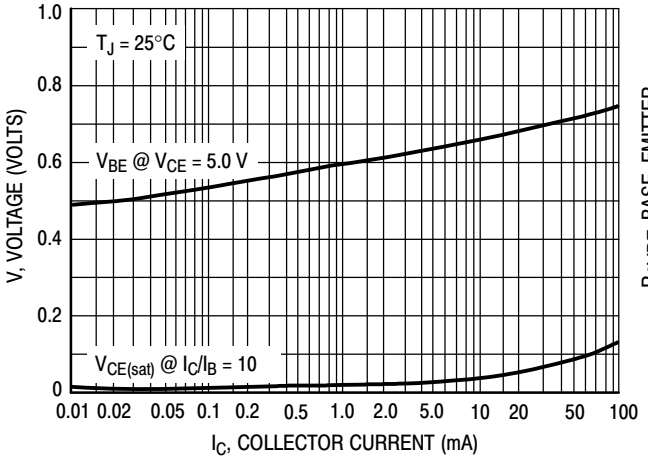


Figure 9. “On” Voltages

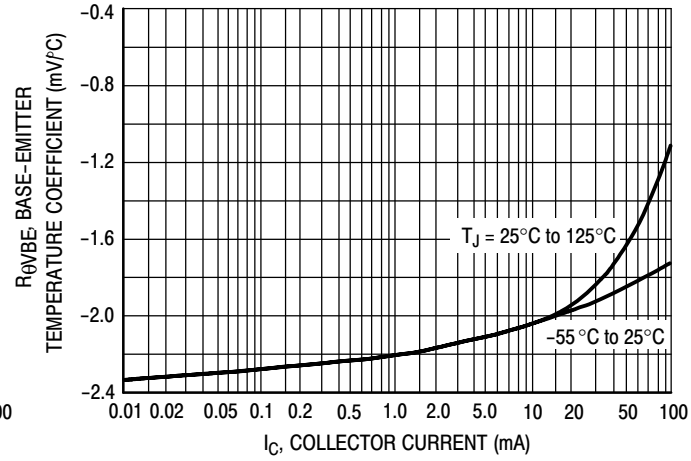


Figure 10. Temperature Coefficients

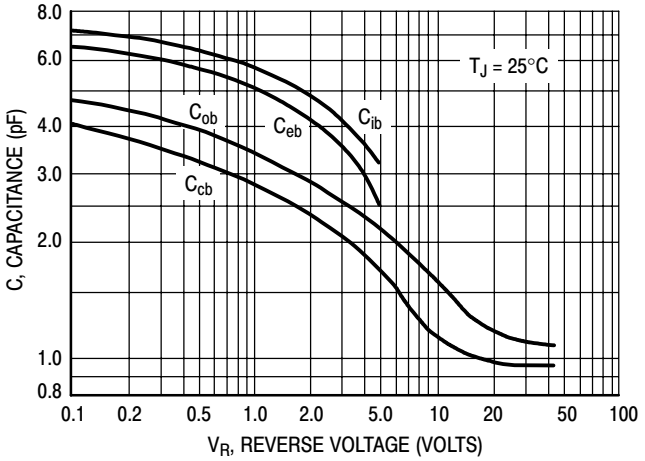


Figure 11. Capacitance

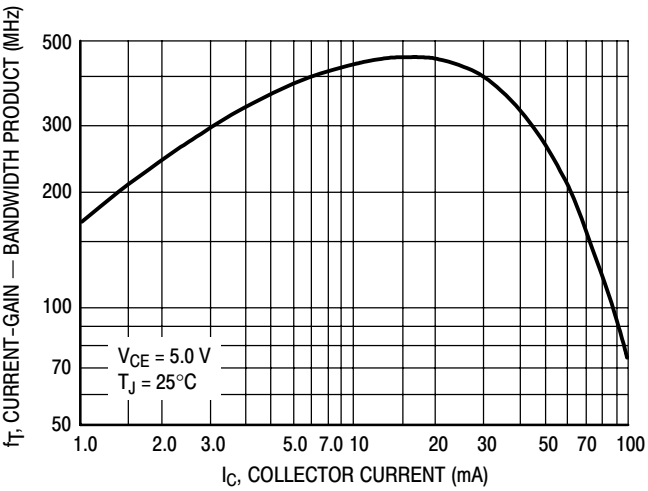


Figure 12. Current−Gain — Bandwidth Product

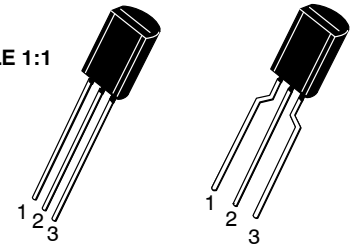
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

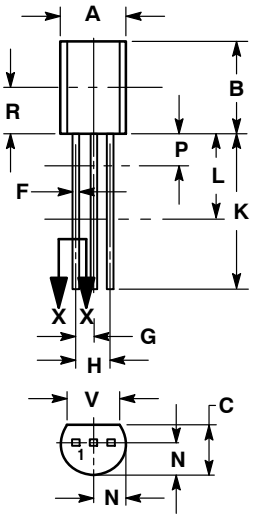
TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

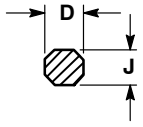
SCALE 1:1



STRAIGHT LEAD BENT LEAD



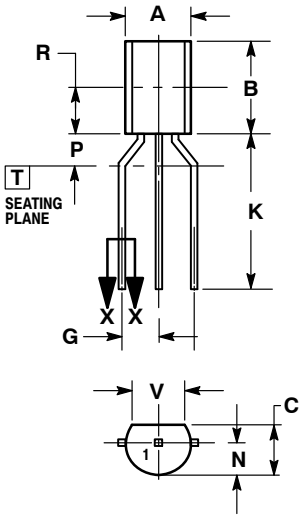
STRAIGHT LEAD



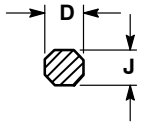
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---



BENT LEAD



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN DIMENSIONS P AND L. DIMENSIONS D AND J APPLY BETWEEN DIMENSIONS L AND K MINIMUM. THE LEAD DIMENSIONS ARE UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.44	5.21
B	0.290	0.310	7.37	7.87
C	0.125	0.165	3.18	4.19
D	0.018	0.021	0.46	0.53
G	0.094	0.102	2.40	2.80
J	0.018	0.024	0.46	0.61
K	0.500	---	12.70	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.135	---	3.43	---
V	0.135	---	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98AON52857E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−92 (TO−226) 1 WATT**	**PAGE 1 OF 2**

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE A

DATE 08 MAY 2012

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

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