# STL6NM60N

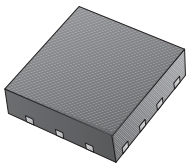
## N-channel 600 V - 0.85 Ω - 5.75 A - PowerFLAT™ (5x5) ultra low gate charge MDmesh™ II Power MOSFET

## Features

| Type | $V_{DSS}$ @ $T_{JMAX}$ | $R_{DS(on)}$ Max | $I_D$ |
|---|---|---|---|
| STL6NM60N | 650 V | < 0.92 Ω | 5.75 A(1) |

1. The value is rated according Rthj-case

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



**PowerFLAT (5x5)**

## Application

- Switching applications

## Description

This series of devices implements the second generation of MDmesh™ Technology. This revolutionary Power MOSFET associates a new vertical structure to the Company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

**Figure 1. Internal schematic diagram**

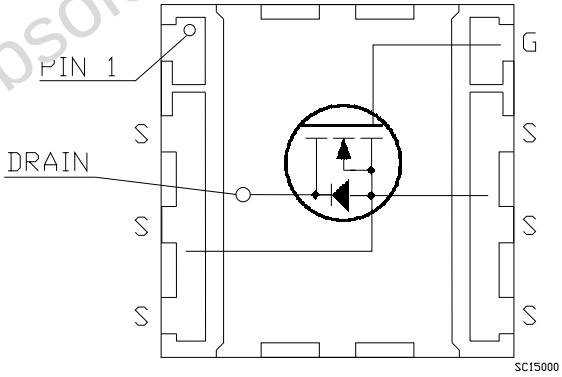



**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL6NM60N | L6NM60N | PowerFLAT™ (5x5) | Tape & reel |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 600 | V |
| $V_{GS}$ | Gate-source voltage | ± 25 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25 °C (steady state) | 5.75 | A |
| $I_D$ (1) | Drain current (continuous) at $T_C$=100 °C | 3.62 | A |
| $I_{DM}$ (1),(2) | Drain current (pulsed) | 23 | A |
| $I_D$ (3) | Drain current (continuous) at $T_C$ = 25 °C | 1 | A |
| $I_D$ (3) | Drain current (continuous) at $T_C$=100 °C | 0.65 | A |
| $I_{DM}$ (2), (3) | Drain current (pulsed) | 4 | A |
| $P_{TOT}$ (3) | Total dissipation at $T_C$ = 25 °C (steady state) | 2.1 | W |
| $P_{TOT}$ (1) | Total dissipation at $T_C$ = 25 °C (steady state) | 70 | W |
| | Derating factor (3) | 0.02 | W/°C |
| dv/dt (4) | Peak diode recovery voltage slope | 5 | V/ns |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>storage temperature | -55 to 150 | °C |

1. The value is rated according Rthj-case
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of 1inch², 2oz Cu
4. $I_{SD}$ ≤4.6A, dv/dt ≤ 400A/µs, $V_{DD}$ = 80%$V_{(BR)DSS}$

**Table 3. Thermal resistance**

| Symbol | Parameter | Typ | Max | Unit |
|---|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | -- | 1.8 | °C/W |
| $R_{thj\text{-}pcb}$ (1) | Thermal resistance junction-pcb | 31.2 | 58.5 | °C/W |

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $I_{AS}$ | Avalanche current, repetitive or not-repetitive (1) | 2 | A |
| $E_{AS}$ | Single pulse avalanche energy (2) | 65 | mJ |

1. Pulse width limited by Tjmax
2. Starting Tj = 25 °C, $I_D$= $I_{AS}$, $V_{DD}$ = 50 V

# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 5. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$= 0 | 600 | | | V |
| dv/dt (1) | Drain-source voltage slope | $V_{DD}$= 480 V, $V_{GS}$ = 10 V, $I_D$ = 4.6 A | | 40 | | V/ns |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = Max rating,<br>$V_{DS}$ = Max rating @125 °C | | | 1<br>100 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$= $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10 V, $I_D$= 2.3 A | | 0.85 | 0.92 | Ω |

1. Characteristics value at turn off on inductive load

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$ =15 V, $I_D$ = 2.3 A | | 4 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ =50V, f=1 MHz, $V_{GS}$=0 | | 420<br>30<br>4 | | pF<br>pF<br>pF |
| $C_{oss\ eq.}$ (2) | Output equivalent capacitance | $V_{GS}$ =0, $V_{DS}$ =0 to 480 V | | 70 | | pF |
| Rg | Gate input resistance | f=1 MHz Gate DC Bias=0<br>test signal level = 20 mV<br>open drain | | 6 | | Ω |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$= 480 V, $I_D$ = 4.6 A<br>$V_{GS}$ =10 V<br>*(see Figure 15)* | | 13<br>2<br>7 | | nC<br>nC<br>nC |

1. Pulsed: pulse duration= 300 µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on delay time<br>Rise time<br>Turn-off delay time<br>Fall time | $V_{DD}$= 300 V, $I_D$ = 2.3 A,<br>$R_G$= 4.7 Ω, $V_{GS}$ = 10 V<br>*(see Figure 14)* | | 10<br>8<br>40<br>9 | | ns<br>ns<br>ns<br>ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | | | 1 | A |
| $I_{SDM}$ (1), (2) | Source-drain current (pulsed) | | | | 4 | A |
| $V_{SD}$(3) | Forward on voltage | $I_{SD}$= 4.6 A, $V_{GS}$=0 | | | 1.3 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$= 4.6 A,<br>di/dt = 100 A/µs,<br>$V_{DD}$=20 V<br>*(see Figure 16)* | | 300<br>2<br>12 | | ns<br>nC<br>A |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$= 4.6 A,<br>di/dt = 100 A/µs,<br>$V_{DD}$=20 V, Tj= 150 °C<br>*(see Figure 16)* | | 470<br>3<br>12 | | ns<br>nC<br>A |

1. Pulse width limited by safe operating area
2. When mounted on FR-4 board of 1inch², 2oz Cu
3. Pulsed: pulse duration=300µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area**

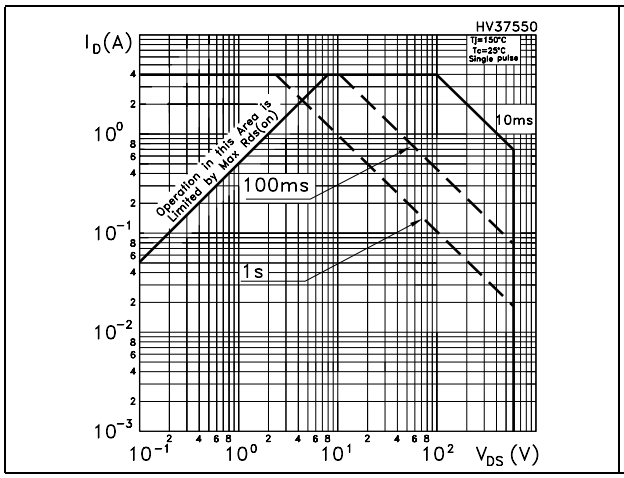



**Figure 3. Thermal impedance**

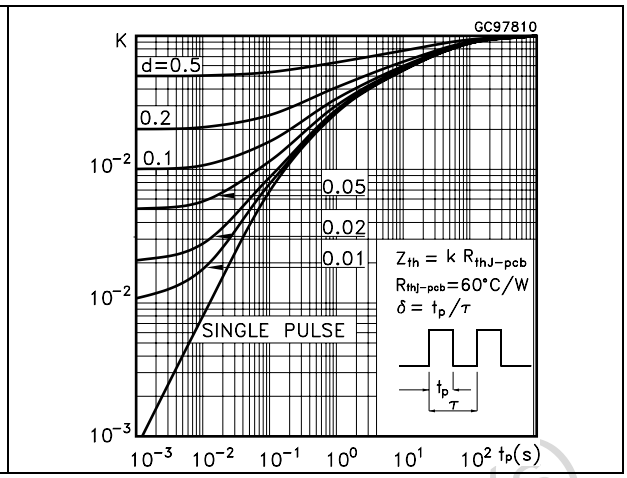



**Figure 4. Output characteristics**

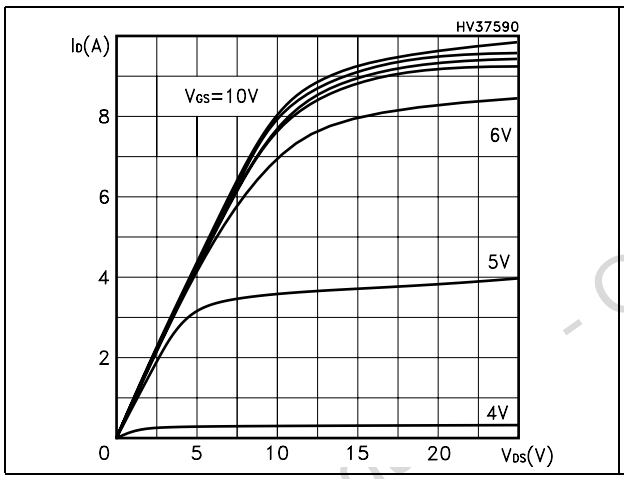



**Figure 5. Transfer characteristics**

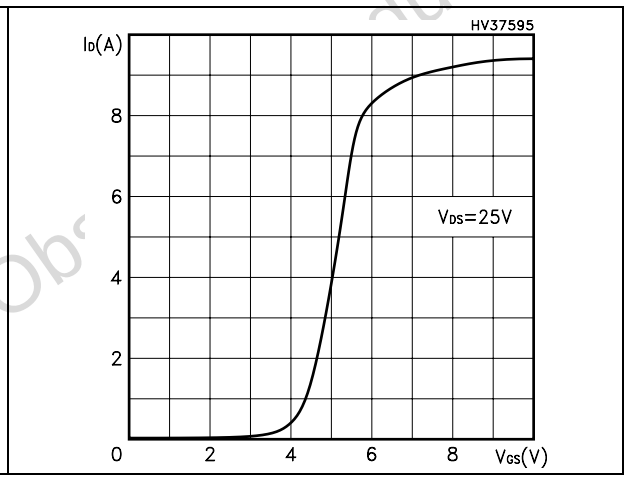



**Figure 6. Transconductance**

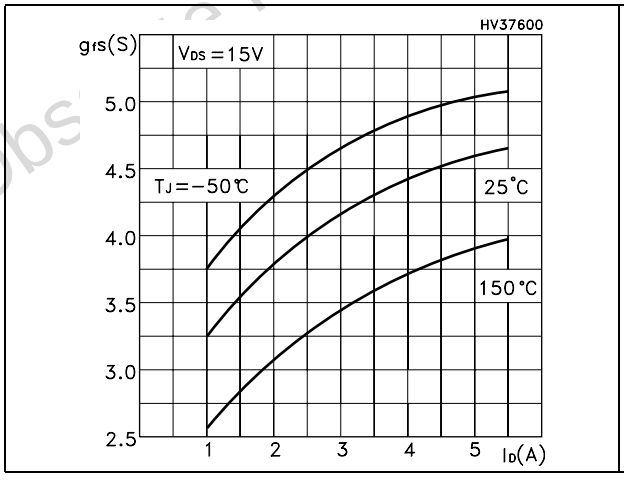



**Figure 7. Static drain-source on resistance**

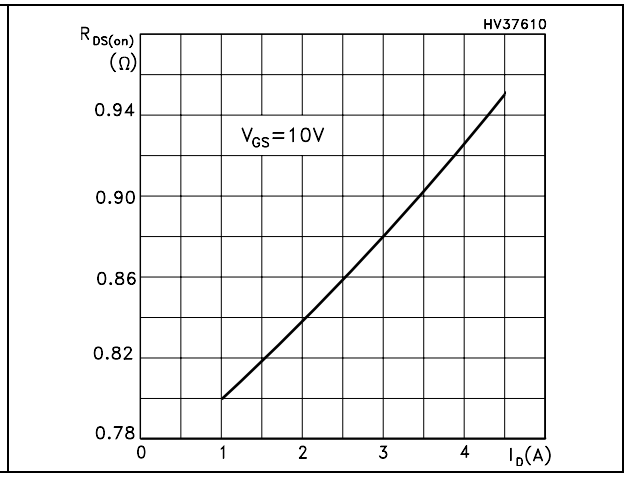


**Figure 8. Gate charge vs gate-source voltage**

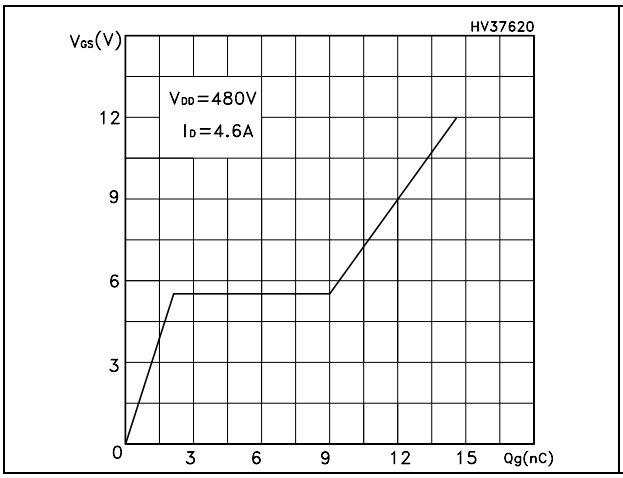



**Figure 9. Capacitance variations**

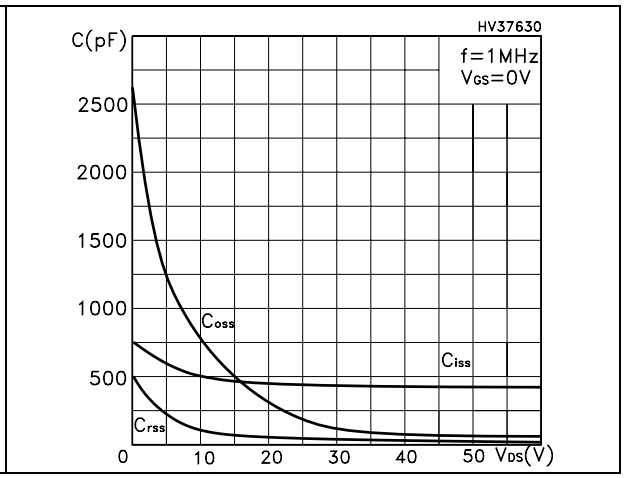



**Figure 10. Normalized gate threshold voltage vs temperature**

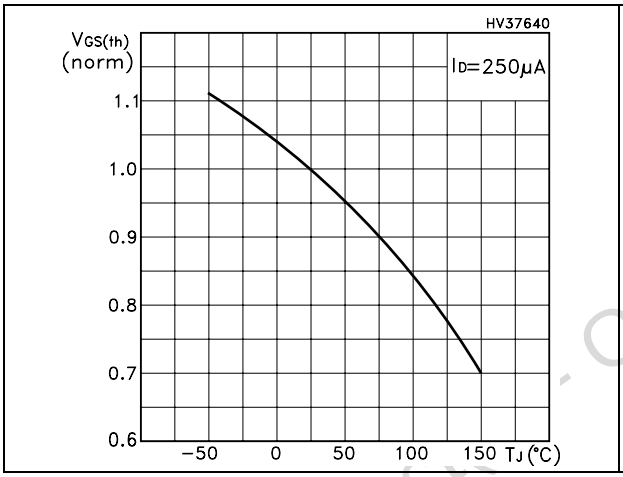



**Figure 11. Normalized on resistance vs temperature**

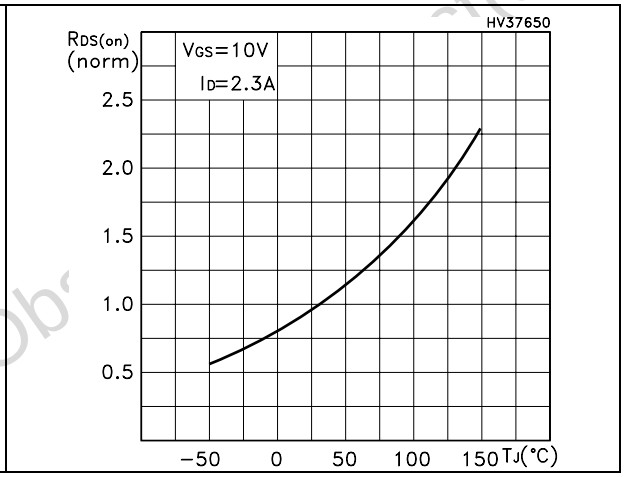



**Figure 12. Source-drain diode forward characteristics**

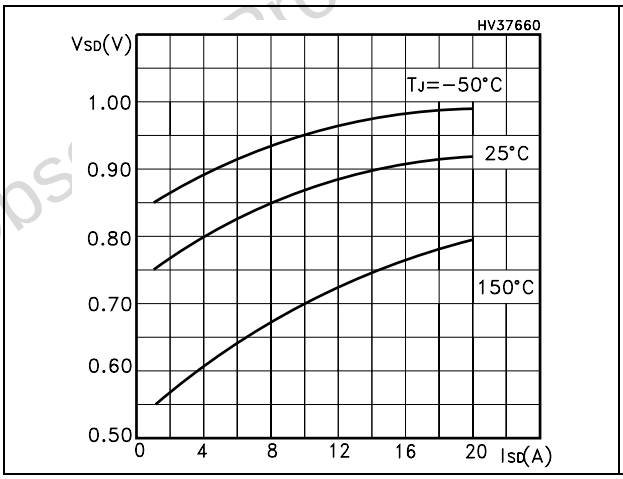
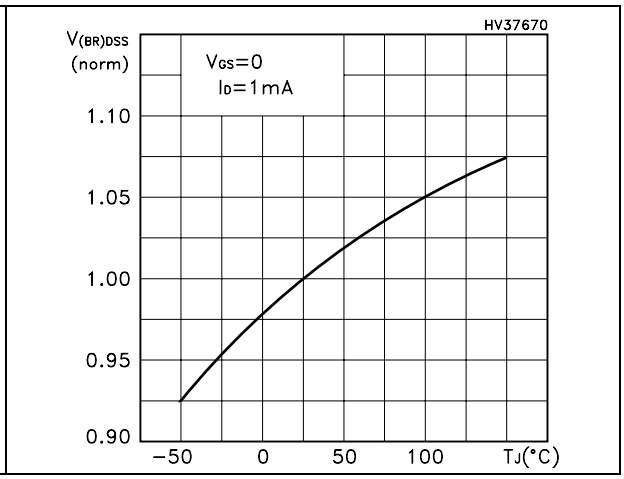



**Figure 13. Normalized $B_{VDSS}$ vs temperature**



# 3 Test circuit

**Figure 14. Switching times test circuit for resistive load**

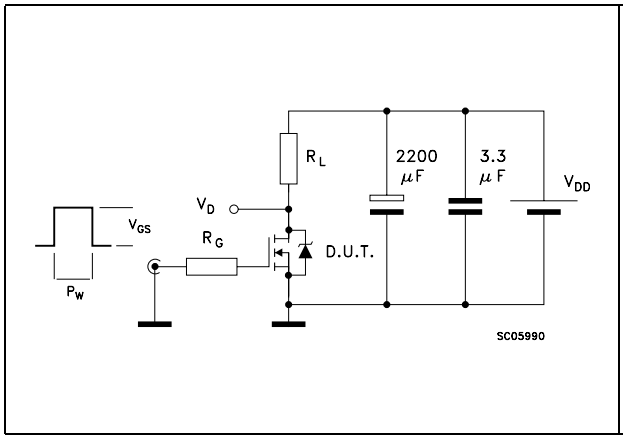



**Figure 15. Gate charge test circuit**

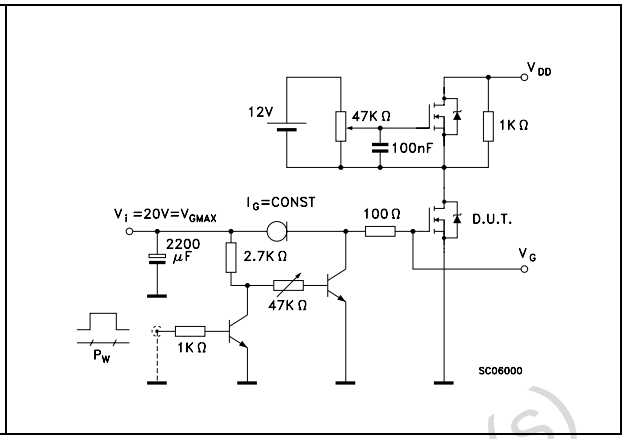



**Figure 16. Test circuit for inductive load switching and diode recovery times**

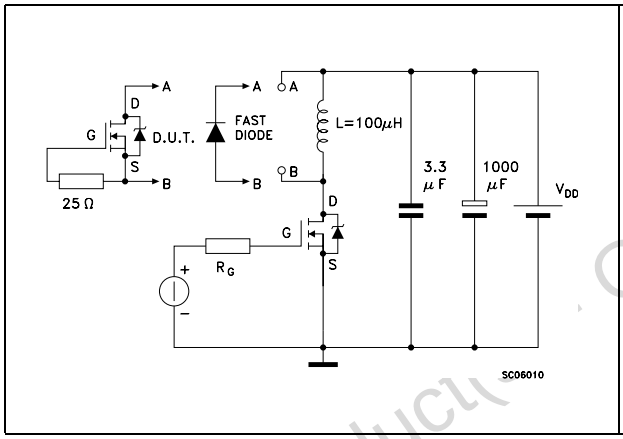



**Figure 17. Unclamped inductive load test circuit**

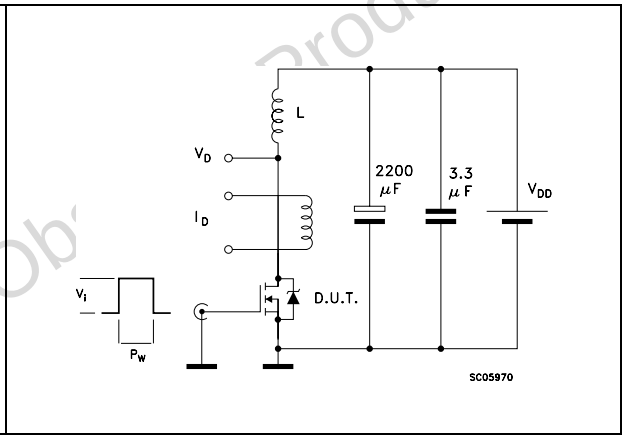



**Figure 18. Unclamped inductive waveform**

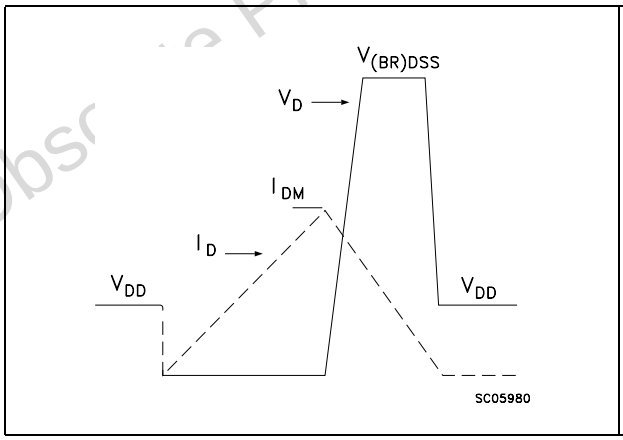
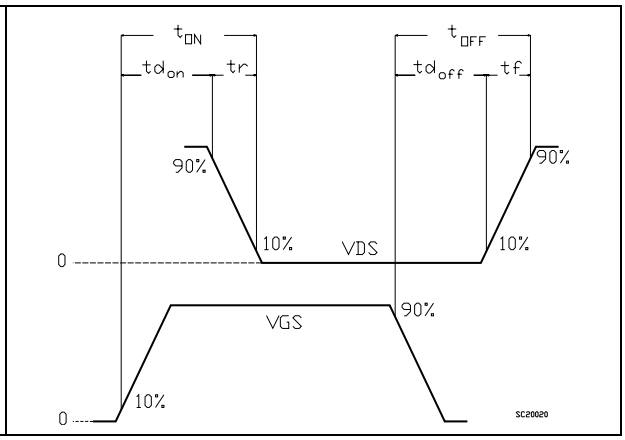



**Figure 19. Switching time waveform**

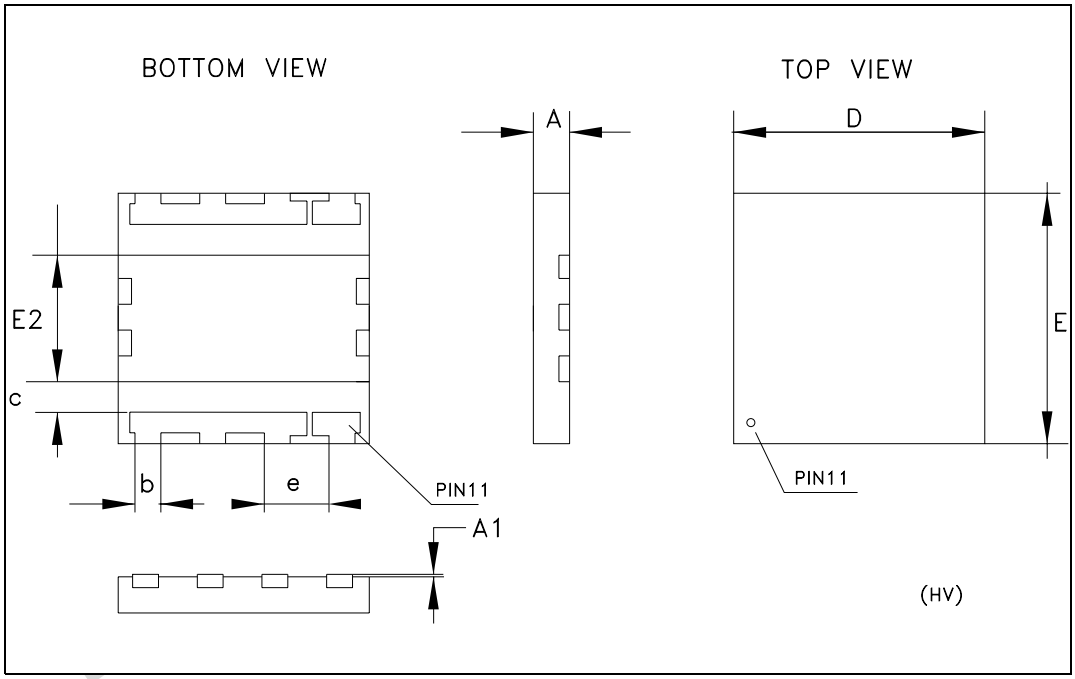


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

## PowerFLAT™(5x5) MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 0.80 | 0.90 | 1.00 | 0.031 | 0.035 | 0.039 |
| A1 | | 0.02 | 0.05 | | 0.0007 | 0.002 |
| A3 | | 0.24 | | | 0.009 | |
| b | 0.43 | 0.51 | 0.58 | 0.016 | 0.020 | 0.022 |
| c | 0.64 | 0.71 | 0.79 | 0.025 | 0.027 | 0.031 |
| D | | 5.00 | | | 0.19 | |
| E | | 5.00 | | | 0.19 | |
| E2 | 2.49 | 2.57 | 2.64 | 0.01 | 0.10 | 0.103 |
| e | | 1.27 | | | 0.05 | |



# 5 Revision history

**Table 9. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 04-May-2007 | 1 | First release |
| 23-May-2007 | 2 | Update test conditions on *Table 7* |
| 27-Nov-2007 | 3 | Mechanical data has been updated |

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