



STC5DNF30V

N-channel 30 V, 0.027 Ω , 5 A TSSOP8
2.7 V - driver STripFET™ Power MOSFET

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STC5DNF30V	30V	< 0.031 Ω (@ 4.5 V) < 0.035 Ω (@ 2.7 V)	5 A

- Ultra low threshold gate drive (2.7 V)
- Standard outline for easy automated surface mount assembly

Applications

- Switching application

Description

This Power MOSFET is the latest development of STMicroelectronics unique “single feature size” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

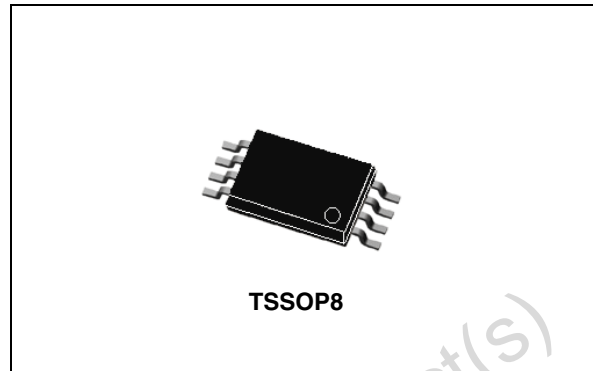


Figure 1. Internal schematic diagram

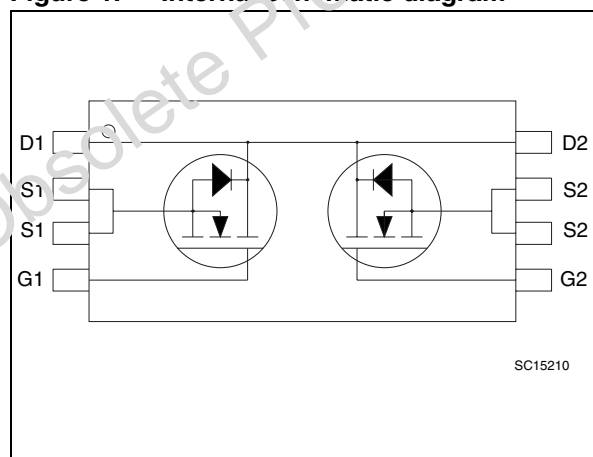


Table 1. Device summary

Order codes	Marking	Package	Packaging
STC5DNF30V	5DN3V	TSSOP8	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	30	V
V_{GS}	Gate-source voltage	± 8	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	4.5	A
I_D	Drain current (continuous) at $T_C=100^\circ\text{C}$	2.8	A
$I_{DM}^{(1)}$	Drain current (pulsed)	18	A
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	1.3	W
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_J	Max. operating junction temperature	-55 to 150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-pbc}$	Thermal resistance junction-pbc max	120 ⁽¹⁾	$^\circ\text{C}/\text{W}$
$R_{thj-pbc}$	Thermal resistance junction-pbc max	97.5 ⁽²⁾	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board with 1 inch² pad, 2 oz of Cu and t = 10 sec
 2. When mounted on minimum recommended footprint

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0$	30			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating @ } 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 8\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	0.6			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 2.3\text{ A}$ $V_{GS} = 2.7\text{ V}$, $I_D = 2.3\text{ A}$		0.032 0.036	0.035 0.040	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{ V}$, $I_D = 2.3\text{ A}$	-	9.5		S
C_{iss}	Input capacitance	$V_{DS} = 15\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	460		pF
C_{oss}	Output capacitance			200		pF
C_{rss}	Reverse transfer capacitance			50		pF
Q_g	Total gate charge	$V_{DD} = 16\text{ V}$, $I_D = 4.5\text{ A}$	-	8.5	11.5	nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\text{ V}$		1.8		nC
Q_{gd}	Gate-drain charge	(see Figure 15)		2.4		nC

1. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10\text{ V}$, $I_D = 2.3\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 4.5\text{ V}$ (see Figure 14)	-	7		ns
t_r	Rise time			33		ns
$t_{d(off)}$	Turn-off delay time			27	-	ns
t_f	Fall time			10		ns
$t_{d(off)}$	Off-voltage rise time			26		ns
t_f	Fall time			11		ns
t_c	Cross-over time			21		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		4.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		18	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.5 \text{ A}, V_{GS} = 0$	-		1.2	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.5 \text{ A},$ $di/dt = 100 \text{ A}/\mu\text{s},$ $V_{DD} = 10 \text{ V}, T_J = 150 \text{ }^\circ\text{C}$ (see Figure 16)	-	26		ns
Q_{rr}	Reverse recovery charge			13		nC
I_{RRM}	Reverse recovery current			1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

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2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

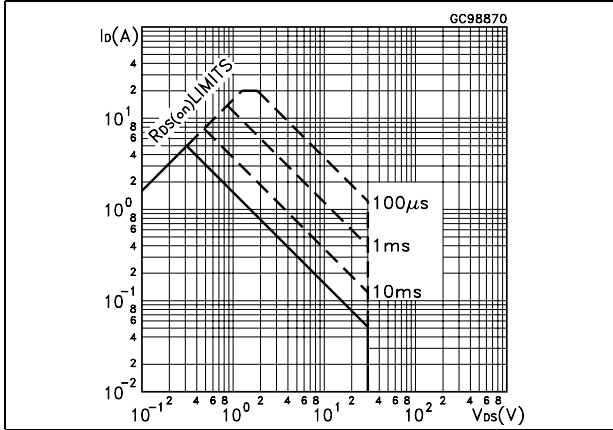


Figure 3. Thermal impedance

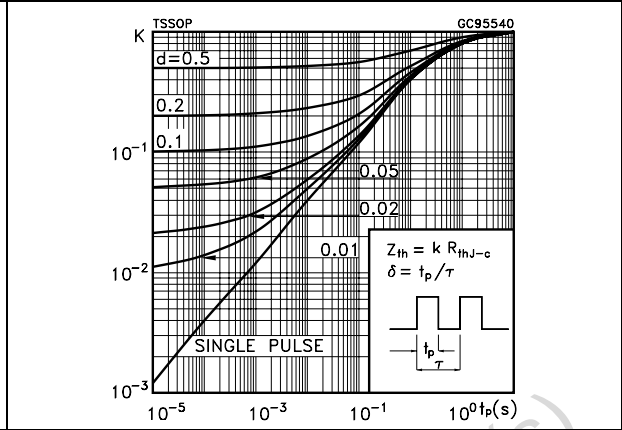


Figure 4. Output characteristics

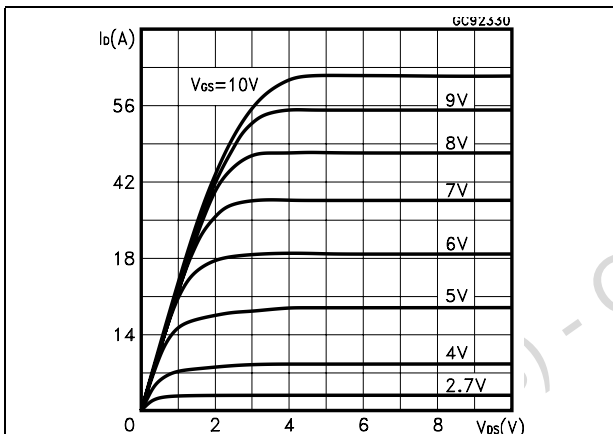


Figure 5. Transfer characteristics

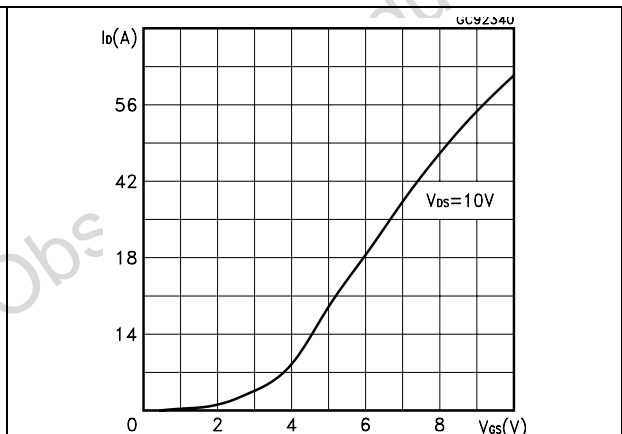


Figure 6. Transconductance

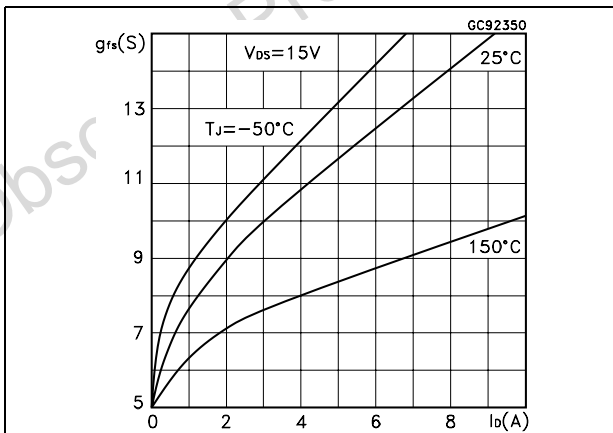


Figure 7. Static drain-source on resistance

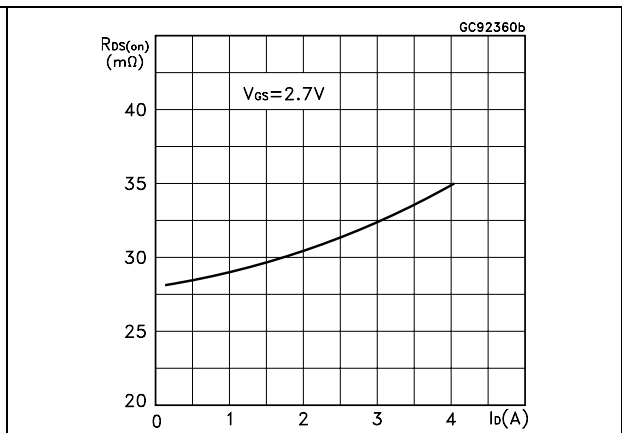


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

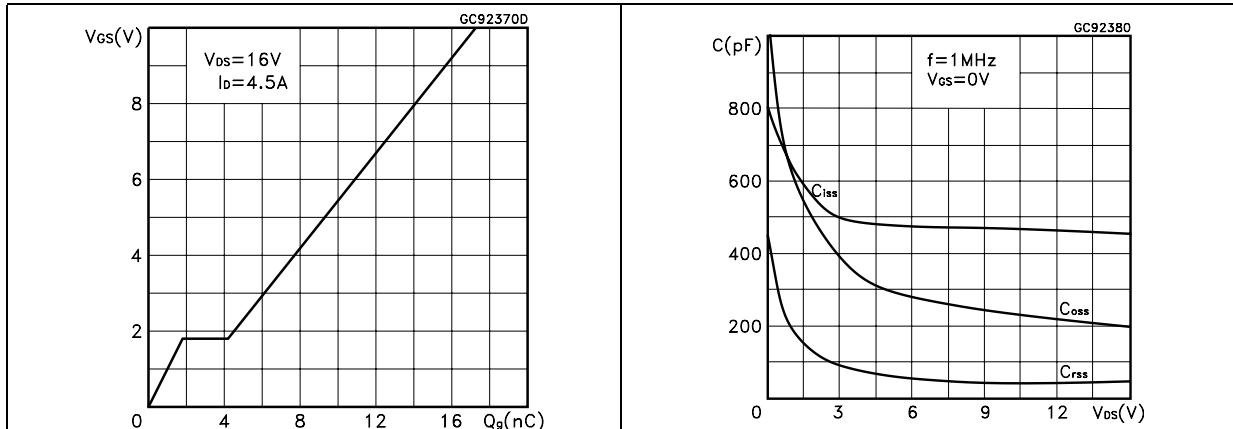


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

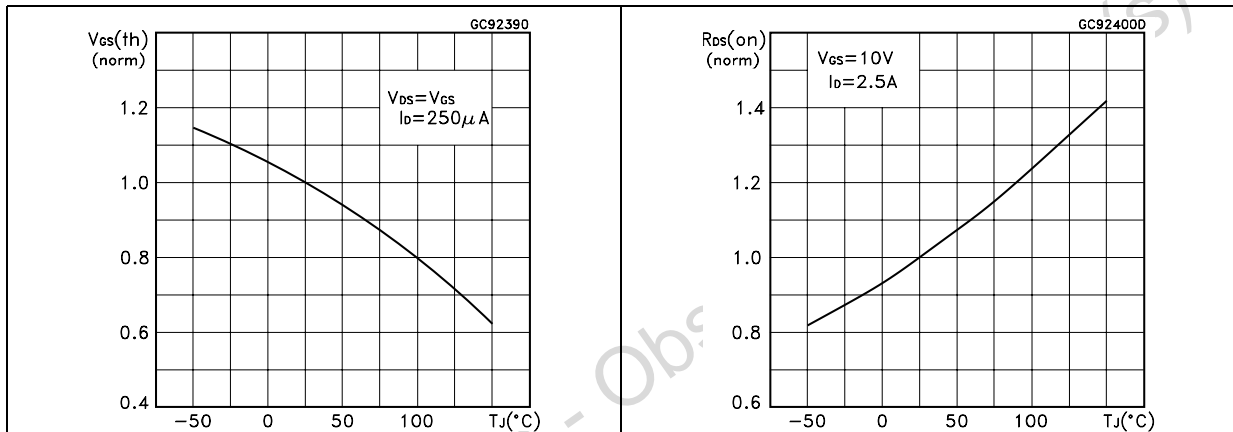
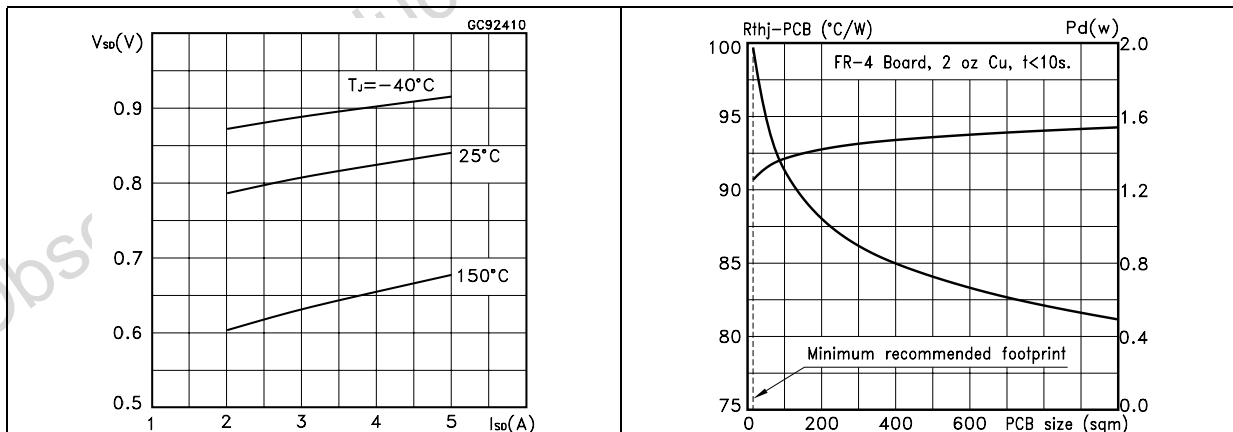


Figure 12. Source-drain diode forward characteristics Figure 13. Thermal resistance and max power



3 Test circuits

Figure 14. Switching times test circuit for resistive load

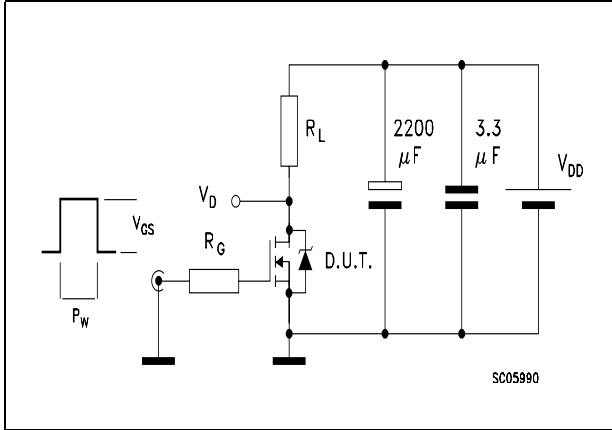


Figure 15. Gate charge test circuit

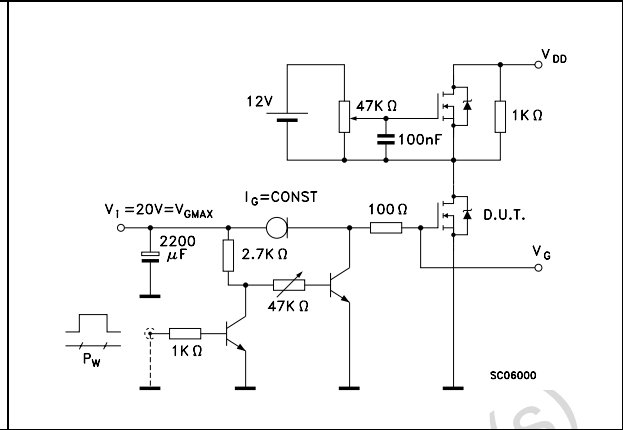


Figure 16. Test circuit for inductive load switching and diode recovery times

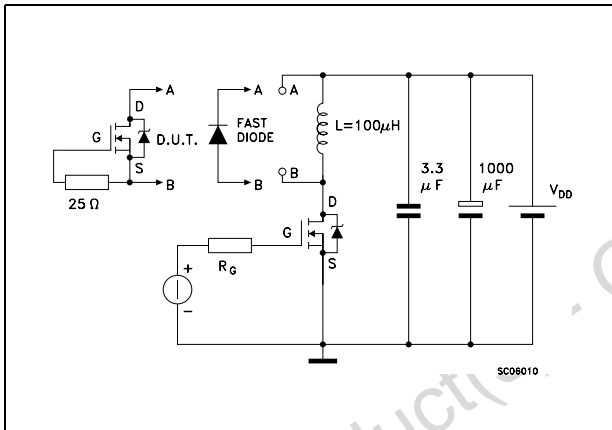


Figure 17. Unclamped inductive load test circuit

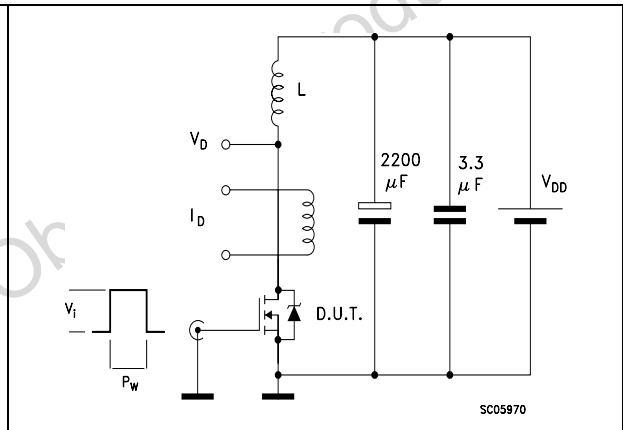
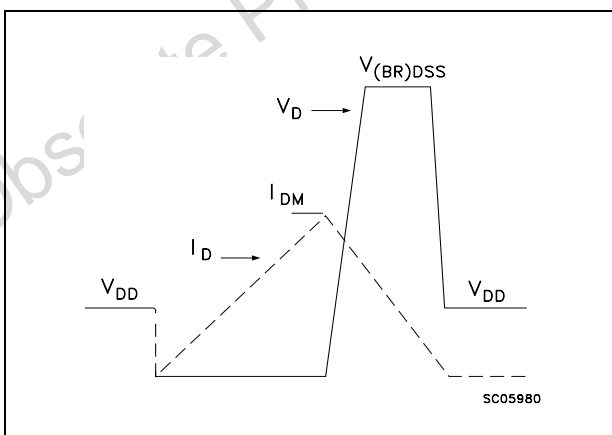


Figure 18. Unclamped inductive waveform



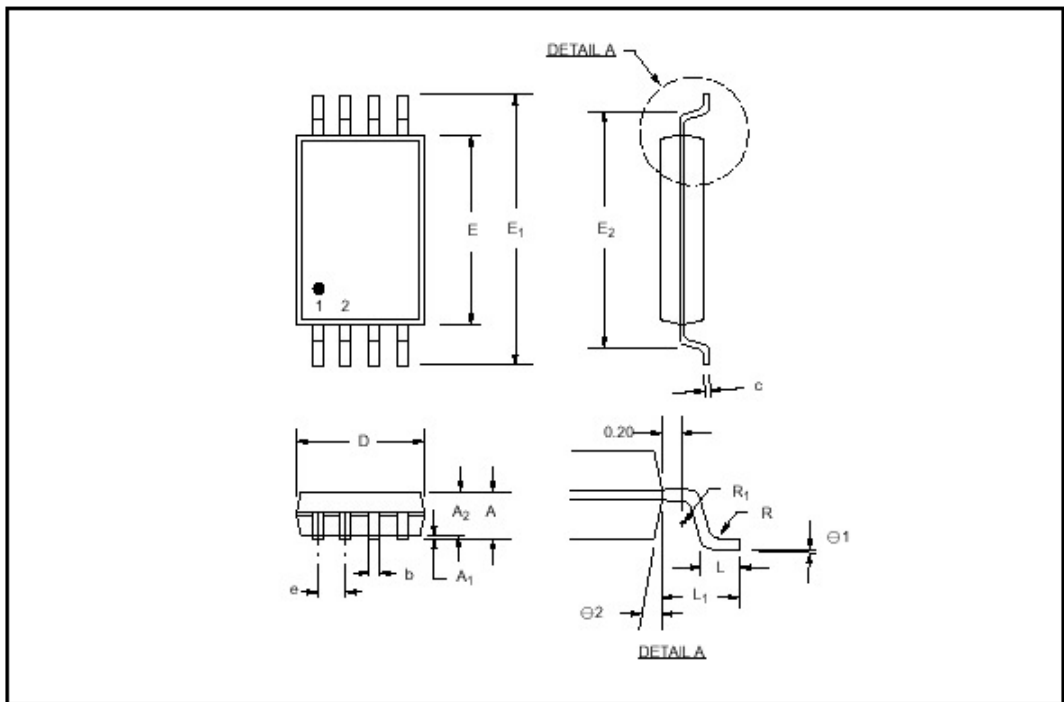
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

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TSSOP8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.05		1.20	0.041		0.047
A1	0.05		0.15	0.002		0.006
A2	0.80		1.05	0.032		0.041
b	0.19		0.30	0.008		0.012
c		0.127			0.005	
D	2.90		3.10	0.114		0.122
E	4.30		4.50	0.170		0.177
E1	6.20		6.60	0.240		0.260
E2	5.14		5.24	0.202		0.206
e		0.65			0.025	
L	0.45		0.75	0.018		0.030
L1	0.90		1.10	0.0355		0.0433
R	0.09			0.004		
R1	0.09			0.004		
θ1	0°		8°	0°		8°
θ2	12°					



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5 Revision history

Table 8. Document revision history

Date	Revision	Changes
11-Apr-2006	1	First release.
05-Nov-2009	2	Updated marking in Table 1 .

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