MOSFET – N-Channel, POWERTRENCH[®]

60 V, 88 A, 3.5 mΩ

FDPF035N06B-F154

Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Features

- $R_{DS(on)} = 2.91 \text{ m}\Omega \text{ (Typ.)} \otimes V_{GS} = 10 \text{ V}, I_D = 88 \text{ A}$
- Low FOM R_{DS(on)}*Q_G
- Low Reverse Recovery Charge, Q_{rr}
- Soft Reverse Recovery Body Diode
- Enables Highly Efficiency in Synchronous Rectification
- Fast Switching Speed
- 100% UIL Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

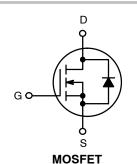
- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Renewable System



ON Semiconductor®

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V _{DSS}	R _{DS(ON)} MAX	I _D MAX
60 V	$3.5~\mathrm{m}\Omega$ @ 10 V	88 A

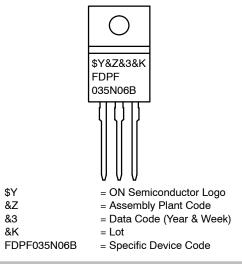






TO-220F Ultra Narrow Lead CASE 221BN

MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{DSS}	Drain to Source Voltage		60	V
V _{GSS}	Gate to Source Voltage		±20	V
I _D	Drain Current	– Continuous ($T_C = 25^{\circ}C$, Silicon Limited)	88	А
		– Continuous ($T_C = 100^{\circ}C$, Silicon Limited)	62	
I _{DM}	Drain Current	– Pulsed (Note 1)	352	А
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		600	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
PD	P _D Power Dissipation	(T _C = 25°C)	46.3	W
	– Derate Above 25°C	0.31	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		–55 to +175	°C
ΤL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. L = 3 mH, I_{AS} = 20 A, starting T_J = 25°C. 3. I_{SD} \leq 100 A, di/dt \leq 200 A/µs, V_{DD} \leq BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Symbol Parameter		Unit
$R_{\theta JC}$	R _{0JC} Thermal Resistance, Junction to Case, Max.		°C/W
$R_{ hetaJA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	°C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Shipping
FDPF035N06B-F154	FDPF035N06B	TO-220F (Pb-Free)	50 Units / Tube

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
FF CHARACT	ERISTICS	·				
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \ \mu A, V_{GS} = 0 \ V$	60	-	_	V
$\Delta \text{BV}_{\text{DSS}} / \Delta \text{T}_{\text{J}}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	-	0.03	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 48 V, V_{GS} = 0 V	-	-	1	μA
I _{GSS}	Gate to Body Leakage Current	V_{GS} = ± 20 V, V_{DS} = 0 V	-	-	±100	nA
N CHARACTE	RISTICS					
V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \ \mu A$	2	-	4	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 88 A	-	2.91	3.5	mΩ
9fs	Forward Transconductance	V _{DS} = 20 V, I _D = 88 A	-	176	_	S
YNAMIC CHA	RACTERISTICS	•				
C _{iss}	Input Capacitance	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	6035	8030	pF
Coss	Output Capacitance		-	1685	2240	pF
C _{rss}	Reverse Transfer Capacitance		-	55	_	pF
C _{oss(er)}	Energy Related Output Capacitance	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	2619	-	
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 30 V, I _D = 100 A, V _{GS} = 10 V (Note 4)	-	76	99	nC
Q _{gs}	Gate to Source Gate Charge		-	29	_	nC
Q _{gd}	Gate to Drain "Miller" Charge		-	12	_	nC
V _{plateau}	Gate Plateau Voltage		-	5.2	_	V
Q _{sync}	Total Gate Charge Sync.	V _{DS} = 0 V, I _D = 50 A	-	67.3	_	nC
Q _{oss}	Output Charge	$V_{DS} = 30 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	92.4	_	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	2.0	_	Ω
WITCHING CH	IARACTERISTICS	·				
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 30 \text{ V}, \text{ I}_{D} = 100 \text{ A}, \text{ V}_{GS} = 10 \text{ V},$	-	32	74	ns
t _r	Turn-On Rise Time	$R_g = 4.7 \Omega$ (Note 4)	-	33	76	ns
t _{d(off)}	Turn-Off Delay Time		-	56	122	ns
t _f	Turn-Off Fall Time		-	23	56	ns
RAIN-SOURC	E DIODE CHARACTERISTICS	•	•	•	•	•
I _S	Maximum Continuous Source to Drain Diode Forward Current		-	-	88	Α
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current		-	-	352	Α
V _{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0 V, I_{SD} = 88 A$	-	-	1.25	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 100 A,	-	71	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100 A/µs	-	78	_	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

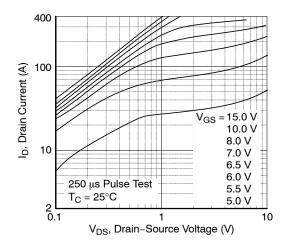
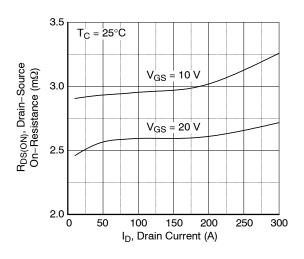
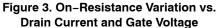


Figure 1. On-Region Characteristics





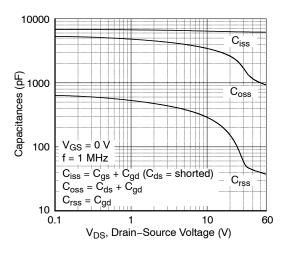


Figure 5. Capacitance Characteristics

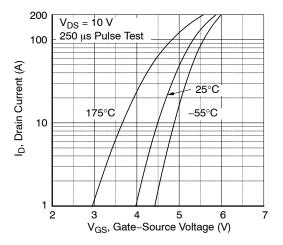


Figure 2. Transfer Characteristics

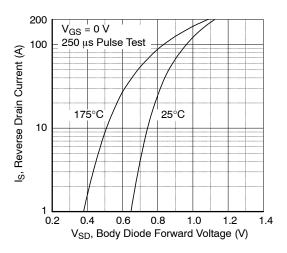


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

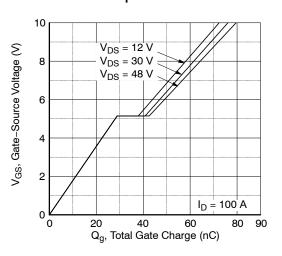
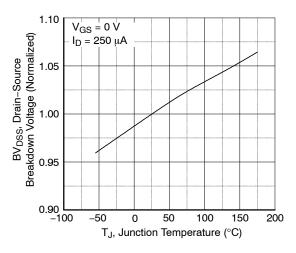
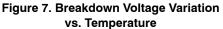


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)





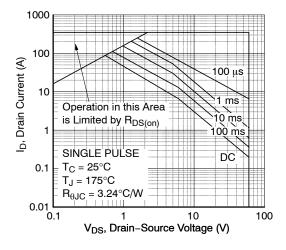


Figure 9. Maximum Safe Operating Area

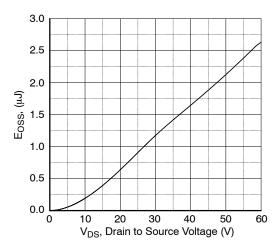


Figure 11. E_{OSS} vs. Drain to Source Voltage

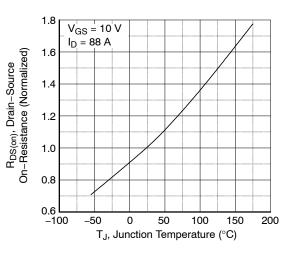


Figure 8. On–Resistance Variation vs. Temperature

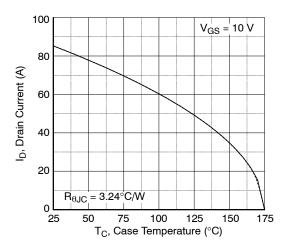


Figure 10. Maximum Drain Current vs. Case Temperature

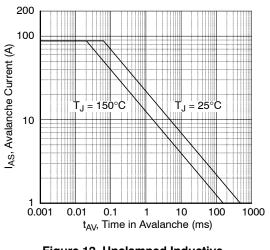


Figure 12. Unclamped Inductive Switching Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

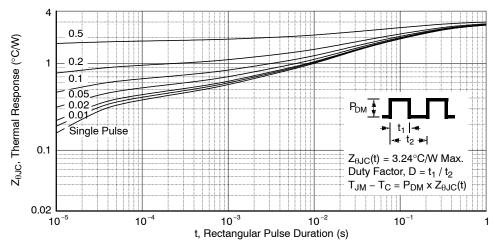


Figure 13. Transient Thermal Response Curve

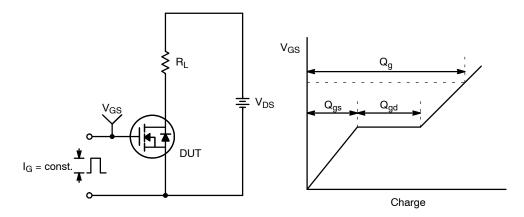


Figure 14. Gate Charge Test Circuit & Waveform

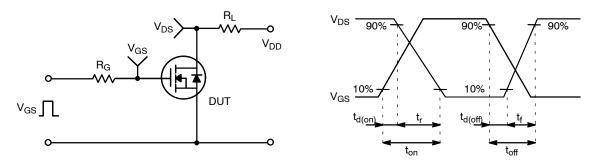


Figure 15. Resistive Switching Test Circuit & Waveforms

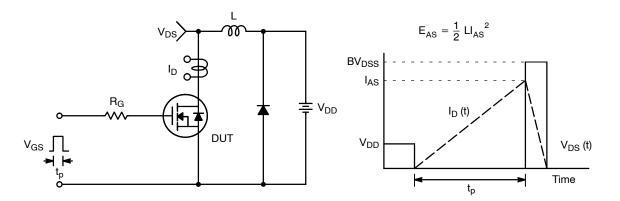


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

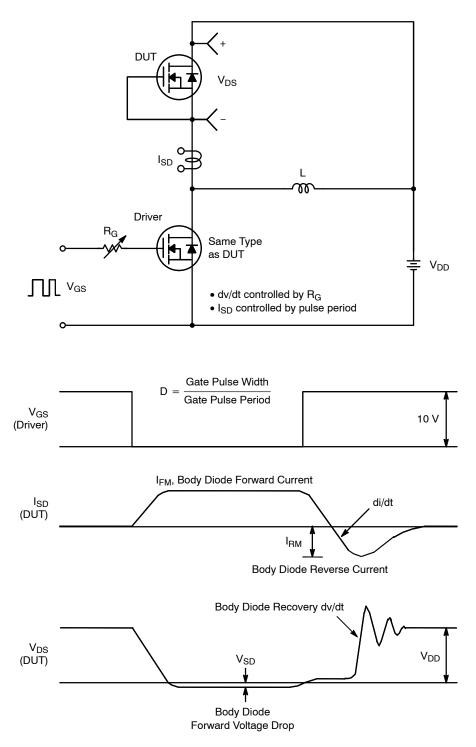


Figure 17. Peak Recovery dv/dt Test Circuit & Waveforms

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



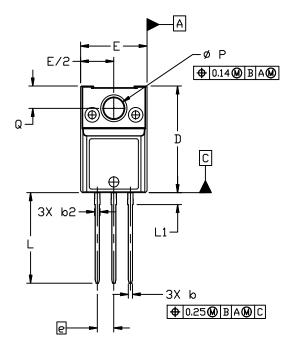
TO-220 FULLPACK, 3-LEAD (ULTRA NARROW LEAD)

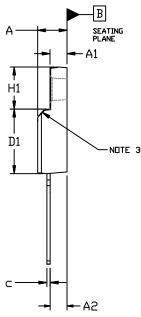
CASE 221BN ISSUE A

DATE 07 MAY 2021

NDTES

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. CONTOUR UNCONTROLLED IN THIS AREA.
- 4. DIMENSIONS EXCLUDE BURRS, MOLD FLASH, AND TIE BAR PROTRUSIONS.





	MILLIMETERS			
DIM	MIN.	NDM.	MAX.	
Α	4.60	4.70	4.80	
A1	2.50	2.60	2.70	
A2	2.47	2.57	2.67	
b	0.56	0.63	0.69	
b2			0.90	
с	0.46	0.53	0.59	
D	15.80	16.00	16.20	
D1	9.58	9.68	9.78	
Е	10.00	10.20	10.40	
е		2.54 BSC		
H1	6.32 REF			
L	13.45	13.60	13.75	
L1	1.70	1.80	1.90	
Р	3.00	3.10	3.20	
Q	3.25	3.35	3.45	



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DESCRIPTION:	TO-220 FULLPACK, 3-LEAD (ULTRA NARROW LEAD) PAGE 1 OF				
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