

STF12NK65Z

N-channel 650 V, 0.6 Ω typ., 10 A SuperMESH™ Power MOSFET in a TO-220FP package

Datasheet - production data

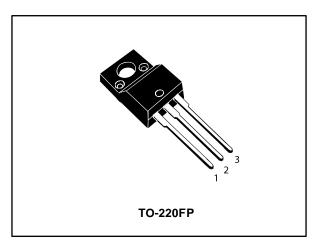
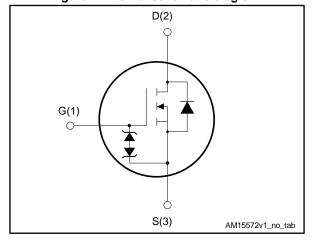


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	lο	Ртот
STF12NK65Z	650 V	0.7 Ω	10 A	35 W

- Extremely high dv/dt capability
- 100% avalanche tested
- · Gate charge minimized
- Zener-protected

Applications

Switching applications

Description

This high voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF12NK65Z	12NK65Z	TO-220FP	Tube

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STF12NK65Z Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	650	V
V_{GS}	V _{GS} Gate-source voltage		V
ΙD	I _D Drain current (continuous) at T _C = 25 °C		Α
ΙD	I _D Drain current (continuous) at T _C = 100 °C		Α
I _{DM} ⁽¹⁾	$\begin{split} & I_{DM}{}^{(1)} & \text{Drain current (pulsed)} \\ & P_{TOT} & \text{Total dissipation at } T_C = 25 ^{\circ}\text{C} \\ & V_{ISO} & \text{Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 ^{\circ}\text{C})} \end{split}$		Α
Ртот			W
V _{ISO}			V
dv/dt ⁽²⁾	t ⁽²⁾ Peak diode recovery voltage slope		V/ns
T _{stg}	Storage temperature range	-55 to 150	°C
Tj	Operation junction temperature range	-55 10 150	C

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	3.6	°C/W
R _{thj-amb}	Thermal resistance junction-ambient		°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	IAR Avalanche current, repetitive or non-repetitive (pulse width limited by T _{JMAX})		А
E _{AS} Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)		225	mJ

⁽¹⁾Pulse width limited by safe operating area

 $^{^{(2)}}I_{SD} \leq 10~A,~di/dt \leq 200~A/\mu s,~V_{DD} \leq V_{(BR)DSS},~T_{j} \leq T_{JMAX}$

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 5: On /off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	650			V
	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 650 \text{ V}$			1	μΑ
I _{DSS}		$V_{GS} = 0 \text{ V}, V_{DS} = 650 \text{ V},$ $T_{C} = 125 \text{ °C}^{(1)}$			50	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±10	μΑ
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100 \mu A$	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on- resistance	V _{GS} = 10 V, I _D = 10 A		0.6	0.7	Ω

Notes:

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
Ciss	Input capacitance		1	1837	-	pF
Coss	Output capacitance	V _{GS} = 0 V, V _{DS} = 25 V, f = 1 MHz	-	208	-	pF
C _{rss}	Reverse transfer capacitance		-	48.8	-	pF
Coss eq ⁽¹⁾	Equivalent output capacitance	V _{GS} = 0 V, V _{DS} = 0 to 520 V	-	122	-	pF
Qg	Total gate charge	V _{DD} = 520 V, I _D = 10 A,	ı	62.6	1	nC
Q_{gs}	Gate-source charge	V _{GS} = 0 to 10 V (see Figure 15: "Test circuit for gate charge behavior")	-	9.6	-	nC
Q_{gd}	Gate-drain charge		-	36	-	nC
Rg	Intrinsic gate resistance	$f = 1 \text{ MHz}, I_D = 0 \text{ A}$	-	1	-	Ω

Notes:

 $^{^{(1)}}$ Defined by design, not subject to production test.

 $^{^{(1)}}C_{oss\;eq}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80%

Table 7: Switchir	na times
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Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 325 \text{ V}, I_D = 5 \text{ A},$	ı	25	-	ns
tr	Rise time	$R_G = 4.7 \Omega, V_{GS} = 10 V$	ı	14	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 14: "Test circuit for resistive load switching times"	-	55	-	ns
t _f	Fall time	and Figure 19: "Switching time waveform")	-	11.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		10	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		1		40	А
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 10 A, V _{GS} = 0 V	-		1.6	V
t _{rr}	Reverse recovery time	$I_{SD} = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	436		ns
Qrr	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	3.4		μC
I _{RRM}	Reverse recovery current	(see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	15.4		А
t _{rr}	Reverse recovery time	$I_{SD} = 10 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s},$	-	518		ns
Qrr	Reverse recovery charge	V _{DD} = 60 V , T _J = 150 °C (see Figure 16: "Test circuit for inductive load switching and diode recovery times")	-	4.1		μC
IRRM	Reverse recovery current		-	15.9		А

Notes:

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)GSO} \\$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_{D} = 0 \text{ A}$	30	-	-	V

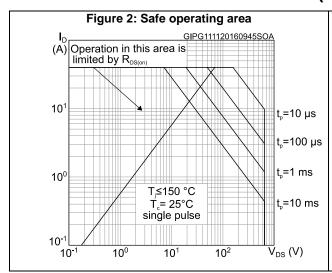
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.



⁽¹⁾Pulsed: pulse duration=300 μs, duty cycle 1.5%.

⁽²⁾Pulse width limited by safe operating area.

2.1 Electrical characteristics (curves)



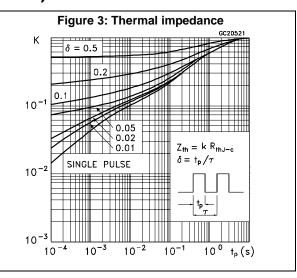


Figure 4: Output characteristics

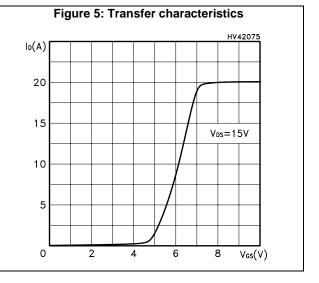
HV42070

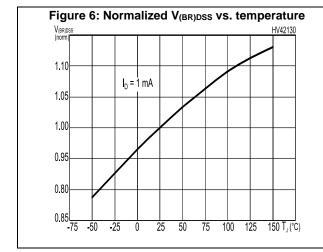
V_{GS} = 10 V

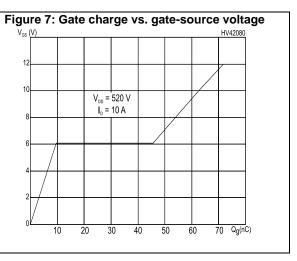
7 V

5 V

0 5 T0 15 20 25 V_{DS} (V)



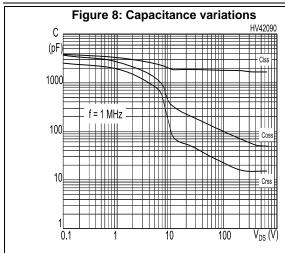




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STF12NK65Z Electrical characteristics



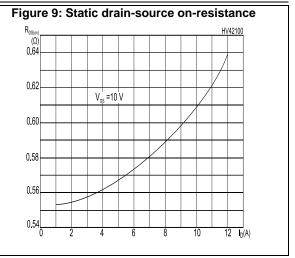
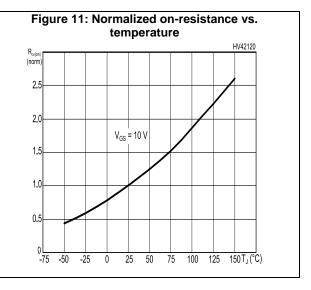
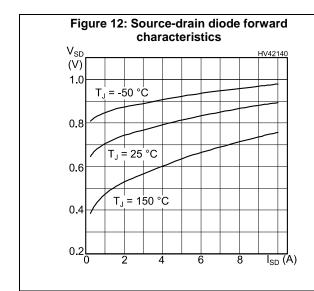
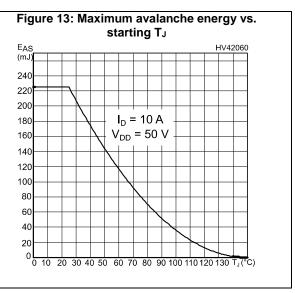


Figure 10: Normalized gate threshold voltage vs. temperature V_{GS}(th) 1.1 1.0 0.9 $I_D = 100 \, \mu A$ 0.8 0.7 0.6 0.5 0 25 50 75 100 125 150 T_J (°C)









Test circuits STF12NK65Z

3 Test circuits

Figure 14: Test circuit for resistive load switching times

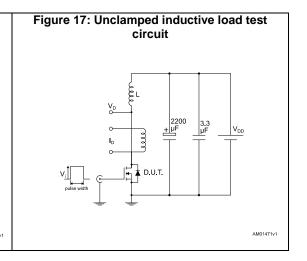
Figure 15: Test circuit for gate charge behavior

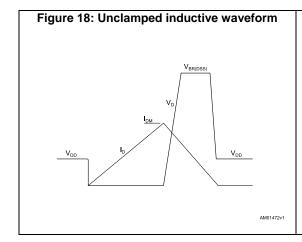
12 V 47 kΩ 100 nF D.U.T.

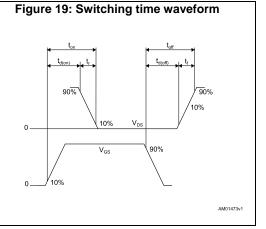
2200 PF 47 kΩ OVG

AM01466y1

Figure 16: Test circuit for inductive load switching and diode recovery times







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STF12NK65Z Package information

4 Package information

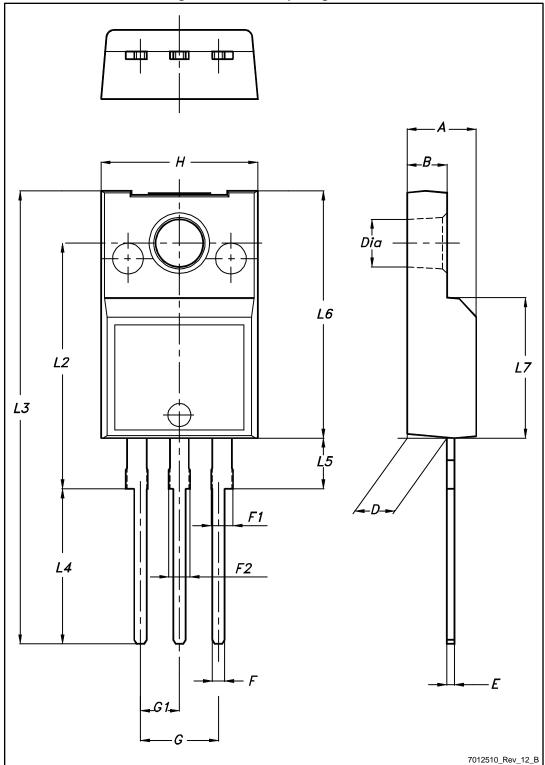
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.



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4.1 TO-220FP package information

Figure 20: TO-220FP package outline



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Table 10: TO-220FP package mechanical data

Table 10. 10 Zzor Package modification and				
Dim.	mm			
	Min.	Тур.	Max.	
A	4.4		4.6	
В	2.5		2.7	
D	2.5		2.75	
Е	0.45		0.7	
F	0.75		1	
F1	1.15		1.70	
F2	1.15		1.70	
G	4.95		5.2	
G1	2.4		2.7	
Н	10		10.4	
L2		16		
L3	28.6		30.6	
L4	9.8		10.6	
L5	2.9		3.6	
L6	15.9		16.4	
L7	9		9.3	
Dia	3		3.2	

Revision history STF12NK65Z

5 Revision history

Table 11: Document revision history

Date	Revision	Changes	
01-Oct-2010	1	Initial release.	
10-Nov-2016	2	Modified title, features and description in cover page Modified Table 2: "Absolute maximum ratings", Table 3: "Thermal data", Table 5: "On /off states", Table 6: "Dynamic", Table 8: "Source drain diode", Table 9: "Gate-source Zener diode" Modified Figure 2: "Safe operating area" Updated Section 4.1: "TO-220FP package information" Minor text changes	
05-Apr-2017	3	Datasheet status promoted from preliminary to production data. Updated Section 2.1: "Electrical characteristics (curves)". Minor text changes	

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