

N-channel 30 V, 2.15 m Ω typ., 120 A Power MOSFET in a TO-220 package

Datasheet - production data

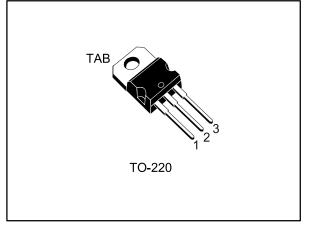
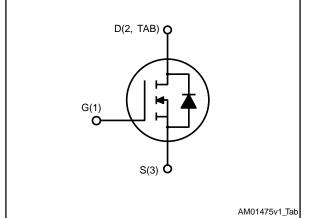


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	ID	Ρτοτ
STP200N3LL	30 V	2.4 mΩ	120 A	176.5 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

• Switching applications

Description

This device is an N-channel Power MOSFET with very low $R_{\text{DS(on)}}$ in all packages.

Table 1: Device summary

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Order code	Marking	Package	Packing	
STP200N3LL	200N3LL	TO-220	Tube	

DocID028758 Rev 2

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This is information on a product in full production.

Contents

Contents

1	Electric	al ratings	3
2	Electric	al characteristics	4
	2.1	Electrical characteristics (curves)	6
3	Test cir	cuits	8
4	Packag	e information	9
	4.1	TO-220 type A package information	10
5	Revisio	on history	12



1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
Vds	Drain-source voltage	30	V
V _{GS}	Gate-source voltage	±20	v
ID	Drain current (continuous) at T _{case} = 25 °C (silicon limited)	200	
ID ⁽¹⁾	Drain current (continuous) at T _{case} = 25 °C	120	٨
ID	Drain current (continuous) at T _{case} = 100 °C	120	A
I _{DM} ⁽²⁾	Drain current (pulsed)	480	
Ртот	Total dissipation at $T_{case} = 25 \text{ °C}$	176.5	W
E _{AS} ⁽³⁾	Single pulse avalanche energy 300		mJ
T _{stg}	Storage temperature range	55 to 175	°C
Tj	Operating junction temperature range	-55 to 175	

Notes:

⁽¹⁾ Current is limited by package.

 $^{\left(2\right) }$ Pulse width is limited by safe operating area.

 $^{(3)}$ starting T_j = 25 °C, I_D = 68 A

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	0.85	°C/W
R _{thj-amb}	Thermal resistance junction-ambient		C/VV



2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$V_{GS} = 0 V$, $I_D = 1 mA$	30			V
	Zara gata valtaga drain	V_{GS} = 0 V, V_{DS} = 30 V			1	
IDSS	Zero gate voltage drain current	$V_{GS} = 0 V, V_{DS} = 30 V,$ $T_{case} = 125 \ ^{\circ}C^{(1)}$			10	μA
I _{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	1		2.5	V
Back	Static drain-source on-	$V_{GS} = 10 \text{ V}, I_D = 60 \text{ A}$		2.15	2.4	mΩ
R _{DS(on)}	resistance	$V_{GS} = 4.5 \text{ V}, I_D = 60 \text{ A}$		2.5	3.1	11122

Notes:

⁽¹⁾Defined by design, not subject to production test.

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
Ciss	Input capacitance		-	5200	-	
Coss	Output capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V		640	-	pF
Crss	Reverse transfer capacitance			510	-	
Qg	Total gate charge	V _{DD} = 15 V, I _D = 120 A, V _{GS} = 4.5 V (see <i>Figure 14: "Test circuit for gate</i> <i>charge behavior"</i>)		53	-	
Q _{gs}	Gate-source charge			13	-	nC
Q _{gd}	Gate-drain charge			27	-	
Rg	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A, gate DC bias = 0 V, magnitude of alternative signal = 20 mV	-	1.1	-	Ω

Table 5: Dynamic

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 15 \text{ V}, \text{ I}_{D} = 60 \text{ A R}_{G} = 4.7 \Omega,$	-	18	-	
tr	Rise time	$V_{GS} = 13 \text{ V}, \text{ IB} = 60 \text{ A KG} = 4.7 \Omega,$ $V_{GS} = 10 \text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	183	-	
t _{d(off)}	Turn-off delay time		-	90	-	ns
tf	Fall time		-	108	-	

4/13



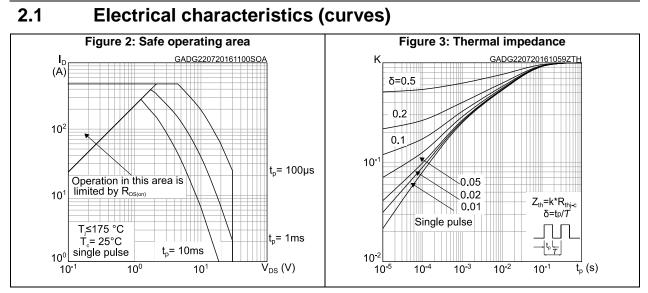
Electrical characteristics

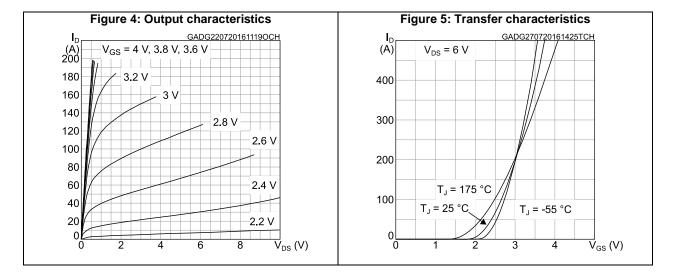
	Table 7: Source-drain diode					
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	$V_{GS} = 0 V, I_{SD} = 60 A$	-		1.1	V
trr	Reverse recovery time	I _{SD} = 120 A, di/dt = 100 A/μs,	-	35		ns
Qrr	Reverse recovery charge	V _{DD} = 24 V (see Figure 15: "Test circuit for inductive load switching	-	34		nC
I _{RRM}	Reverse recovery current	and diode recovery times")	-	2		А

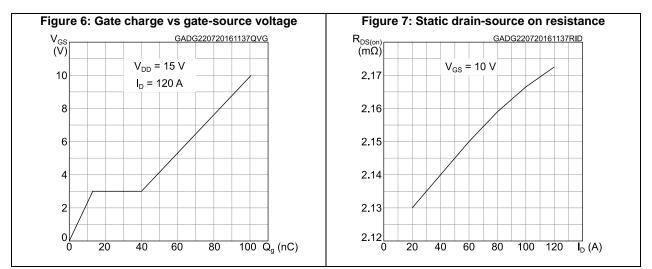
Notes:

 $^{(1)}$ Pulse test: pulse duration = 300 $\mu s,$ duty cycle 1.5%.







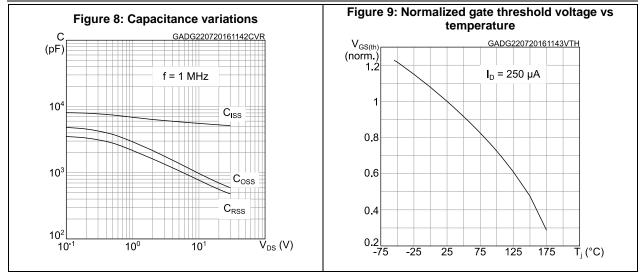


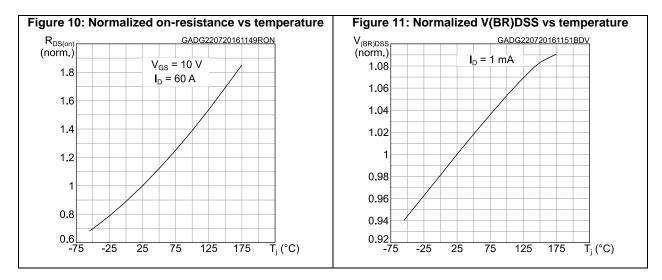
6/13

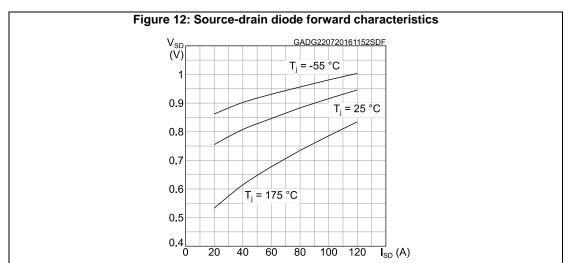
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Electrical characteristics



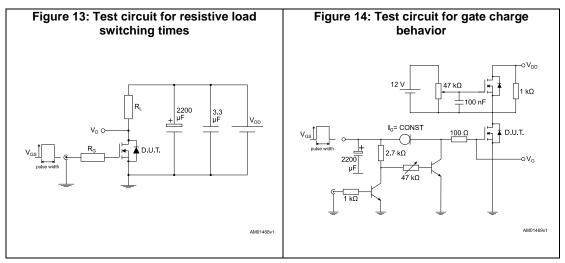


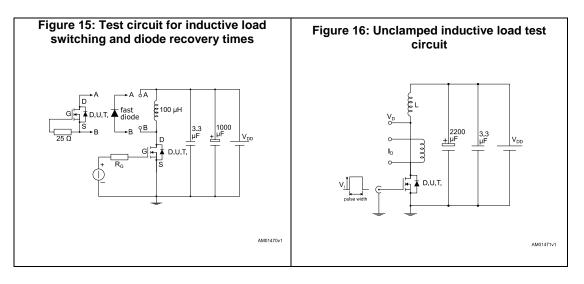


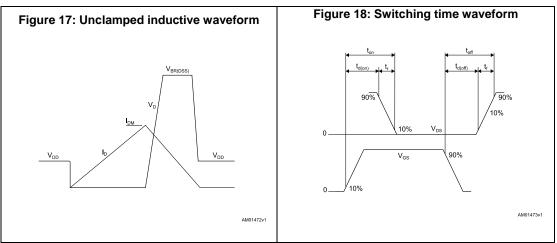
DocID028758 Rev 2

57

3 Test circuits









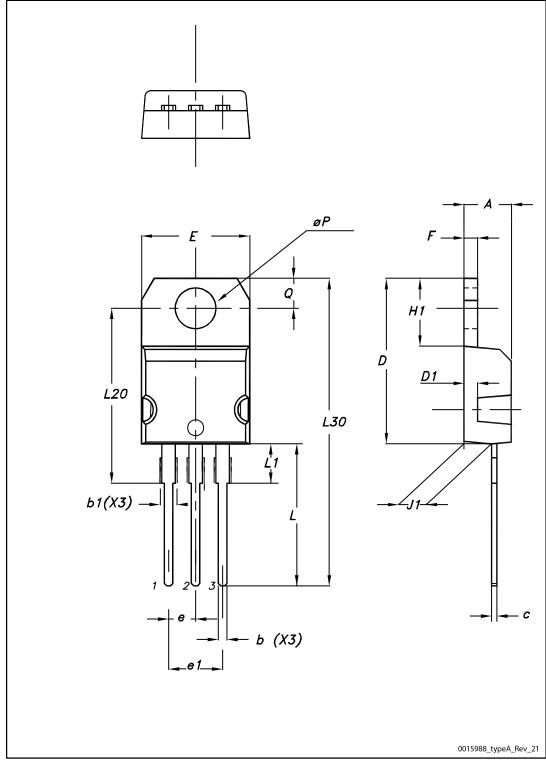
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK[®] is an ST trademark.











Package information

LL			Package information
	Table 8: TO-220 typ	be A mechanical data	
Dim.		mm	
Dim.	Min.	Тур.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
с	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
е	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
			L



5 Revision history

Date	Revision	Changes
14-Dec-2015	1	First release.
27-Jul-2016	2	Document status promoted from preliminary to production data. Updated Section 2: "Electrical ratings" and Section 3: "Electrical characteristics". Added Section 3.1: "Electrical characteristics (curves)". Minor text changes.



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