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ON Semiconductor®

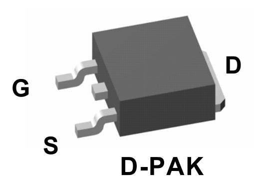
FDD9410L-F085

N-Channel Logic Level PowerTrench® MOSFET

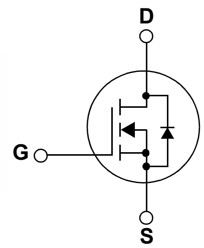
40 V, 50 A, 4.2 mΩ

Features

- Typical $R_{DS(on)}$ = 3.3 mΩ at V_{GS} = 10V, I_D = 50 A
- Typical $Q_{g(tot)}$ = 29 nC at V_{GS} = 10V, I_D = 50 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101



D-PAK
(TO-252)



Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Electronic Steering
- Integrated Starter/Alternator
- Distributed Power Architectures and VRM
- Primary Switch for 12V Systems

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-to-Source Voltage		40	V
V_{GS}	Gate-to-Source Voltage		±20	V
I_D	Drain Current - Continuous (V_{GS}=10) (Note 1)	T_C = 25°C	50	A
	Pulsed Drain Current	T_C = 25°C	See Figure 4	
E_{AS}	Single Pulse Avalanche Energy	(Note 2)	24	mJ
P_D	Power Dissipation		75	W
	Derate Above 25°C		0.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature		-55 to + 175	°C
$R_{\theta JC}$	Thermal Resistance, Junction to Case		2	°C/W
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient	(Note 3)	52	°C/W

Notes:
1: Current is limited by bondwire configuration.
2: Starting T_J = 25°C, L = 30µH, I_{AS} = 40A, V_{DD} = 40V during inductor charging and V_{DD} = 0V during time in avalanche.
3: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD9410L	FDD9410L-F085	D-PAK(TO-252)	13"	16mm	2500units

Electrical Characteristics T_J = 25°C unless otherwise noted.

Off Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
B_{VDSS}	Drain-to-Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V		40	-	-	V
I_{DSS}	Drain-to-Source Leakage Current	V_{DS}=40V,	T_J = 25°C	-	-	1	μA
		V_{GS} = 0V	T_J = 175°C (Note 4)	-	-	1	mA
I_{GSS}	Gate-to-Source Leakage Current	V_{GS} = ±20V		-	-	±100	nA

On Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA		1.0	1.8	3.0	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 50A, V_{GS}= 4.5V		-	5.0	6.5	mΩ
		I_D = 50A,	T_J = 25°C	-	3.3	4.2	mΩ
		V_{GS}= 10V	T_J = 175°C (Note 4)	-	6.0	7.6	mΩ

Dynamic Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
C_{iss}	Input Capacitance	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz		-	1960	-	pF
C_{oss}	Output Capacitance			-	615	-	pF
C_{rss}	Reverse Transfer Capacitance			-	41	-	pF
R_g	Gate Resistance	f = 1MHz		-	1.9	-	Ω
$Q_{g(ToT)}$	Total Gate Charge	V_{GS} = 0 to 10V	V_{DD} = 32V I_D = 50A	-	29	43	nC
$Q_{g(th)}$	Threshold Gate Charge	V_{GS} = 0 to 2V		-	4	-	nC
Q_{gs}	Gate-to-Source Gate Charge			-	6	-	nC
Q_{gd}	Gate-to-Drain “Miller“ Charge			-	5	-	nC

Switching Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{on}	Turn-On Time	V_{DD} = 20V, I_D = 50A, V_{GS} = 10V, R_{GEN} = 6Ω	-	-	22	ns
$t_{d(on)}$	Turn-On Delay		-	8	-	ns
t_r	Rise Time		-	7	-	ns
$t_{d(off)}$	Turn-Off Delay		-	25	-	ns
t_f	Fall Time		-	5	-	ns
t_{off}	Turn-Off Time		-	-	45	ns

Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Source-to-Drain Diode Voltage	I_{SD} =50A, V_{GS} = 0V	-	-	1.25	V
		I_{SD} = 25A, V_{GS} = 0V	-	-	1.2	V
t_{rr}	Reverse-Recovery Time	I_F = 50A, dI_{SD}/dt = 100A/μs V_{DD} = 32V	-	47	71	ns
Q_{rr}	Reverse-Recovery Charge		-	36	71	nC

Note:

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

Typical Characteristics

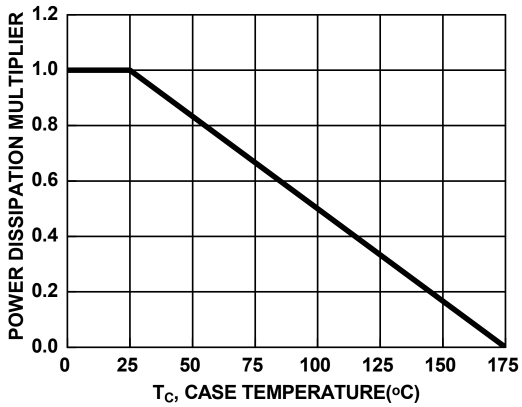


Figure 1. Normalized Power Dissipation vs. Case Temperature

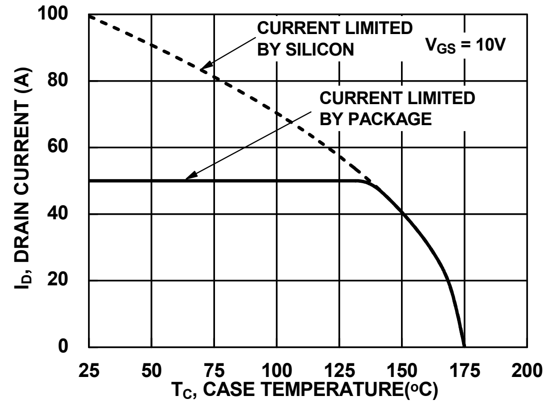


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

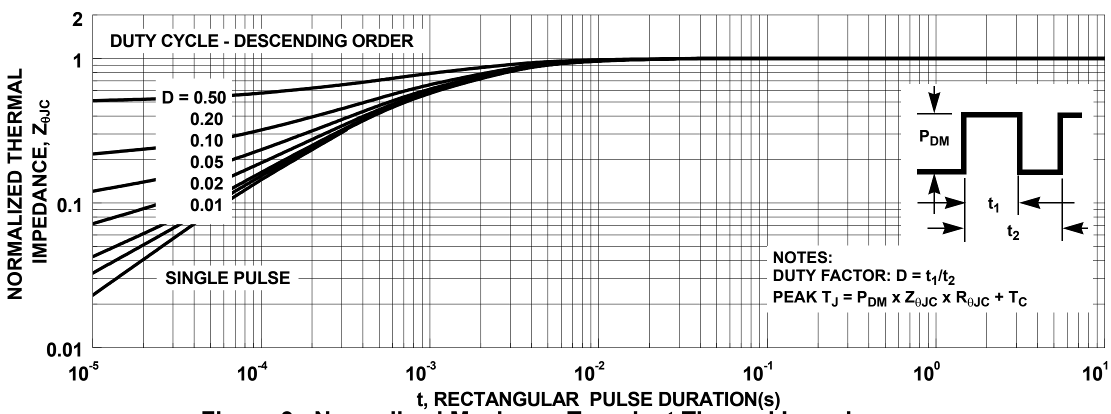


Figure 3. Normalized Maximum Transient Thermal Impedance

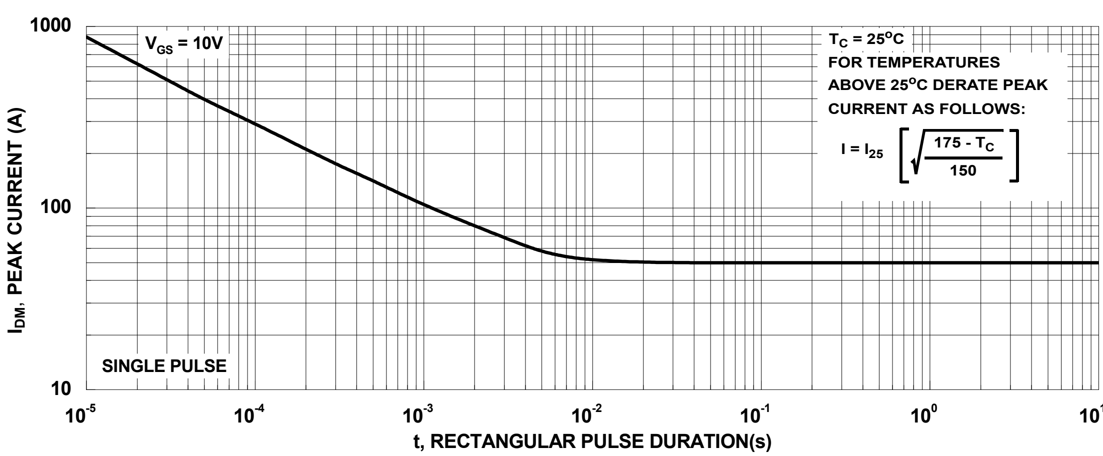


Figure 4. Peak Current Capability

Typical Characteristics

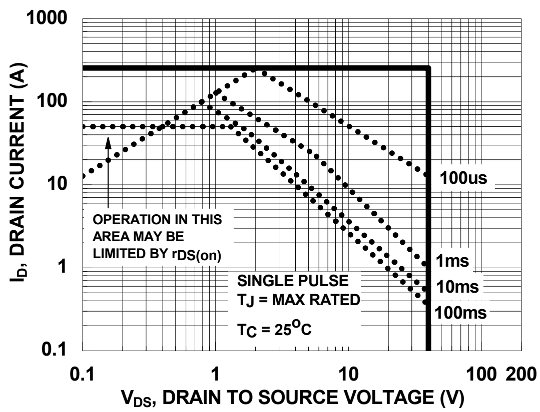
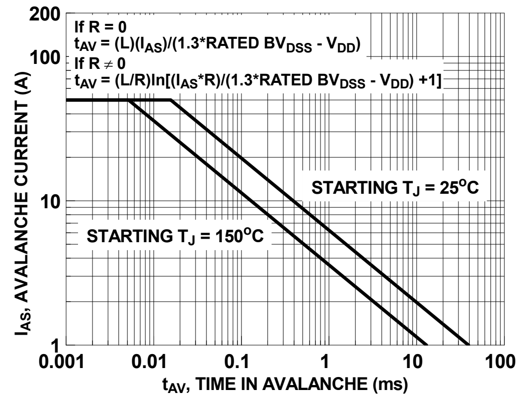


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

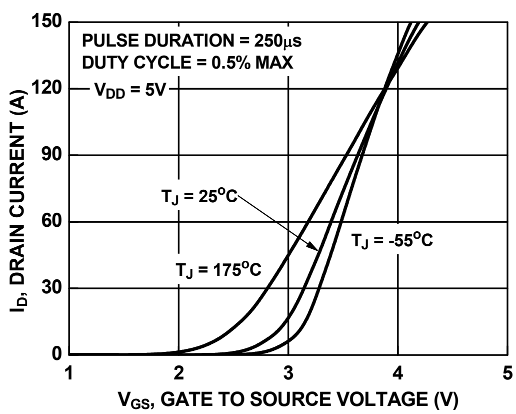


Figure 7. Transfer Characteristics

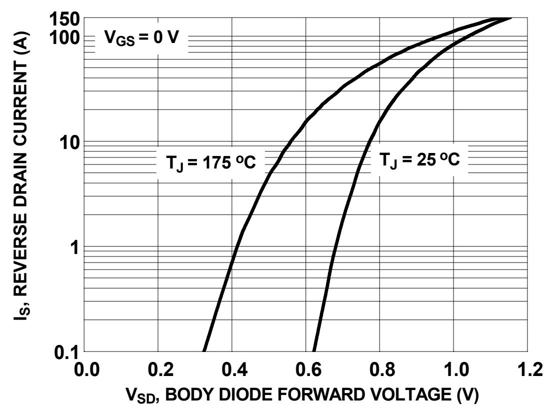


Figure 8. Forward Diode Characteristics

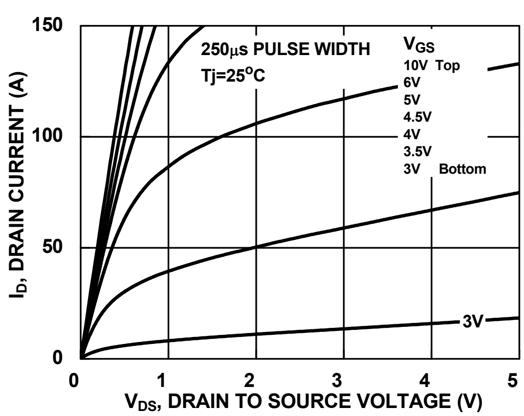


Figure 9. Saturation Characteristics

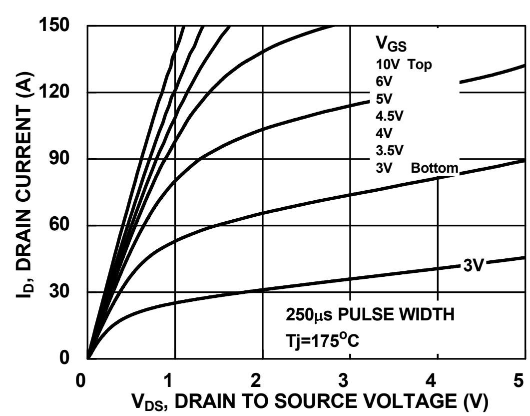


Figure 10. Saturation Characteristics

Typical Characteristics

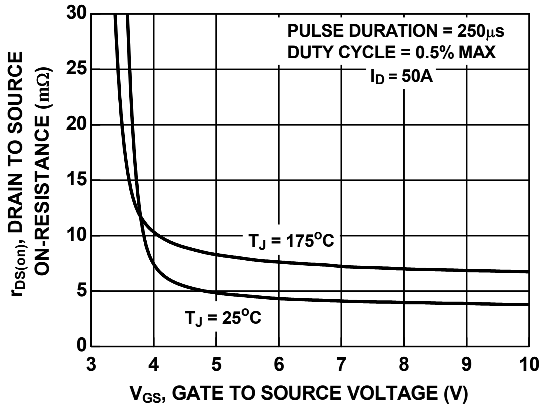


Figure 11. R_{DSON} vs. Gate Voltage

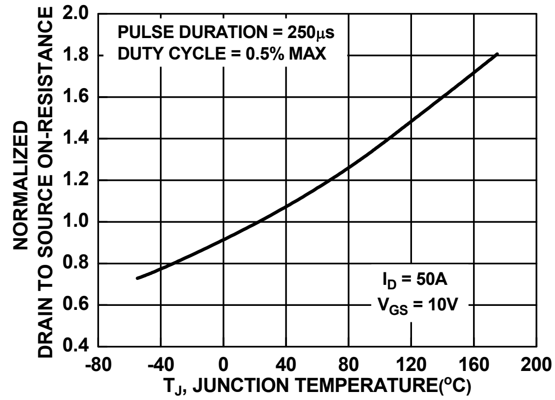


Figure 12. Normalized R_{DSON} vs. Junction Temperature

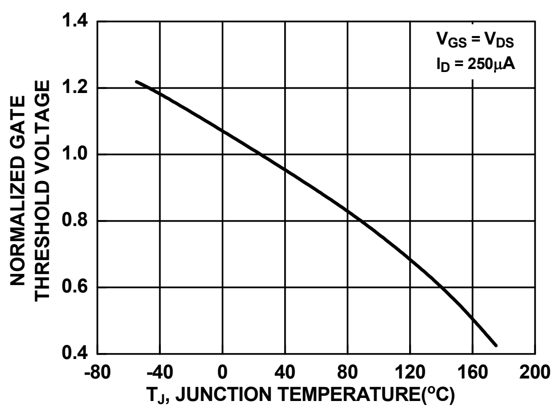


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

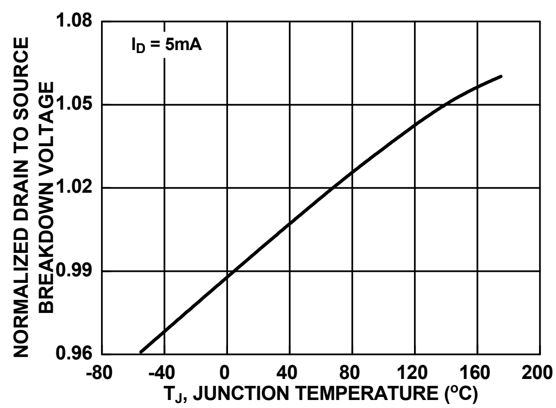


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

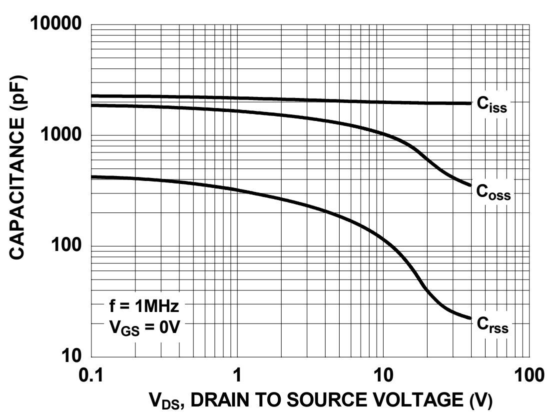


Figure 15. Capacitance vs. Drain to Source Voltage

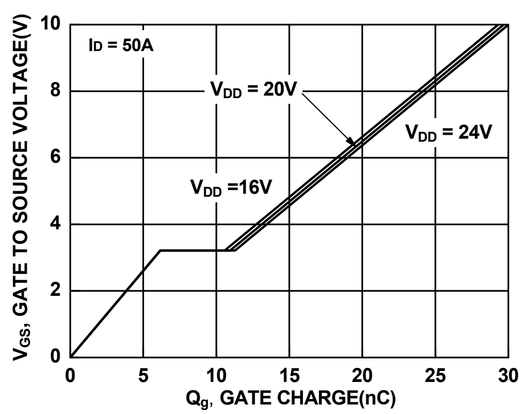


Figure 16. Gate Charge vs. Gate to Source Voltage

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