



STFW3N170, STW3N170

N-channel 1700 V, 8 Ω typ., 2.3 A, PowerMESH™ Power MOSFET
in TO-3FP and TO-247 packages

Datasheet – preliminary data

Features

Order codes	V _{DSS}	R _{DS(on) max}	I _D
STFW3N170	1700 V	12 Ω	2.3 A
STW3N170			

- Intrinsic capacitances and Q_g minimized
- TO-3PF for higher creepage between leads
- High speed switching
- 100% avalanche tested

Applications

- Switching applications

Description

These Power MOSFETs are designed using the company's consolidated strip layout-based MESH OVERLAY™ process. The result is a product that matches or improves on the performance of comparable standard parts from other manufacturers.

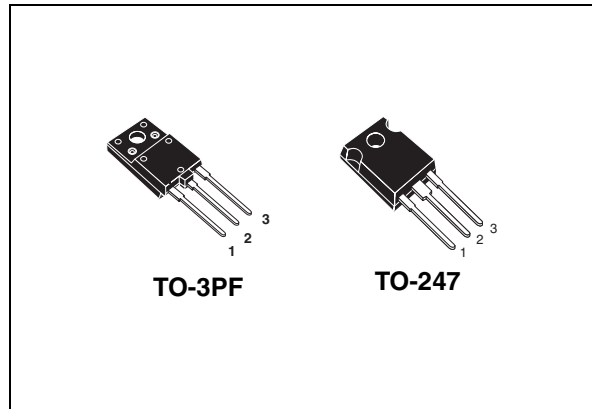


Figure 1. Internal schematic diagram

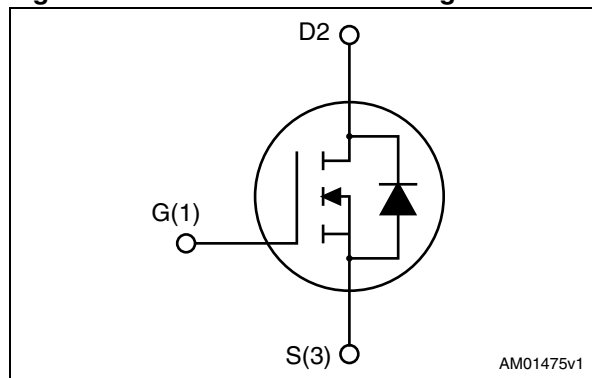


Table 1. Device summary

Order codes	Marking	Package	Packaging
STFW3N170	3N170	TO-3PF	Tube
STW3N170		TO-247	

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-3PF	TO-247	
V_{DS}	Drain-source voltage	1700		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	2.3 ⁽¹⁾	2.3	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	1.45 ⁽¹⁾	1.45	A
I_{DM}	Drain current (pulsed)	9.2 ⁽¹⁾	9.2	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	63	160	W
I_{AR}	Max current during repetitive or single pulse avalanche (pulse width limited by T_{jmax})	TBD		A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	TBD		mJ
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; $T_C = 25\text{ }^\circ\text{C}$)	3500		V
T_{stg}	Storage temperature	-55 to 150		$^\circ\text{C}$
T_j	Max. operating junction temperature			$^\circ\text{C}$

1. Limited by maximum junction temperature

Table 3. Thermal data

Symbol	Parameter	TO-3PF	TO-247	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2	0.78	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-amb max	50		$^\circ\text{C/W}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	1700			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 1700\text{ V}$, $V_{DS} = 1700\text{ V}$, $T_c = 125\text{ °C}$			10 500	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 1.2\text{ A}$		8	12	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1250	-	pF
C_{oss}	Output capacitance			110		pF
C_{rss}	Reverse transfer capacitance			14		pF
R_g	Gate input resistance	$f = 1\text{ MHz}$ Gate DC Bias=0 Test signal level=20 mV open drain	-	TBD	-	Ω
Q_g	Total gate charge	$V_{DD} = 1360\text{ V}$, $I_D = 2.3\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 3)	-	28	-	nC
Q_{gs}	Gate-source charge			TBD		nC
Q_{gd}	Gate-drain charge			TBD		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 850\text{ V}$, $I_D = 1.2\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)	-	TBD	-	ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	$T_J=25\text{ }^\circ\text{C}$	-		2.3	A
I_{SDM}	Source-drain current (pulsed)				9.2	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 2.3\text{ A}, V_{GS}=0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s},$ $V_{DD} = 60\text{ V}$ <i>(see Figure 4)</i>	-	TBD		ns
Q_{rr}	Reverse recovery charge					μC
I_{RRM}	Reverse recovery current					A
t_{rr}	Reverse recovery time	$V_{DD} = 60\text{ V}$ $di/dt = 100\text{ A}/\mu\text{s}, I_{SD} = 2.3\text{ A}$ $T_j = 150\text{ }^\circ\text{C}$ <i>(see Figure 4)</i>	-	TBD		ns
Q_{rr}	Reverse recovery charge					μC
I_{RRM}	Reverse recovery current					A

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

3 Test circuits

Figure 2. Switching times test circuit for resistive load

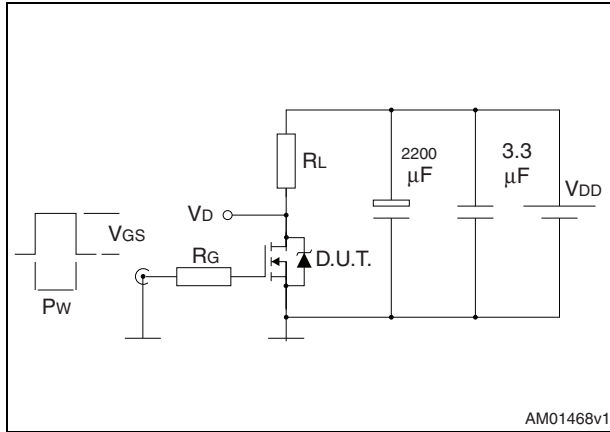


Figure 3. Gate charge test circuit

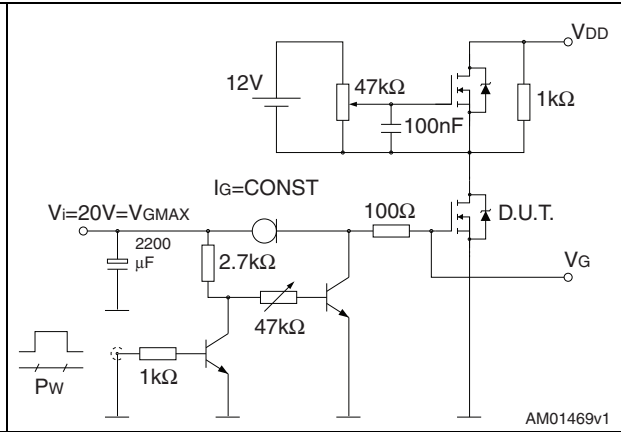


Figure 4. Test circuit for inductive load switching and diode recovery times

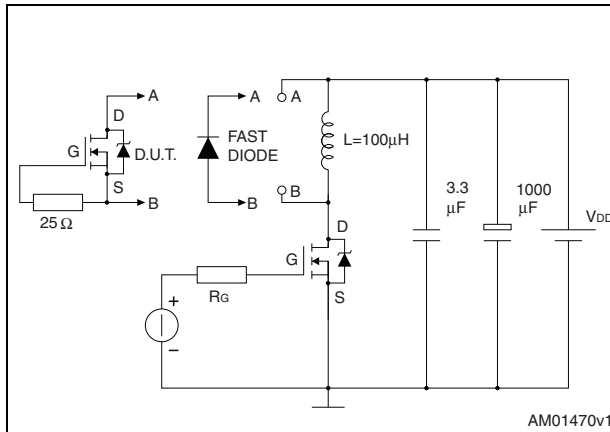


Figure 5. Unclamped inductive load test circuit

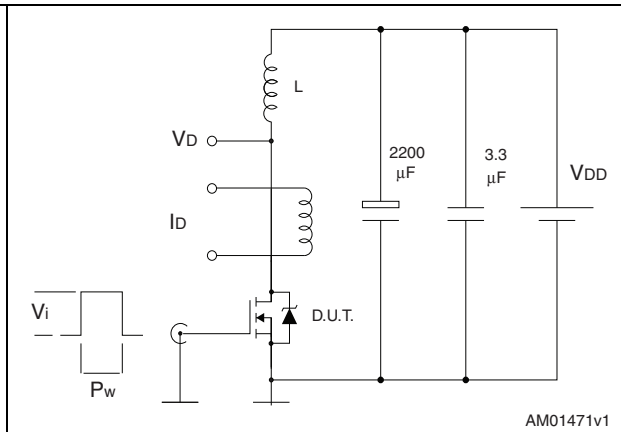


Figure 6. Unclamped inductive waveform

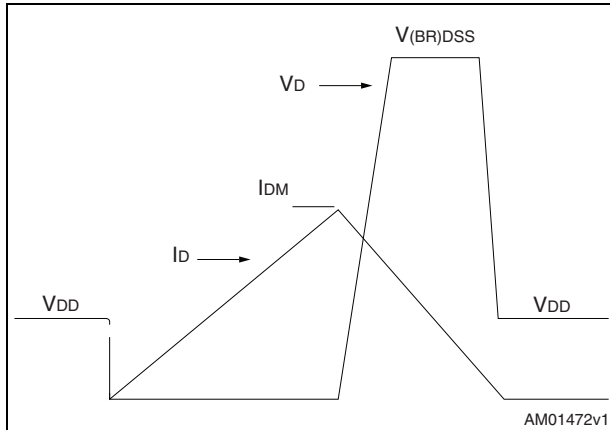
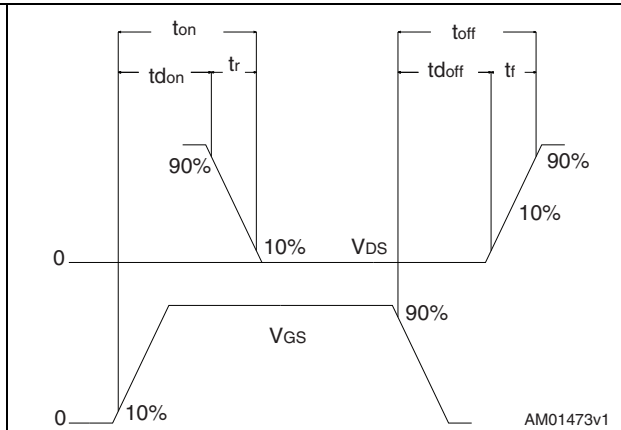


Figure 7. Switching time waveform



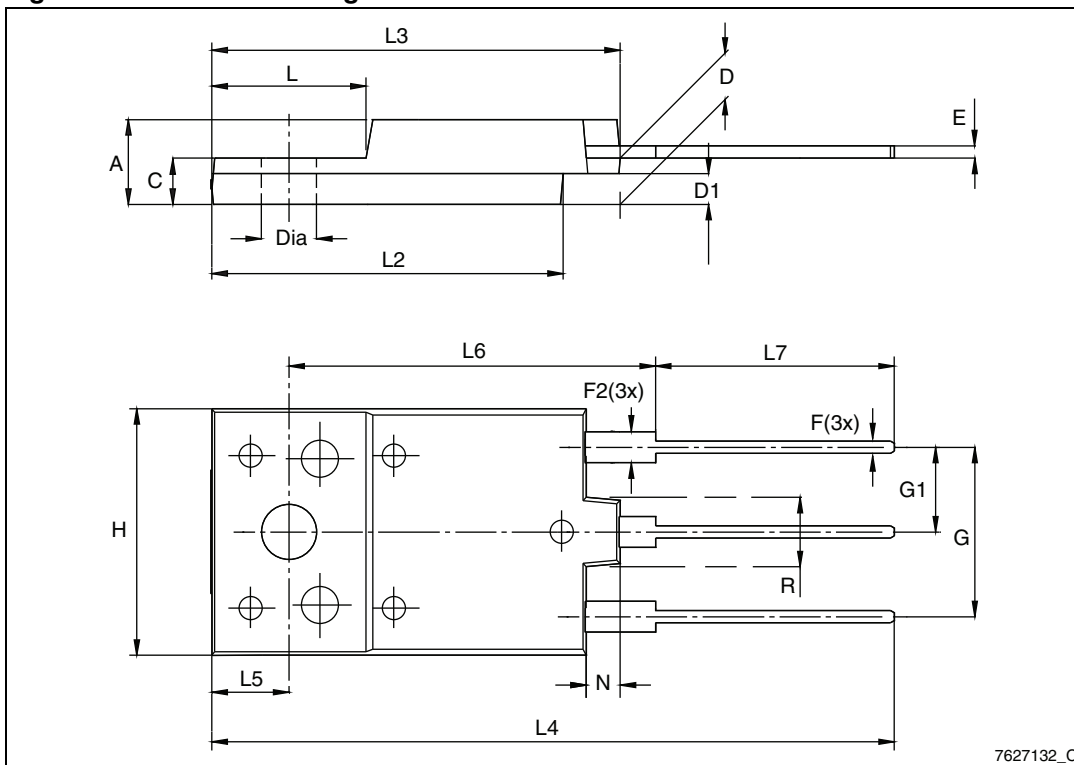
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. TO-3PF mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9.80	10	10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

Figure 8. TO-3PF drawing

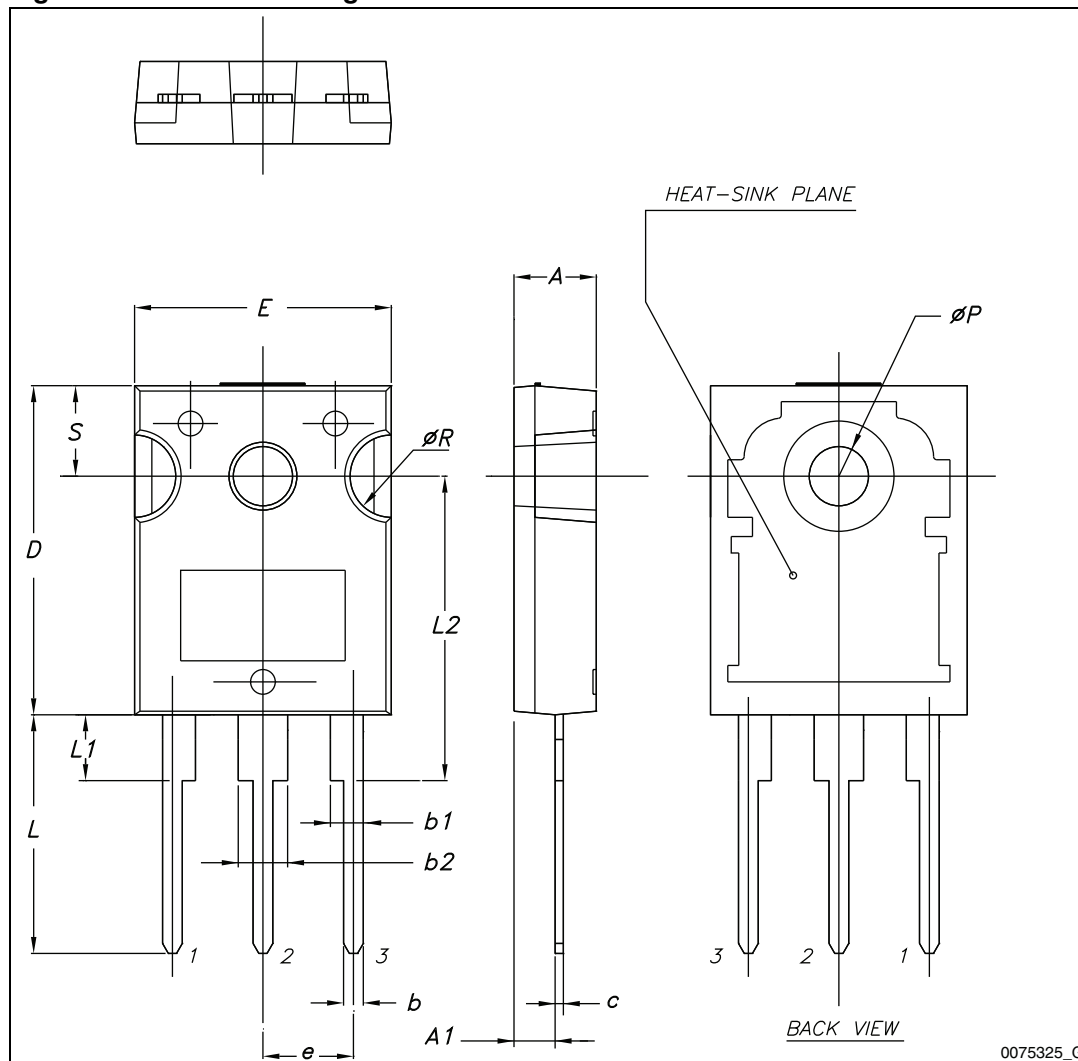


7627132_C

Table 9. TO-247 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

Figure 9. TO-247 drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
17-Jan-2013	1	First release

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