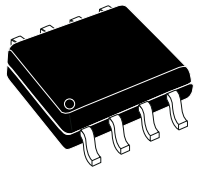
# SRK1001

Datasheet

## Adaptive synchronous rectification controller for flyback converter

SO8 package



| Product status link |
|---|
| SRK1001 |

| Product summary | |
|---|---|
| Order code | SRK1001 |
| Package | SO8 |
| Packing | Tape and reel |

## Features

- Secondary side synchronous rectification controller optimized for flyback converter
- Suitable for QR and mixed CCM/DCM fixed frequency operation
- Wide $V_{CC}$ operating voltage range 3.7 to 32 V
- CC regulation operation down to 2V output supported
- Very low quiescent current in low consumption mode (170 µA)
- High-voltage sensing input for SR MOSFET drain-source voltage (185 V AMR)
- Operating frequency up to 300 kHz
- High-current gate-drive output for N-MOSFET
- Fast turn-on with minimum delay time and adaptive turn-off logic
- Programmable minimum $T_{ON}$ and $T_{OFF}$
- Low consumption mode entry by DIS pin, by primary side burst-mode detection or by detection of SR MOSFET conduction lower than programmed min. $T_{ON}$
- SO8 package

## Applications

- AC-DC adapters
- Battery chargers / quick chargers
- USB power delivery (profile 4)
- Industrial SMPS

## Description

The SRK1001 controller is designed for secondary side synchronous rectification (SR) in flyback converters, suitable for operation in QR and mixed CCM/DCM fixed frequency circuits.

It provides a high-current gate-drive output capable of driving N-channel Power MOSFETs.

The control scheme of this IC is such that the SR MOSFET is switched on as soon as current starts flowing through its body diode, and then switched off as current approaches zero.

The fast turn-on with minimum delay and innovative adaptive turn-off logic allow maximizing the conduction time of the SR MOSFET and eliminating the effect of parasitic inductance in the circuit.

The device enters low consumption mode when it detects primary controller burst-mode operation, or when the DIS pin is pulled up by the user, or when the SR MOSFET conduction falls below the programmed minimum $T_{ON}$. This improves the converter efficiency at light load, where synchronous rectification is no longer beneficial.

After the converter restarts switching or the DIS pin goes low again and the IC detects that the current conduction in the rectifiers has increased 20% above the min $T_{ON}$ programmed value, the IC exits low consumption mode and resumes switching operation.

# 1 Block diagram and pin connection

Figure 1. **Internal block diagram**

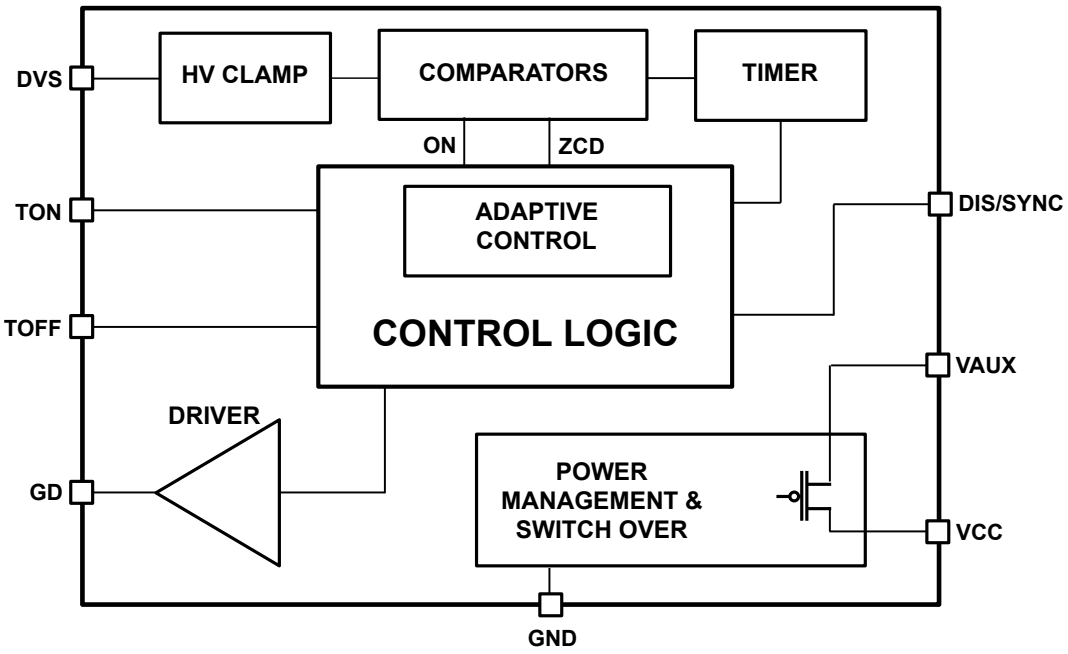
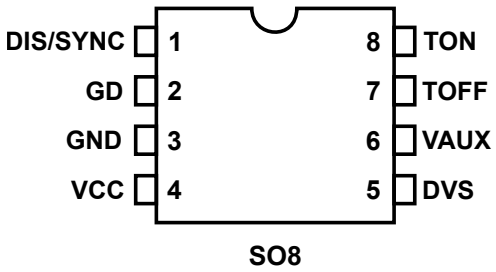



Figure 2. **Pin connections (top view)**




SO8

Table 1. **Pin functions**

| N. | Name | Function |
|---|---|---|
| 1 | DIS/ SYNC | This pin has two functions: disable and synchronization input.<br>• Asynchronous turn-off of SR MOSFET always occurs after DIS pin voltage shows a positive rising edge and the synchronous rectification stays disabled as long as it remains at the high level. If the DIS pin voltage stays high for at least 4 switching cycles, the device enters low consumption mode.<br>• Synchronization function requires that no external capacitor must be mounted between TON pin and GND, so that SR MOSFET turn-off is accomplished by the positive rising edge of the applied SYNC signal or when triggered by ZCD comparator output.<br>This pin is pulled high by internal current source (5 µA); if not used, it must be grounded. |
| 2 | GD | Gate driver output. Totem pole output stage is able to drive power MOSFET with high peak current levels. To avoid excessive gate voltages in case the device is supplied with a high VCC, the high level voltage of this pin is clamped to about 11.5 V. The pin must be connected directly to the SR MOSFET gate terminal. |
| 3 | GND | Return of the device bias current and return of the gate drive current. Route this pin close to the source terminal of synchronous rectifier MOSFET. |

| N. | Name | Function |
|---|---|---|
| 4 | VCC | Supply voltage of the device. A bypass capacitor to GND, located as close to IC pins as possible, helps obtain a clean supply voltage for the internal control circuitry and acts as an effective energy buffer for the pulsed gate drive current. |
| 5 | DVS | Drain voltage sensing. This pin must be connected to the drain terminal of the synchronous rectifier MOSFET through a series resistor of at least 300 Ω. |
| 6 | VAUX | Auxiliary supply voltage of the device. When VCC voltage is lower than UVLO voltage threshold ($V_{CC\_SO\_On}$), the bypass capacitor on the VCC pin (coupled to application VOUT through a diode) is supplied by the VAUX pin if this is connected to an auxiliary winding or to an external capacitor sourced by a DVS voltage rectifier.<br>If the functionality is not used, VAUX pin must be connected to VCC pin. |
| 7 | TOFF | Programming pin for blanking time after turn-off. A resistor connected from this pin to GND, supplied by an internal current source, sets a voltage $V_{TOFF}$; depending on this voltage level, the user can choose the blanking time after turn-off suitable for application requirements. |
| 8 | TON | Programming pin for blanking time after turn-on. A resistor connected from this pin to GND, supplied by an internal current source, sets a voltage $V_{TON}$; depending on this voltage level, the user can choose the blanking time after turn-on, suitable to mask ZCD comparator output and avoid premature turn-off due to parasitic voltage oscillation on DVS pin. In tracking with $V_{TON}$, the thresholds to enter/exit automatic sleep mode are derived.<br>A capacitor larger than 60 pF (100 pF typ.) between this pin and GND sets the internal timer mode for SR MOSFET turn-off in mixed CCM/DCM operation. If no capacitor is used, timer mode is set for turn-off in QR or DCM operation. No capacitor is also required when SYNC signal is used for turn-off. |

# 2 Maximum ratings

**Table 2. Absolute maximum ratings**

| Symbol | Pin | Parameter | Value | Unit |
|---|---|---|---|---|
| VCC | 4 | DC supply voltage | -0.3 to 36 | V |
| DVS | 5 | Drain sense voltage referred to GND (with 300 Ω in series to the pin) | -3 to 185 | V |
| VAUX | 6 | Auxiliary DC supply voltage | -0.3 to 185 | V |
| $V_{TOFF}$ | 7 | TOFF pin voltage rating | -0.3 to 3.6 | V |
| $V_{TON}$ | 8 | TON pin voltage rating | -0.3 to 3.6 | V |
| $V_{SYNC/DIS}$ | 1 | DIS/SYNC pin voltage rating | -0.3 to 3.6 | V |

Stressing the device above the rating listed in above table may cause permanent damage to the device. Exposure to absolute maximum rated conditions may affect device reliability.

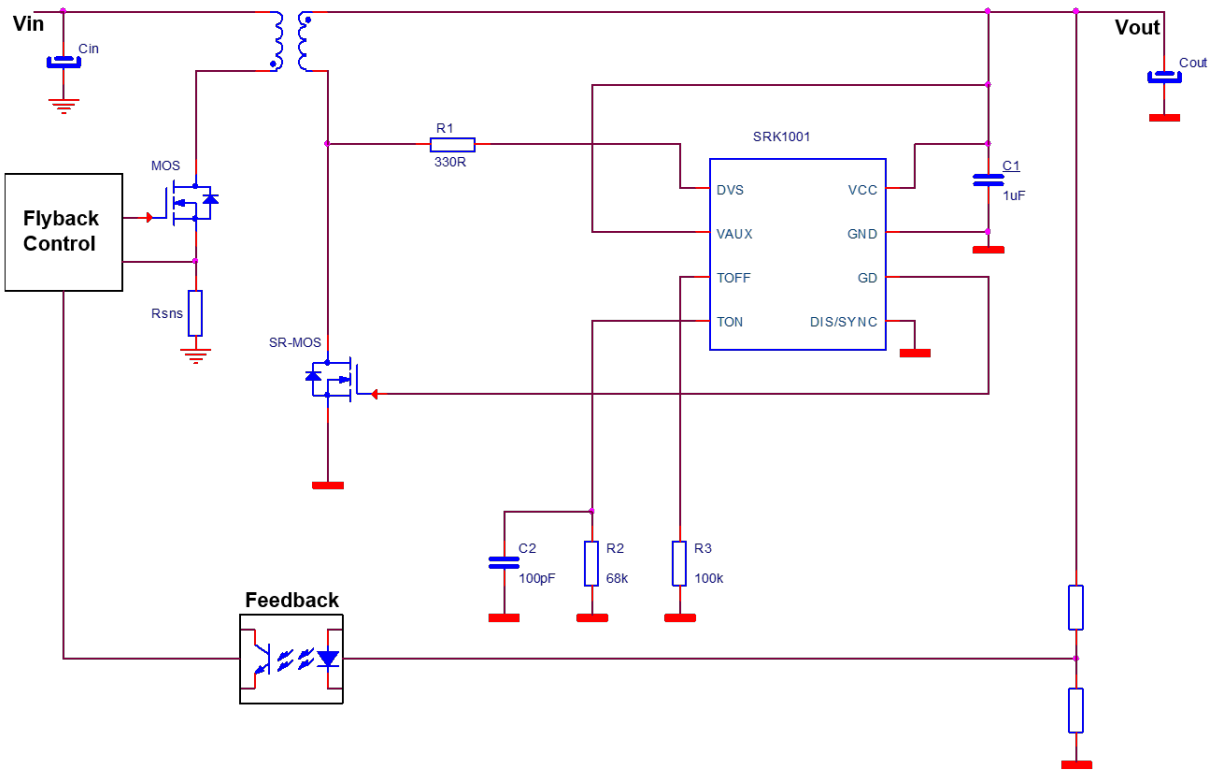
**Table 3. Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\Theta_{th\ j\text{-}amb}$ | Max. thermal resistance, junction-to-ambient(1) | 125 | °C/W |
| $\Psi_{th\ j\text{-}case}$ | Max thermal resistance, junction-to-case top(1) | 5 | °C/W |
| $P_{tot}$ | Power Dissipation @Tamb = 50°C | 0.8 | W |
| $T_j$ | Junction Temperature Operating range | -40 to 150 | °C |
| $T_{stg}$ | Storage Temperature | -55 to 150 | °C |

1. *Natural convection test environment, using JEDEC 1s1p PCB with vias.*

# 3 Typical application schematic

Figure 3. **Typical application schematic**



# 4 Electrical characteristics

$T_j$ = -25°C to 125°C, $V_{CC}$ = 12 V, $C_{GD}$ = 4.7 nF; unless otherwise specified, typical values refer to $T_j$ = 25°C

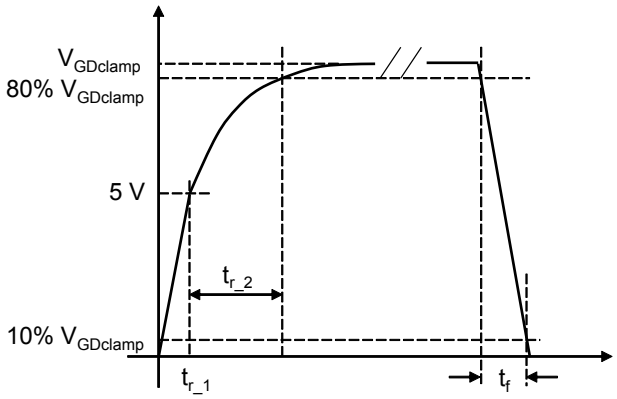
**Table 4. Electrical characteristics**

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply section** | | | | | | |
| $V_{AUX}$ | VAUX pin operating voltage | | | | 185 | V |
| $V_{CC}$ | Operating voltage range | After turn-on | 3.7 | | 32 | V |
| $V_{CC\_On}$ | Turn-on supply voltage | Voltage rising (1) | 4.18 | 4.3 | 4.42 | V |
| $V_{CC\_SO\_On}$ | Turn-on supply voltage for AUX switch activation | Voltage falling (1) | 3.7 | 3.95 | 4.15 | V |
| $V_{CC\_Off}$ | Turn-off supply voltage | Voltage falling (1) | 3.3 | 3.5 | 3.7 | V |
| $V_{CC\_AGD\_en}$ | $V_{CC}$ voltage above which adaptive drive is enabled | On $V_{CC}$ rising edge (2) | | 7.4 | | V |
| $V_{CC\_AGD\_dis}$ | $V_{CC}$ voltage below which adaptive drive is disabled | On $V_{CC}$ falling edge (2) | | 6.5 | | V |
| $I_{q\_run}$ | Current consumption in run mode | After turn-on (excluding SR MOS gate driving) @ 100 kHz | | 600 | | µA |
| $I_{CC}$ | Operating supply current | @ 300 kHz | | 17 | | mA |
| $I_q$ | Quiescent Current | Low consumption mode operation, with DVS pin not switching (3), $T_j$ = -25°C to 85°C | | 170 | 225 | µA |
| $R_{on}$ | VAUX switch resistance | (2) | | 40 | | Ω |
| $I_{DSAT\_VAUX}$ | VAUX pin saturation current | | | 125 | | mA |
| **Drain-source sensing input and synch function** | | | | | | |
| $V_{DS\_H}$ | DVS operating voltage | | | | 185 | V |
| $V_{TH\_A}$ | Cycle comparator threshold | | 70 | 100 | 130 | mV |
| $V_{ZCD\_OFF\_MIN}$ | Minimum ZCD comparator threshold | (2) | | -20 | | mV |
| $T_{diode\_off}$ | Body diode residual conduction time after turn-off | | 230 | 330 | 430 | ns |
| $T_{D\_On\_min}$ | Turn-on delay | | 55 | 85 | 105 | ns |
| $T_{ant\_timer}$ | Anticipation time referred to DVS rising edge to force turn off of SR MOSFET | DVS switching<br>Low level on DVS pin = -1 V | 180 | 280 | 325 | ns |
| $T_{timer\_step}$ | Timer step every 4 switching cycles (in FF operation) | With 100pF on TON pin, during switching period increase | | 56 | | ns |
| $T_{ON\_MAX}$ | Max turn-on duration | | 45 | 60 | 80 | µs |
| **Disable pin remote on/off function** | | | | | | |
| $V_{DIS\_OFF}$ | Disable threshold | For at least 4 cycle to enter in disable state (low consumption mode).<br>Used also as SYNCH input, it always forces a SR MOSFET turn off when pulled high | 1.9 | 2.1 | 2.3 | V |

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DIS\_ON}$ | Enable threshold | | 1.4 | 1.6 | 1.8 | V |
| $I_{DIS}$ | Sourced current | | | 5 | | µA |
| $T_{mask}$ | Sync signal masking time after turn-on | | | 170 | | ns |
| $T_{out}$ | Time-out interval from DVS falling, after which turn-on by sync signal is not allowed | | | 300 | | ns |
| $T_{pulse}$ | Minimum sync pulse width to trigger a turn-off | | 50 | | | ns |
| **Blanking time after turn-on programming** | | | | | | |
| $T_{ON\_MIN}$ | Minimum turn-on time programmable by $R_{TON}$ in the range [33 kΩ - 250 kΩ] | $R_{TON\_MIN}$ = 33 kΩ | 0.28 | 0.4 | 0.52 | µs |
| | | $R_{TON\_MAX}$= 250 kΩ | 2.1 | 3.0 | 3.9 | |
| $I_{TON}$ | Sourced current | In run mode | | 8 | | µA |
| **Blanking time after turn off programming** | | | | | | |
| $T_{OFF\_MIN}$ | Blanking time after turn-off (with DVS voltage continuously above $V_{TH\_A}$) programmable by $R_{TOFF}$ in the range [16 kΩ - 200 kΩ] | $R_{TOFF\_MIN}$ = 16 kΩ | 0.34 | 0.48 | 0.63 | µs |
| | | $R_{TOFF\_MAX}$= 200 kΩ | 4.7 | 6.7 | 8.7 | |
| $I_{TOFF}$ | Sourced current | Run/Sleep Mode | | 10 | | µA |
| **Low consumption mode** | | | | | | |
| $T_{ON\_sleep\_in}$ | Minimum operating current conduction time to enter sleep-mode: $T_{ON\_sleep\_in} = T_{ON\_MIN} + 300$ ns | $R_{TON\_MIN}$ = 33 kΩ | 0.49 | 0.7 | 0.91 | µs |
| | | $R_{TON\_MAX}$= 250 kΩ | 2.31 | 3.3 | 4.29 | |
| $T_{ON\_sleep\_out}$ | Restart current conduction time from sleep-mode: $T_{ON\_sleep\_out} = 1.2*T_{ON\_MIN} + 300$ ns | $R_{TON\_MIN}$ = 33 kΩ | 0.55 | 0.78 | 1 | µs |
| | | $R_{TON\_MAX}$= 250 kΩ | 2.73 | 3.9 | 5.07 | |
| $T_{stop}$ | Switching stop time interval detection to enter low consumption mode (primary controller burst-mode) | | 80 | 120 | 160 | µs |
| **Gate driver** | | | | | | |
| $I_{source\_pk}$ | Output source peak current | See (2) | | 0.6 | | A |
| $I_{sink\_pk}$ | Output sink peak current | See (2) | | 1 | | A |
| $t_{r\_1}$ | Rise Time (see picture below) | $V_{CC}$ = 20V, $C_{GD}$ = 4.7 nF | | 45 | | ns |
| | | $V_{CC}$ = 20V, $C_{GD}$ = 10 nF | | 75 | | |
| $t_{r\_2}$ | Rise Time (see picture below) | $V_{CC}$ = 20V, $C_{GD}$ = 4.7 nF | | 140 | | ns |
| | | $V_{CC}$ = 20V, $C_{GD}$ = 10 nF | | 140 | | |
| $t_f$ | Fall Time (see picture below) | $V_{CC}$ = 20V, $C_{GD}$ = 4.7 nF | | 60 | | ns |
| | | $V_{CC}$ = 20V, $C_{GD}$ = 10 nF | | 120 | | |
| $V_{GDclamp}$ | Drive clamp voltage | $V_{CC}$ = 20V (4) | 10.6 | 11.6 | 12.6 | V |
| $V_{GD\_ad\text{-}step}$ | Adaptive driving step voltage | $V_{CC}$ = 20V (4) | | 400 | | mV |
| $V_{GDL\_UVLO}$ | UVLO saturation | $V_{CC}$ = 0 to $V_{CC\_On}$, $I_{sink}$ = 5 mA | | 1 | 1.3 | V |

1. *Parameters tracking each other*
2. *Parameter guaranteed by design*
3. *Low-consumption-mode is one of the following: sleep-mode for conduction below min TON, converter burst-mode detection or DIS pin pulled high for at least 4 cycles*
4. *Parameters tracking each other*

Figure 4. **Rise and fall time definition**



# 5 Operation description

SRK1001 (see Figure 1. Internal block diagram) controller is specifically designed for synchronous rectification in flyback converters operating in QR and mixed CCM/DCM fixed frequency. This IC turns on the SR MOSFET with a minimum delay when the rectified current starts flowing through the body diode, and turns off the SR MOSFET when current approaches zero, using an adaptive mechanism that leads the body diode residual conduction time after turn-off to the target value $T_{diode\_off}$ (refer to Table 4 for the various parameter values).

The adaptive turn-off method presents certain advantages compared to a standard approach based on a comparator with fixed threshold.

The first advantage is that the adaptive method automatically compensates stray inductances $L_S$ in series to rectified current path: this parasitic (mainly the SR MOSFET package inductances in series to drain and source terminals) normally produces an offset on the sensed voltage across MOSFET $R_{DS\_ON}$ that anticipates by $T_X = L_S/R_{DS\_ON}$ the turn-off in case of standard comparator.

The second aspect to consider is that a standard comparator with fixed threshold turns off at a current level $I_{OFF}$ that depends on $R_{DS\_ON}$ of the chosen SR MOSFET. Referring to Figure 5. Comparison between adaptive turn-off and comparator based turn-off and considering a fixed comparator threshold $V_{TH}$ = -5 mV, the turn-off current in the rectifier can be calculated.

In an application with a SR MOSFET having channel resistance $R_{DS\_ON}$ = 2.5 mΩ and package stray inductance $L_S$ = 2.5 nH, where the current slope is di/dt = -3 A/µs (for example starting from a peak current of 15 A with 5 µs transformer demagnetization), the turn off current is:

- $I_{OFF} = -\frac{V_{TH}}{R_{DS\_ON}} - T_X\frac{di}{dt} = 5A$ for comparator turn-off
- $I_{OFF\_AD} = -T_{diode\_off}^{*}\frac{di}{dt} = 0.9A$ for adaptive turn-off

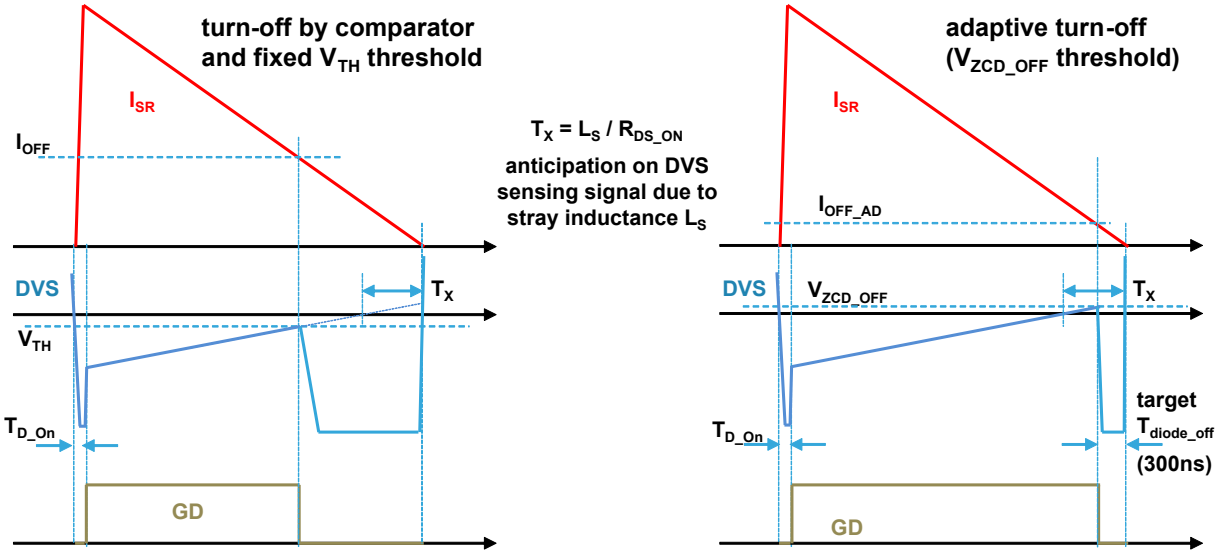
Furthermore, the adaptive turn-off method also performs better in applications with CC regulation, where the standard comparator with fixed threshold increasingly anticipates the turn-off during load impedance drops (since current slope also decreases), while the adaptive method fixes $T_{diode\_off}$.

The SRK1001 controller starts operation when the VCC pin voltage exceeds the turn-on threshold $V_{CC\_On}$; then it stops operation when the $V_{CC}$ voltage drops below the turn-off threshold $V_{CC\_Off}$.

In order to guarantee SR switching even with low $V_{CC}$ supply voltage (in the case of chargers operating in CC regulation), the device is provided with the VAUX pin. When the $V_{CC}$ voltage decreases below the threshold $V_{CC\_SO\_On}$ (> $V_{CC\_Off}$), an internal switch is turned on, allowing VCC pin capacitor to be charged up to the turn-on threshold $V_{CC\_On}$ by a current drawn through VAUX pin connected, for example, to the rectified SR MOSFET drain voltage or to another auxiliary voltage of the flyback transformer.

For maximum flexibility across all kinds of applications and to overcome noise and ringing problems that may arise after turn-on and turn-off events, the SRK1001 allows users to program the blanking time after turn-on and after turn-off by means of two resistors connected between TON and TOFF pins to GND, respectively.

Figure 5. **Comparison between adaptive turn-off and comparator based turn-off**




## 5.1 Drain voltage sensing

The drain voltage of the SR MOSFET is sensed through the DVS pin: this is a high voltage pin and needs to be properly routed to the MOSFET drain, through a resistor of at least 300 Ω (in order to limit dynamic current injection in any condition). The DVS signal is used to detect when current flows through the MOSFET body diode and for the internal timings.

## 5.2 Turn-on

After the flyback converter primary switch has been turned off, the voltage across the transformer reverses and the SR MOSFET drain voltage quickly decreases and goes negative ($-V_F$), allowing the rectifier current to flow. Consequently, triggered on the falling edge of the DVS signal (when it decreases below the arming voltage $V_{TH\_A}$), the controller turns on the SR MOSFET, with a very short delay $T_{D\_On}$. After turn-on, the sensed DVS signal passes from the (negative) body diode forward voltage to the drop across the MOSFET channel resistance ($R_{DS\_ON}$).

This drop is generally affected by some amount of noise, associated with the flyback transformer leakage inductance, and this could trigger a premature turn-off of the SR MOSFET.

## 5.3 Minimum $T_{ON}$ programming

In order to avoid premature turn-off of the SR MOSFET due to ringing and oscillations, the IC allows user to program a blanking time after turn-on. The circuit bases on an internal timing capacitance and an external resistor $R_{TON}$ connected from TON pin to ground. The blanking time settlement is done according to the following expression:

$$T_{ON\_MIN} = 12*10^{-12}*R_{TON}$$

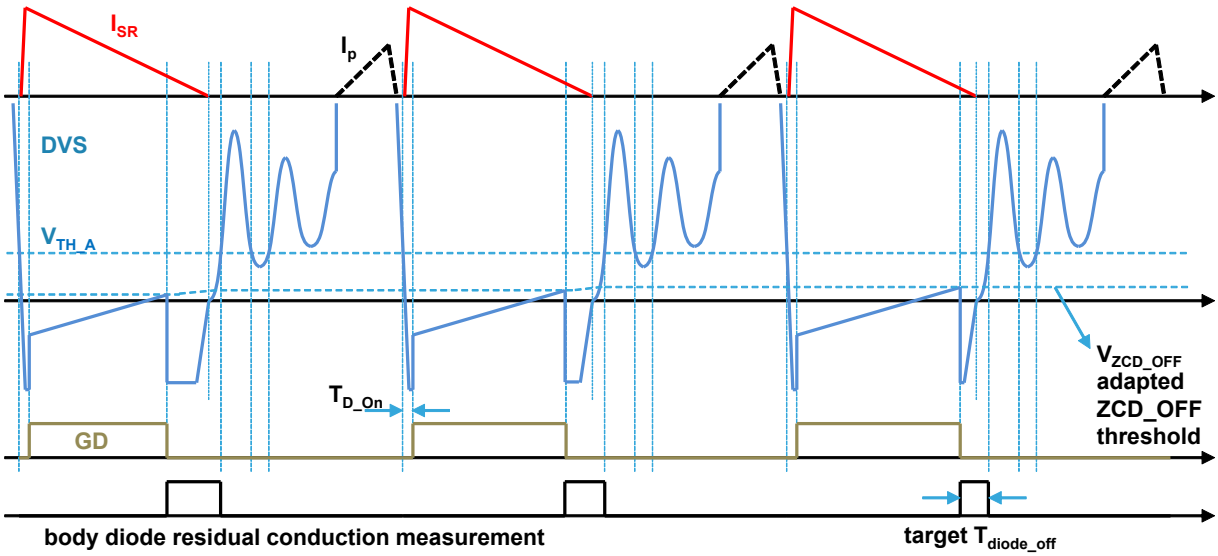
(with $R_{TON}$ expressed in Ohms and $T_{ON\_MIN}$ in seconds, starting from when the DVS signal falls below $V_{TH\_A}$). This blanking time sets a minimum turn-on time of the SR MOSFET as well: hence, when load reduction causes the SR MOSFET conduction time to become shorter than the programmed blanking time, the IC must stop driving the SR MOSFET to avoid current inversion (see Section 5.7 Low consumption mode operation: sleep-mode, burst mode, disable state).

## 5.4 Adaptive turn-off and TIMER

The SR MOSFET can be turned off through two coexisting mechanisms (whichever triggers first), the first based on an adaptive algorithm, the second on the internal timer.

The adaptive turn-off consists of a ZCD_OFF comparator, where the DVS signal is compared to an adapting threshold. This threshold is adapted in such a way that, at steady state, the measured residual conduction time of SR MOSFET body diode after turn-off meets the target value $T_{diode\_off}$ (as shown in Figure 6. ZCD_OFF threshold adapting for target body diode conduction). The residual conduction time of the body diode is measured between the falling edge of the driving signal and the rising edge of the DVS signal (first time exceeding the arming voltage $V_{TH\_A}$).

**Figure 6. ZCD_OFF threshold adapting for target body diode conduction**




The internal timer turns off the SR MOSFET with a fixed anticipation time $T_{ant\_timer}$ with respect to the first rising edge of the DVS signal. The IC has two different user timer operating modes optimized for fixed frequency mixed CCM/DCM converters or for QR/DCM applications. The selection of the proper timer mode is performed through a 100 pF capacitor across the TON pin:

- if capacitor is present, mixed CCM/DCM operation is assumed
- if capacitor is not present, QR/DCM operation is assumed.

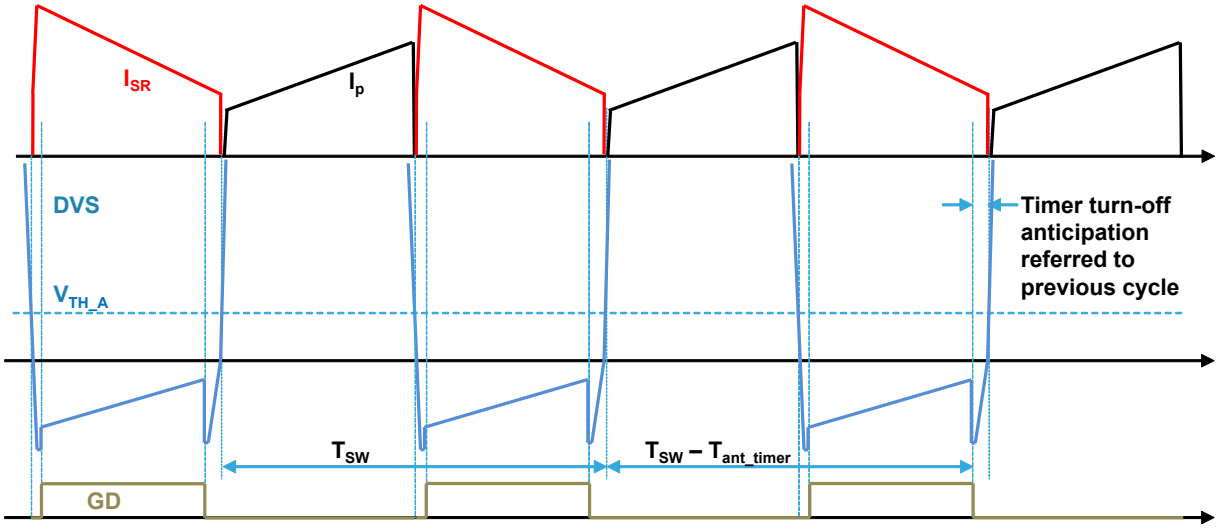
### 5.4.1 Fixed frequency mixed DCM/CCM operation

In fixed frequency operation, SR MOSFET turn-off is triggered by ZCD_OFF adaptive mechanism at load levels where DCM operation occurs, while it is triggered by timer at higher loads where CCM operation occurs. The latter consists of turning off the SR MOSFET with a fixed lead time $T_{ant\_timer}$ with respect to the first rising edge of the DVS signal, based on a switching period $T_{SW}$ estimate, (over a few previous cycles) as illustrated in Figure 7.

Turn-off by the timer may also intervene during low-to-high load transients, where the ZCD_OFF threshold is in the adapting phase (because of the output voltage drop occurring as a consequence of the transient), preventing undesired current inversions.

Most flyback controllers use operating frequency modulation to help optimize the EMI filter. For correct operation of the SRK1000 timer, the maximum rate of change of modulated frequency must be limited, so the switching period increase from the current cycle to the following cycle is much shorter than the timer anticipation $T_{ant\_timer}$ (14 ns maximum). In fact, the timer anticipation adaptation during the switching period increase is limited to $T_{timer\_step}$ every 4 cycles, and with a switching period increase longer than 14 ns from one cycle to the next, the timer turn-off lead time steadily increases (increasing the body diode conduction).

Figure 7. **Timer anticipation for fixed frequency CCM operation (100pF mounted on TON pin)**




### 5.4.2 QR operation (with valley skipping)

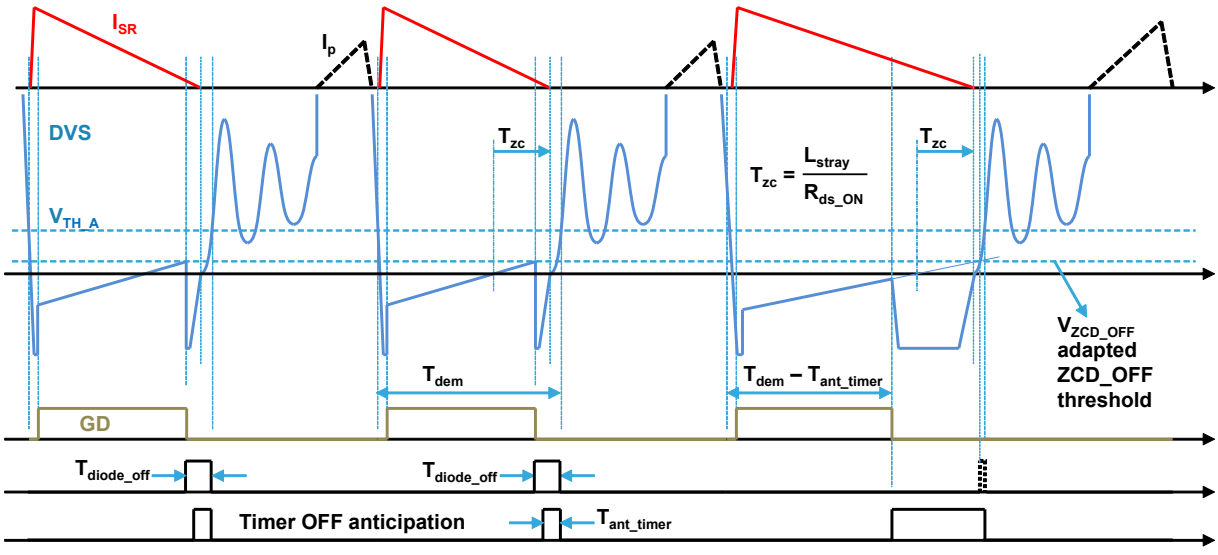
In QR flyback applications, the circuit works at variable frequency and, after transformer demagnetization, a resonance occurs due to primary inductance and total parasitic capacitance across primary switch. In this case, at steady state, SR MOSFET turn-off is triggered by the ZCD_OFF adaptive mechanism.

During load transitions or during CC regulation operation in which output voltage may decrease, turn-off by the adaptive ZCD_OFF comparator would be too late as the threshold needs to adapt to the new slope of the current flowing into the SR MOSFET, while turn-off by internal timer prevents current inversion.

Timer for fixed frequency CCM is not suitable in QR operation, which inherently operates at variable frequency. In this case, the timer operating mode consists of turning off the SR MOSFET with a fixed anticipation time $T_{ant\_timer}$ with respect to the first rising edge of the DVS signal, based on the duration of the previous demagnetization time of transformer $T_{dem}$, as shown in Figure 8.

Looking at Figure 8, during the first two switching cycles (steady state operation), the turn-off is triggered by the ZCD_OFF comparator. This is because the DVS signal reaches the adapted ZCD_OFF threshold before the timer OFF event as the target diode $T_{diode\_off}$ is larger than timer anticipation $T_{ant\_timer}$. In the third switching cycle, as a consequence of the transient, the turn-off is instead triggered by timer, since current slope has decreased and the ZCD_OFF threshold would be reached too late. In the following cycle (not shown in figure), the timer stabilizes the anticipation to the duration of the demagnetization period of the third cycle.

Figure 8. **Timer anticipation for QR operating circuit (no capacitor mounted on TON pin)**



### 5.4.3 Fixed frequency DCM operation

In fixed frequency circuits designed to operate always in DCM in all line and load conditions, the SRK1001 controller operates in a similar way to QR operation: the turn-off is accomplished by adaptive mechanism in steady state operation, while timer turn-off is invoked to protect against current inversion during load transitions and in CC regulation. In this case, the timer mode can be either the one for FF CCM or the one for QR application, which is the cheaper option as no capacitor on TON pin is required.

### 5.4.4 Variable frequency CCM operation

Some advanced flyback controllers provide multimode operation in order to maximize performance and optimize transformer design. Some of these controllers also provide variable frequency CCM operation to facilitate overload management, while helping to reduce the transformer size (on overpower request, the operating frequency is increased). The SRK1001 controller is suitable for operation in these kinds of applications, allowing SR MOSFET turn-off through a synchronization signal (provided from primary side through a pulse transformer) applied to the SYNC pin. Refer to Section 5.7 Low consumption mode operation: sleep-mode, burst mode, disable state for a detailed operation description.

## 5.5 Minimum $T_{OFF}$ programming

In flyback applications operating in DCM and QR with valley skipping, resonance occurs across transformer windings after demagnetization, whose period $T_{RES}$ depends on the transformer primary inductance and on the total capacitance across primary switch. In order to prevent this ringing from affecting the SRK1001 internal timings, a blanking time after turn-off needs to be programmed. The circuit is based on an internal timing capacitance and an external resistor $R_{TOFF}$ connected from TOFF pin to ground and allows fixing a $T_{OFF\_MIN}$ time according to the following expression:

$$T_{OFF\_MIN} = 30{*}10^{-12}{*}R_{TOFF}$$

$R_{TOFF}$ is expressed in Ohms and $T_{OFF\_MIN}$ in seconds. The $T_{OFF\_MIN}$ time must be set slightly longer than the ringing period $T_{RES}$: in this way, referring to Figure 9, the circuit provides a blanking time from the falling edge of the driving signal to the time instant occurring after the DVS pin voltage is permanently higher than $V_{TH\_A}$ for $T_{OFF\_MIN}$.

Furthermore, referring to Figure 10, an internal comparator referenced to a voltage $V_R$ higher than 2 times $V_{OUT}$ senses the DVS pin voltage (where $V_R$ and VDS are conveniently scaled). When VDS voltage rises above $V_R$, the comparator triggers and the blanking time is terminated. This helps during constant voltage regulation operation, at high input voltage levels (where typically the conduction time of the primary MOSFET is short), preventing the blanking time determined by $T_{OFF\_min}$ from delaying the SR MOSFET turn-on. The internal threshold $V_R$ is fixed to 2.83 $V_{CC}$ (where $V_{CC}$ equals $V_{OUT}$ or $V_{OUT}$-$V_F$, depending on whether VAUX functionality is used or not; see Section 5.9 VAUX pin operation in CC regulation).

**Figure 9. Blanking time after turn-off**

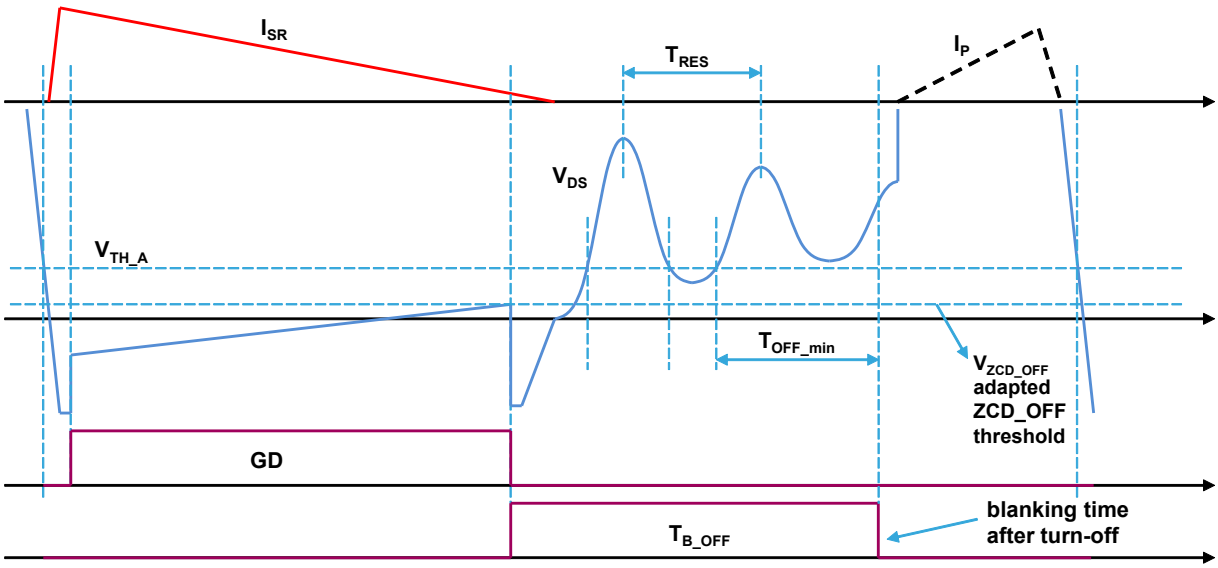
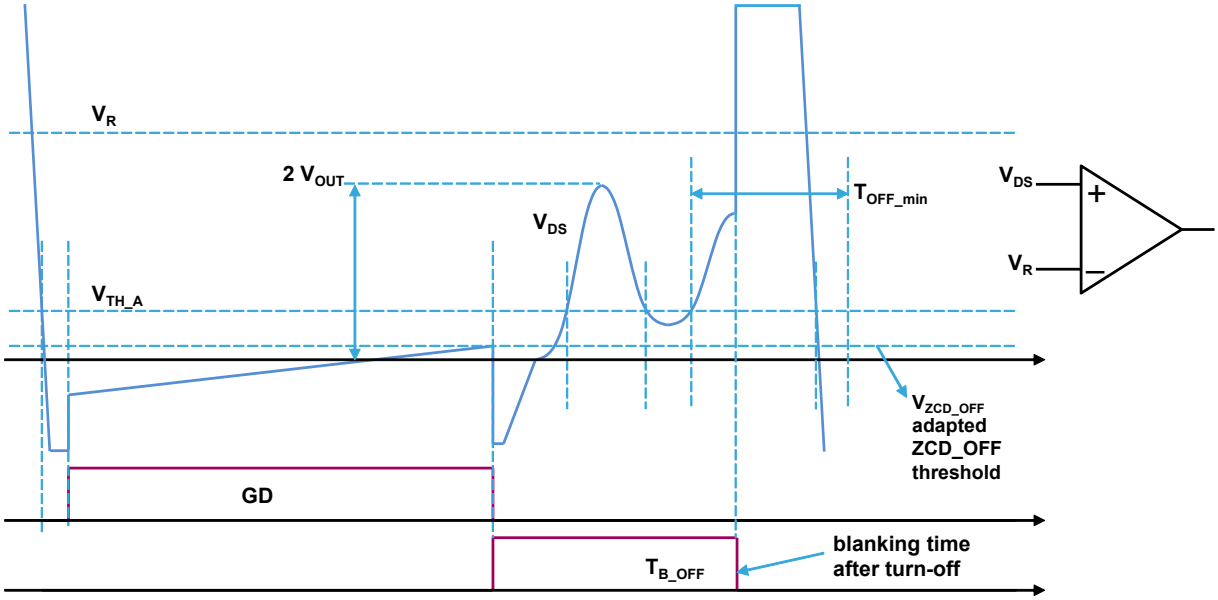


Figure 10. **Comparator for blanking time termination**




## 5.6 Start-up phase

At converter start-up, after the VCC pin voltage exceeds the turn-on threshold $V_{CC\_On}$, the SRK1001 controller enters the pinstrap phase (lasting 5 switching cycles), where it checks whether a 100 pF capacitor is present on TON pin or not and internally stores this information as long as $V_{CC}$ voltage remains above the turn-off threshold $V_{CC\_Off}$. After pinstrap, SRK1001 checks the DIS/SYNC pin. If it remains high, the driving is disabled (see Section 5.8 DIS/SYNC pin functions). If it is sensed low, SRK1001 enters sleep-mode state and, when it detects that the demagnetization time is longer than the programmed sleep-mode exiting threshold (see Section 5.7 Low consumption mode operation: sleep-mode, burst mode, disable state), the SRK1001 controller enters run mode and starts adapting the turn-off (with the ZCD comparator threshold starting from the minimum level $V_{ZCD\_OFF\_MIN}$).

## 5.7 Low consumption mode operation: sleep-mode, burst mode, disable state

By progressively reducing the load, the SR MOSFET conduction time (the transformer demagnetization time) also decreases. When the conduction time approaches the programmed minimum $T_{ON}$, the IC stops switching, reduces its consumption, and enters automatic sleep-mode state. The SR MOSFET conduction time to enter sleep-mode (measured from the falling and rising edge and of DVS across $V_{TH\_A}$) is:

$$T_{ON\_sleep\_in} = T_{ON\_MIN} + 300ns$$

The IC resumes operation when the load is increased and the conduction time of the SR MOSFET body diode becomes a fixed amount longer than the programmed minimum $T_{ON}$:

$$T_{ON\_sleep\_out} = 1.2{*}T_{ON\_MIN} + 300ns$$

Both $T_{ON\_sleep\_in}$ and $T_{ON\_sleep\_out}$ are measured from the instant when the DVS signal falls below $V_{TH\_A}$ and the instant when it rises above $V_{TH\_A}$ for the first time. Once the condition is detected, the device takes a single cycle to enter/exit sleep-mode operation.

The controller also enters low consumption mode when it detects primary controller burst-mode operation; that is, when a switching stop occurs for more than $T_{stop}$ ($V_{DS}$ is sensed higher than $V_{TH\_A}$ for more than $T_{stop}$). On converter operation resumption, the SRK1001 sleep out transition occurs after the first negative edge of the DVS voltage (falling below the threshold $V_{TH\_A}$). In this first cycle, gate driving is skipped, and from the next cycle, the SRK1001 starts driving and adapting the turn-off time instant.

It may occur that the SRK1001 enters sleep-mode first and then (after further load reduction) it detects primary controller burst-mode operation. In this case, when primary side switching operation restarts, the SRK1001 resumes SR MOSFET driving after it detects the body diode conduction time is larger than the sleep out value $T_{ON\_sleep\_out}$ for one cycle.

The IC may also enter low consumption mode when the DIS/SYNC pin goes high (left floating by user, it goes high by internal pull-up; refer to Section 5.8 DIS/SYNC pin functions).

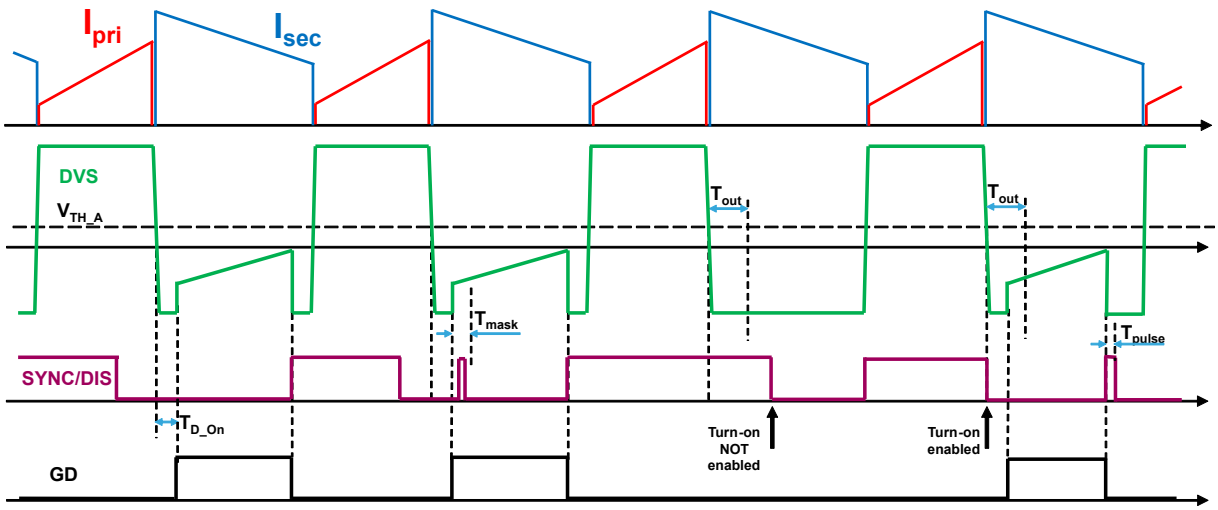
## 5.8 DIS/SYNC pin functions

The DIS/SYNC pin has two functions: disable and synchronization input.

As a disable input, it allows remote ON-OFF by user: an asynchronous turn-off of the SR MOSFET always occurs after a positive rising edge of the DIS pin voltage and, as long as it remains at high level (above $V_{DIS\_OFF}$ disable threshold), all switching functions are disabled and the gate output is pulled down. If the DIS pin voltage remains high for at least 4 switching cycles, the device enters low consumption mode. The operation resumes when the pin voltage decreases below the threshold $V_{DIS\_ON}$ and SR MOSFET body diode conduction time is detected longer than the sleep out value $T_{ON\_sleep\_out}$ for one cycle.

As a synchronization input, the pin allows turning off the SR MOSFET according to the applied signal. Synchronization function requires that no capacitor is placed between TON pin and GND. In this way the SR MOSFET turn-off is accomplished by the positive rising edge of the applied SYNC signal (during CCM operation) or when triggered by ZCD_OFF comparator output (during DCM operation). SR MOSFET turn-on is still triggered by the DVS signal falling edge, but it may only occur if the synchronization pin voltage is asserted low within a fixed timeout $T_{out}$ from DVS signal falling (refer to Figure 11). Furthermore, any glitch on synchronization signal is neglected within a masking time $T_{mask}$ after turn-on.

**Figure 11. DIS/SYNC pin synchronization timing**




The synchronization function is suitable in CCM flyback with fixed or variable operating frequency, where the sync signal (available at converter primary side) is transferred through a pulse transformer. Note that there must be the proper delay between the SR MOSFET turn-off time instant (i.e., the sync signal rising edge) and the turn-on of the primary side MOSFET, in order to avoid converter shoot-through. Therefore, the generation of the sync signal and of the primary MOSFET driving signal must be carefully controlled at primary side.

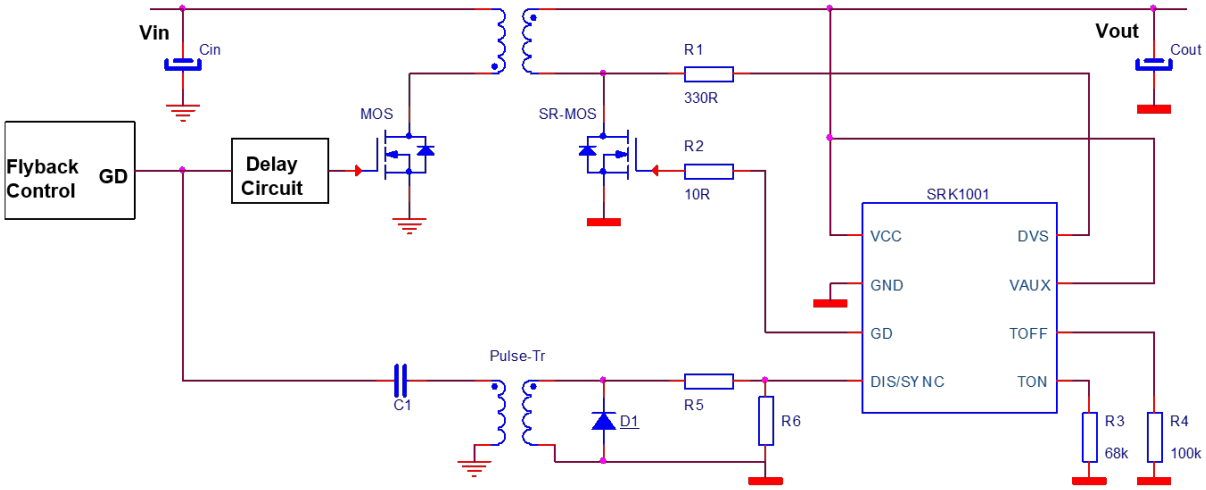
The schematic in Figure 12 shows the basic circuit: it is not necessary to transfer the complete driving signal from the primary controller. In fact, in order to turn off the SR MOSFET, the SRK1001 only needs to sense the rising edge of the sync signal, that can even be a pulse train, with the minimum pulse width equal to $T_{pulse}$. The coupling capacitor C1 (for transformer core reset) provides these short pulses through a very small pulse transformer.

The DIS/SYNC pin has an internal pull-up ($I_{DIS}$) and, if its functionality is not used, it must be connected to GND.

## 5.9 VAUX pin operation in CC regulation

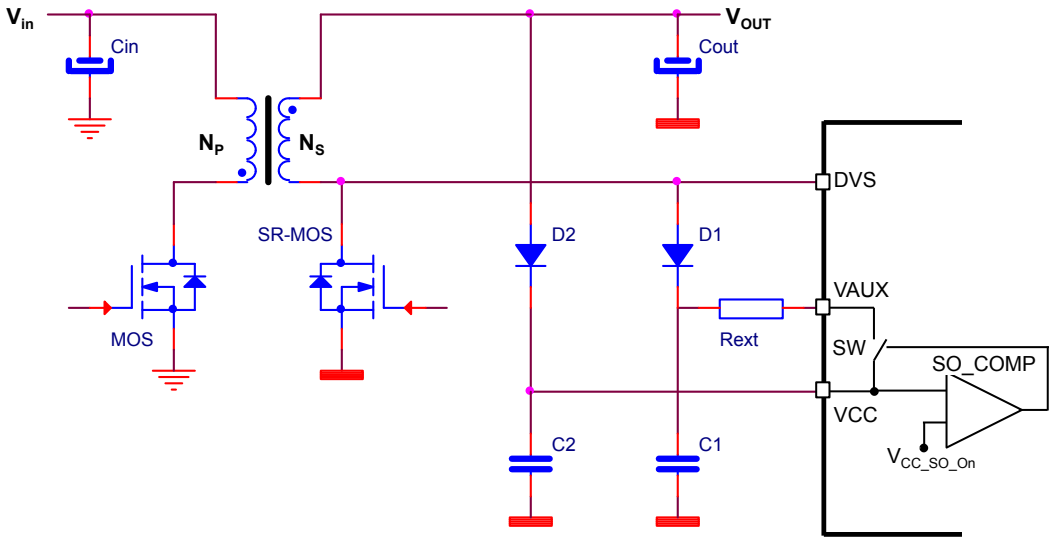
In charger applications operating in CC regulation, the output voltage $V_{out}$ (which is also used to supply the SRK1001) may considerably decrease while output current is kept constant at progressively reduced load impedance. For example, a 10 W charger, set at +5 V output in CV regulation, may be required to operate down to 2 V output while it is regulating the output current to somewhat more than 2 A in CC regulation.

Figure 12. **Sync circuit with pulse transformer**




In order to guarantee SR MOSFET switching even with low $V_{CC}$ supply voltage, the SRK1001 is provided with the VAUX pin. Referring to the schematic in Figure 13, when the $V_{CC}$ voltage decreases below the threshold $V_{CC\_SO\_On}$ (> $V_{CC\_Off}$), an internal switch is turned on allowing the capacitor C2 placed on VCC pin to be charged up to the turn-on threshold $V_{CC\_On}$ by a current drawn through VAUX pin.

Figure 13. **VAUX supply for CC regulation operation (from rectified SR MOSFET drain)**



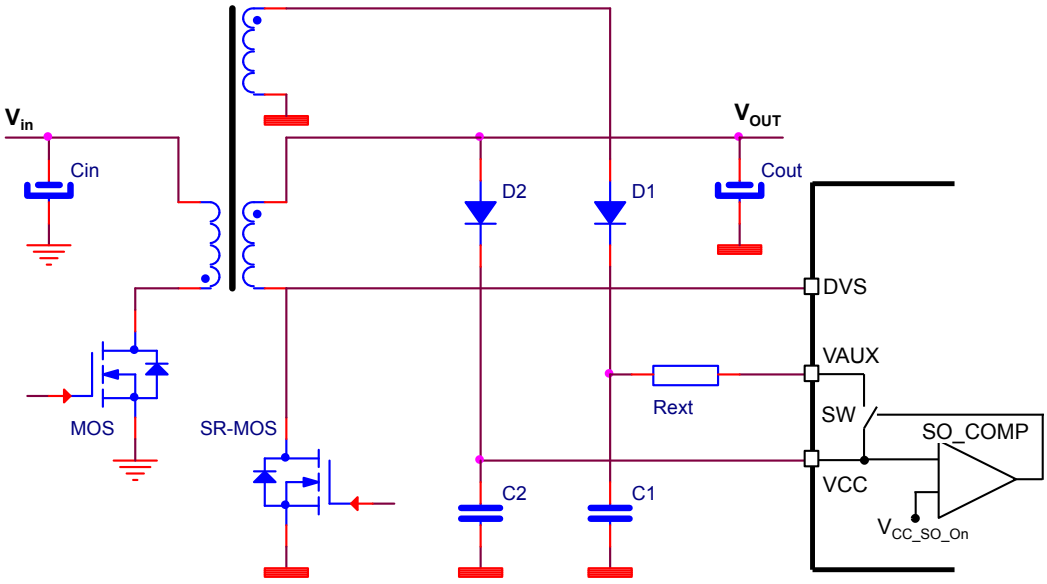

The VAUX pin may be connected, for example, to the rectified SR MOSFET drain voltage, like in Figure 13, or to another auxiliary voltage of the flyback transformer, as shown in Figure 14.

In either case, a (schottky) decoupling diode (D2) is necessary to avoid the VAUX pin charging the output capacitor. An external resistor $R_{ext}$ may be used in series with the VAUX pin in order to externally dissipate some of the power that, without that resistor, would be totally dissipated inside the SRK1001.

### 5.9.1 Example for parameter calculations

Considering the circuit in Figure 13, the following example is provided to calculate the value of the $R_{ext}$ resistor and power dissipation, in the case of a +5 V charger with operation down to 2 V in CC regulation and transformer secondary-to-primary reflected voltage of 75 V.

Figure 14. **VAUX supply for CC regulation operation from auxiliary winding**




**Step 1.** Measure or estimate the IC current consumption during CC regulation operation as below:

$$I_{CC} = I_{q\_run} + V_{CC\_avg} * C_{iss} * F_{sw} = 0.7mA + 4.1V * 5nF * 50kHz = 1.725mA$$

where $I_q$ is the IC quiescent current, $V_{cc\_avg}$ is the average voltage across VCC pin (mean value between $V_{CC\_On}$ and $V_{CC\_SO\_On}$), $C_{iss}$ is the SR MOSFET input capacitance and $F_{sw}$ is the operating frequency.

**Step 2.** Calculate the maximum and minimum voltage available at VAUX pin:

$$V_{AUX\_min} = V_{o.CC} + V_{in.min}\left(\frac{N_S}{N_P}\right) - V_F = 2V + 75V\left(\frac{1}{15}\right) - 0.35V = 6.65V$$

$$V_{AUX\_max} = V_{o.CC} + V_{in.max}\left(\frac{N_S}{N_P}\right) - V_F = 2V + 375V\left(\frac{1}{15}\right) - 0.35V = 26.65V$$

where $V_{o.CC}$ is the output voltage in CC regulation, $V_{in.min}$ / $V_{in.max}$ is the converter minimum/maximum input dc voltage, $N_S/N_P$ is the transformer turn ratio, and $V_F$ is the voltage drop of D1.

**Step 3.** Calculate the power dissipation of SRK1001, including device consumption and driving:

$$P_{d\_CC} = V_{cc\_avg} * I_{CC} = 4.1V * 1.725mA = 7.072mW$$

where $V_{CC\_avg}$ is the mean value between $V_{CC\_On}$ and $V_{CC\_SO\_On}$.

**Step 4.** Calculate the maximum external resistance in series to VAUX pin:

$$R_{ext\_MAX} = \frac{\left(V_{AUX\_min} - V_{CC\_On}\right)}{I_{CC}} - R_{on} = \frac{6.65V - 4.3V}{1.725mA} - 40\Omega = 1.322k\Omega$$

$$R_{tot} = R_{ext} + R_{on} = 1.2k\Omega + 40\Omega = 1.24k\Omega$$

where $R_{on}$ is the resistance of the internal VAUX switch.

**Step 5.** Calculate the maximum and minimum current from VAUX pin:

$$I_{AUX\_min} = \frac{V_{AUX\_min} - V_{CC\_On}}{R_{tot}} = \frac{6.65V - 4.3V}{1.24k\Omega} = 1.89mA$$

$$I_{AUX\_max} = \frac{V_{AUX\_max} - V_{CC\_On}}{R_{tot}} = \frac{26.65V - 4.3V}{1.24k\Omega} = 18.02mA$$

**Step 6.** Calculate the maximum power dissipation from VAUX at maximum input voltage ($V_{in.max}$):

$$P_{d\_AUX} = V_{AUX\_max} * I_{CC} = 26.65V * 1.725mA = 45.971mW$$

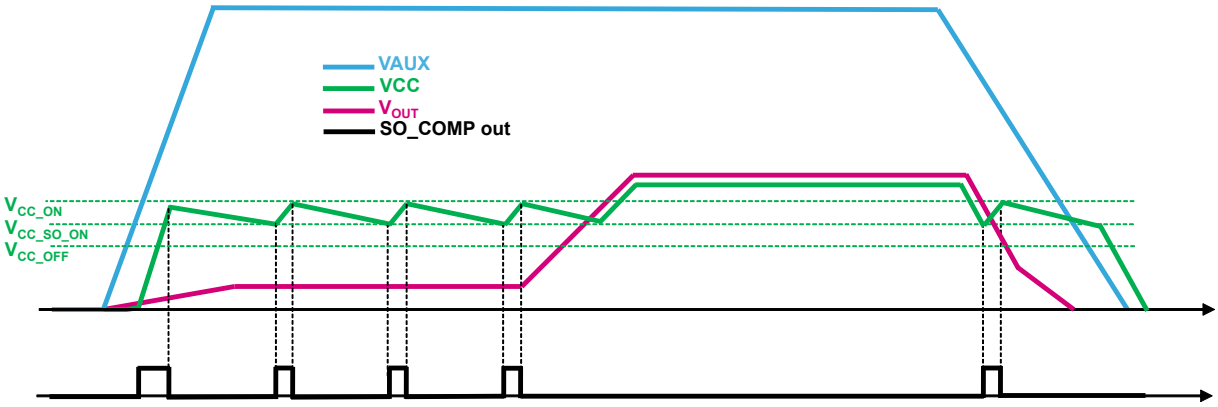
**Step 7.** Calculate the maximum power dissipation on external resistance and inside SRK1001:

$$P_{d\_Rext} = \frac{(P_{d\_AUX} - P_{d_{CC}})^{*}R_{ext}}{R_{tot}} = \frac{(45.971mW - 7.072mW)^{*}1.2k\Omega}{1.24k\Omega} = 37.64mW$$

$$P_{d\_SRK} = P_{d\_AUX} - P_{d\_Rext} = 45.971mW - 37.64mW = 8.33mW$$

The following figure shows VAUX pin operation during the various circuit phases (start-up phase, CC-CV regulation and mains turn-off).

**Figure 15. VAUX pin operation**




## 5.10 Operation in CC regulation and short circuit

During CC regulation operation in QR applications, the demagnetization time progressively increases while reducing the load impedance and the output voltage consequently reduces. Therefore, the conduction duty cycle of SR MOSFET driving progressively increases. The SRK1001 fixes a maximum driving pulse width level to $T_{ON\_MAX}$, and after this time interval has elapsed, it turns off the SR MOSFET. This means that, for the rest of the demagnetization time after $T_{ON\_MAX}$, the rectified current will continue flowing through the body diode.

If CC regulation is extended to short-circuit conditions (i.e., the output current is also regulated during short-circuit and the primary controller does not enter hiccup protection), some care must be taken to avoid temperature increase in the SR MOSFET, such as appropriate thermal design or the usage of an external schottky diode.

## 5.11 Adaptive gate drive

The IC is provided with a low-noise, high-current gate-drive output, capable of directly driving N-channel Power MOSFETs.

The high-level voltage provided by the driver is in fact clamped at $V_{GDclamp}$ (11.6 V typ.) through accurate circuitry. This avoids excessive voltage levels on the gate when the device is supplied with a high $V_{CC}$, thus minimizing the gate charge provided in each switching cycle.

Furthermore, the gate driver has a pull-down capability that ensures the SR MOSFET cannot be spuriously turned on even at low $V_{CC}$. In fact, the driver has a 1 V (typ.) saturation level at $V_{CC}$ below the turn-on threshold.

In order to optimize efficiency at low load levels (where driving losses may be relevant with respect to conduction losses), the high-level of driver output is adapted, decreasing with decreasing demagnetization time. The adaptive gate drive changes the driving high-level $V_{HIGH}$ in 16 steps of 400 mV, corresponding to 16 steps of detected demagnetization time $T_D$ of the transformer, as described by the following relationships:

$$T_D = 300ns + \frac{T_{ON\_min}^{*}(n+6)}{6}$$

$$V_{HIGH} = V_{GDclamp} - (16 - n)^{*}V_{GD\_ad\_step}$$

where $V_{GD\_ad\_step}$ is the voltage step and n = 1 to 16 is the step number.

The voltage step increase or decrease is performed after the demagnetization time interval $T_D$ has been detected longer or shorter by one step for 32 consecutive cycles..

The driver voltage level $V_{HIGH}$ is limited by the supply voltage on $V_{CC}$ pin and, in any case, when $V_{CC}$ voltage supply is detected lower than a threshold, the driver high-level modulation is disabled. A comparator with hysteresis enables adaptive drive when $V_{CC}$ supply increases above $V_{CC\_AGD\_en}$ and disables it as $V_{CC}$ falls below $V_{CC\_AGD\_dis}$. This means that if the $V_{CC}$ supply is low (but higher than $V_{CC\_AGD\_dis}$), the driver high-level $V_{HIGH}$ will be the minimum between the value of above formula and a value equal to:

- $V_{CC}$ supply if VAUX function is used (and VAUX pin voltage is larger than $V_{CC}$ - 1.2V), or
- $V_{CC}$ - 1.2 V if VAUX function is not used.

The adaptive gate drive is also disabled when the circuit enters burst-mode operation. On resuming operation from burst-mode, the gate drive always starts from the highest level and then it begins adapting the level according to the sensed demagnetization period.

In sleep-mode, the behavior is different. When the load (after entering sleep-mode) increases and the SRK1001 controller resumes switching, the gate drive starts from the lower level and then progressively adapts with step $V_{GD\_ad\_step}$ according to the sensed demagnetization period. The same also happens when the SRK1001 device exits the low-consumption state by DIS-SYNC pin. Also in this case, the gate drive starts from the lower level and then begins adapting with step $V_{GD\_ad\_step}$ according to the sensed demagnetization period.

Generally speaking, an SR MOSFET is always switched on after current starts flowing through its body diode when the drain-source voltage is already low (equal to $V_F$). Therefore, there is no Miller effect or switching losses at MOSFET turn-on. This is true also at turn-off, since rectifier current after the SR MOSFET is switched off continues flowing into the body diode. Consequently, the required gate charge the driver has to provide each cycle for ON/OFF switching is rather lower than in case of hard switching and can be easily determined from MOSFET datasheets in order to calculate the driver power dissipation.

# 6 Layout guidelines

The GND pin is the return of the bias current of the device and return for gate drive current. It should be routed along the shortest route possible to the common point where the source terminal of the SR MOSFET and output capacitor negative terminal are connected. When laying out the PCB, keep the source terminal of the SR MOSFET as close to output capacitor negative terminal as possible.

DVS connection to SR MOSFET drain terminal is not critical (since adaptive turn-off algorithm automatically compensates for stray inductances in the SR MOSFET current path). Nevertheless, it is preferable to sense the MOSFET voltage as close to its drain terminal as possible.

The usage of bypass capacitors between the VCC pin and GND pin is recommended. They should be low-ESR, low-ESL type and located as close to the IC pins as possible. Sometimes, a series resistor (in the tens of Ohms) between the converter output voltage and the VCC pin, forming an RC filter along with the bypass capacitor, is useful to obtain a cleaner $V_{CC}$ voltage.

Since the TON pin and TOFF pin source current is relatively low, this pin may be affected by current injections coming from nearby tracks with high dV/dt (i.e., drain sense signals). Therefore, TON pin and TOFF pin should be kept away from SR MOSFET drain tracks. In case of large noise, a capacitor can be used on these pins for filtering. For the TOFF pin, the allowed capacitance $C_{OFF}$ is such that the time constant $R_{OFF}$ $C_{OFF}$ is lower than 100 µs. For the TON pin, as it is also used for internal timer setting according to user selected operation (quasi-resonant or fixed frequency), the allowed capacitance $C_{ON}$ is as follows:

- Max. 22 pF for quasi-resonant operation
- Min. 100 pF and time constant $R_{ON}$ $C_{ON}$ < 100 µs for fixed frequency operation

In applications where high noise is present on the sensed DVS signal (especially after the SR MOSFET turn-off instant with a non-optimized layout or coupling with other asynchronous noise sources), some RC filtering on the DVS pin may help avoid undesirable device operation.

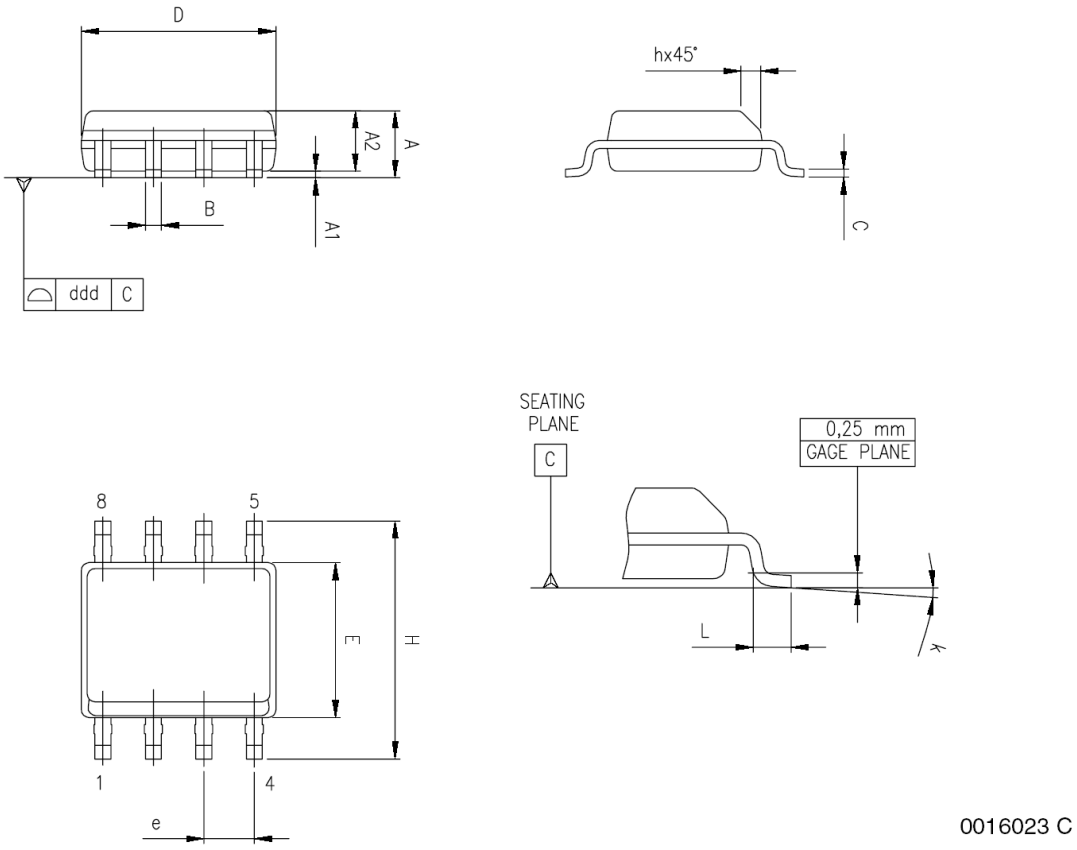
# 7 Package mechanical data

**Table 5. SO8 mechanical data**

| Dimensions | | | | | | |
|---|---|---|---|---|---|---|
| Ref. | mm | | | inch | | |
| | Min | Typ | Max | Min | Typ | Max |
| A | 1.35 | | 1.75 | 0.053 | | 0.069 |
| A1 | 0.10 | | 0.25 | 0.004 | | 0.010 |
| A2 | 1.10 | | 1.65 | 0.043 | | 0.065 |
| B | 0.33 | | 0.51 | 0.013 | | 0.020 |
| C | 0.19 | | 0.25 | 0.007 | | 0.010 |
| D (1) | 4.80 | | 5.00 | 0.189 | | 0.197 |
| E | 3.80 | | 4.00 | 0.150 | | 0.157 |
| e | | 1.27 | | | | |
| H | 5.8 | | 6.20 | 0.228 | 0.050 | 0.244 |
| h | 0.25 | | 0.50 | 0.010 | | 0.020 |
| L | 0.40 | | 1.27 | 0.016 | | 0.050 |
| k | 0° (min), 8° (max) | | | | | |
| ddd | | | 0.10 | | | 0.004 |

1. *D dimensions do not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs should not exceed 0.15 mm (0.006 inch) in total (both sides)*

**Figure 16. SO8 package outline**



# Revision history

Table 6. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 29-Nov-2019 | 1 | Initial release. |

# Contents

# List of figures

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