STL65P4LLF6AG

Automotive P-channel -40 V, 0.0115 Ω typ., -57 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - preliminary data

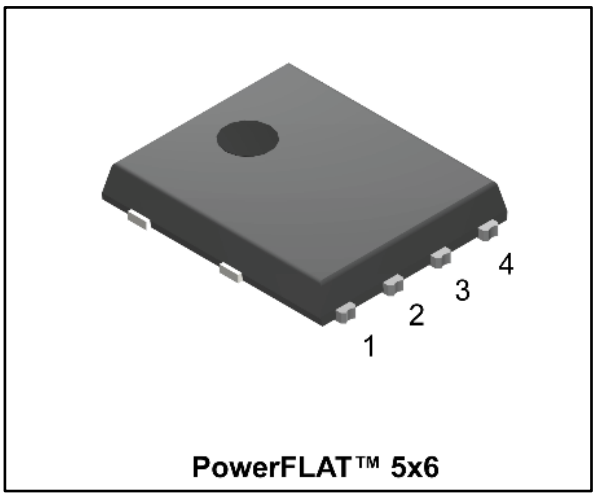
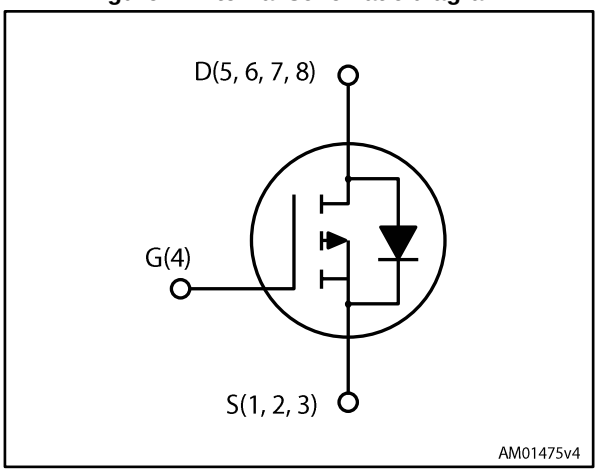


Figure 1: Internal schematic diagram



Features

Order codes	V_{DS}	$R_{DS(on)max.}$	I_D
STL65P4LLF6AG	-40 V	0.014 Ω	-57

- Designed for automotive applications
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

Applications

Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order codes	Marking	Package	Packing
STL65P4LLF6AG	65P4LLF6	PowerFLAT™ 5x6	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-40	V
V_{GS}	Gate-source voltage	±18	V
I_D	Drain current (continuous) at T_C = 25 °C	-57	A
I_D	Drain current (continuous) at T_C = 100 °C	-35	A
I_D (1)	Drain current (pulsed)	-228	A
P_{TOT}	Total dissipation at T_C = 25 °C	73	W
T_{stg}	Storage temperature range	- 55 to +150	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.7	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	32	°C/W

Notes:

(1)When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 s.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = -250 µA	-40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = -40 V			-1	µA
		V_{GS} = 0 V, V_{DS} = -40 V, T_C = 125 °C (1)			-10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V_{GS} = - 18 V			-100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-2.5	V
$R_{DS(on)}$	Static drain source on-resistance	V_{GS} = -10 V, I_D = -6.5 A		0.0115	0.014	Ω
		V_{GS} = -4.5 V, I_D = -6.5 A		0.015	0.019	Ω

Notes:

(1)Defined by design, not subject to production test

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ISS}	Input capacitance	V_{DS} = -25 V, f = 1 MHz, V_{GS} = 0 V	-	3525	-	pF
C_{OSS}	Output capacitance			344		pF
C_{rss}	Reverse transfer capacitance			238		pF
Q_g	Total gate charge	V_{DD}= -20 V, I_D = -13 A, V_{GS} = -4.5 to 0 V (See *Figure 14: "Gate charge test circuit"*)		34		nC
Q_{gs}	Gate-source charge			11.3		nC
Q_{gd}	Gate-drain charge			13.8		nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = -20 V, I_D = -6.5 A, R_G = 4.7 Ω, V_{GS} = -10 V (See *Figure 13: "Switching times test circuit for resistive load"*)	-	49.4	-	ns
t_r	Rise time		-	60.6	-	ns
$t_{d(off)}$	Turn-off delay time		-	170	-	ns
t_f	Fall time		-	20	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	I_{SD} = -6.5 A, V_{GS} = 0 V	-		-1.1	V
t_{rr}	Reverse recovery time	I_{SD} = -13 A, di/dt = 100 A/µs V_{DD} = -24 V, T_j =150 °C (See *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	29		ns
Q_{rr}	Reverse recovery charge		-	27.6		nC
I_{RRM}	Reverse recovery current		-	1.9		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

For the P-channel Power MOSFET, current and voltage polarities are reversed.

Figure 2: Safe operating area

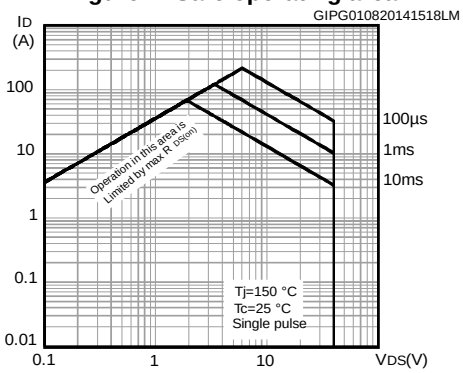


Figure 3: Thermal impedance

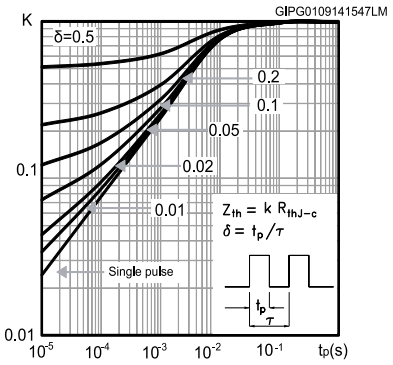


Figure 4: Output characteristics

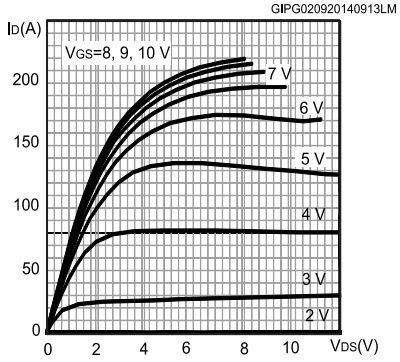


Figure 5: Transfer characteristics

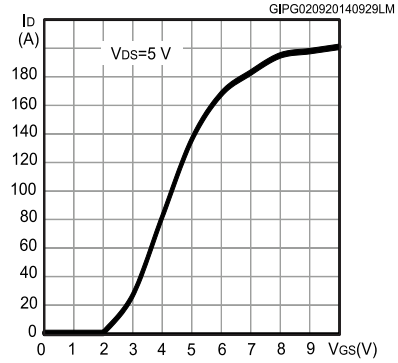


Figure 6: Gate charge vs gate-source voltage

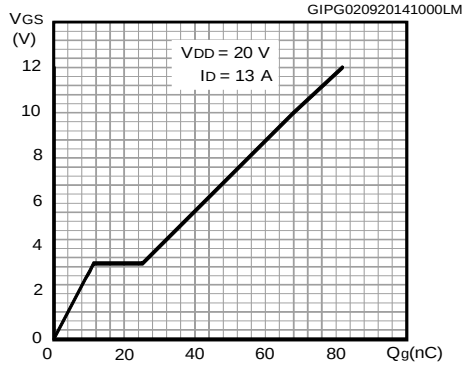


Figure 7: Static drain-source on-resistance

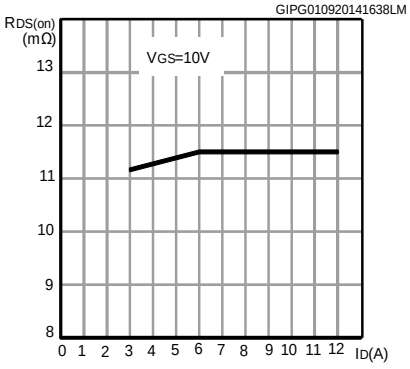


Figure 8: Capacitance variation

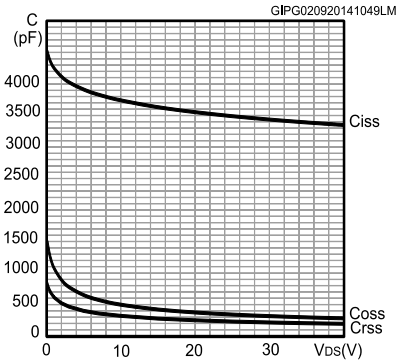


Figure 9: Normalized gate threshold voltage vs temperature

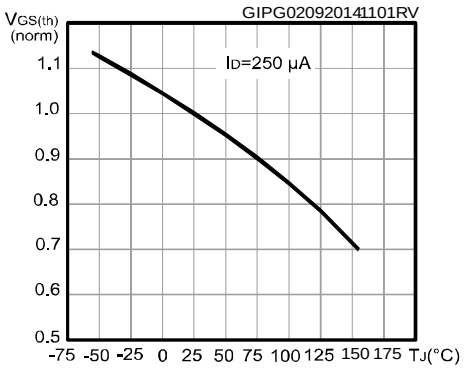


Figure 10: Normalized on-resistance vs temperature

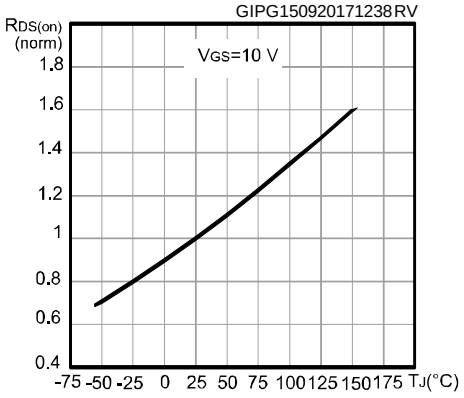


Figure 11: Normalized VBR(DSS) vs temperature

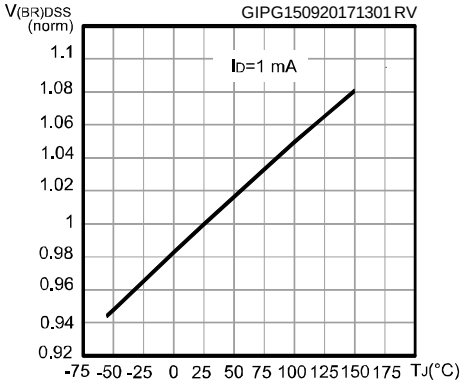
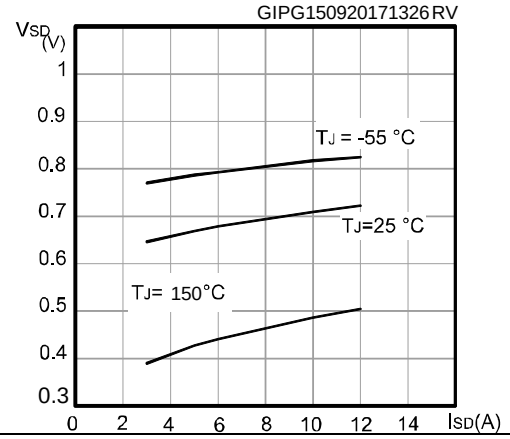


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Switching times test circuit for resistive load

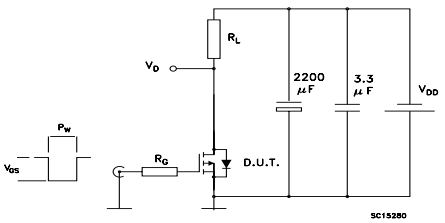


Figure 14: Gate charge test circuit

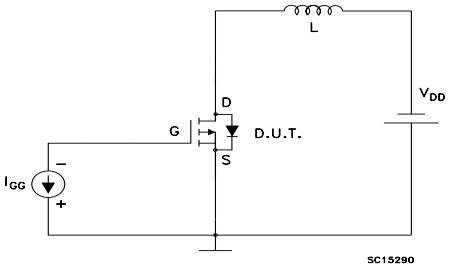
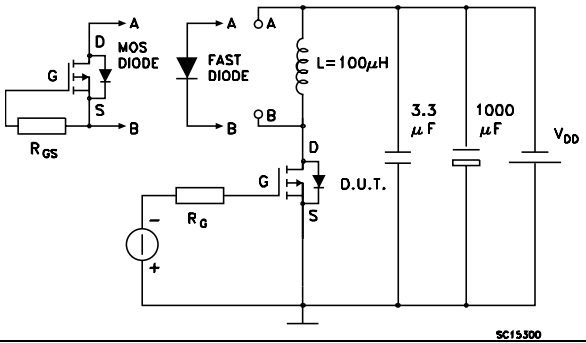


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 PowerFLAT™ 5x6 WF type R package information

Figure 16: PowerFLAT™ 5x6 WF type R package outline

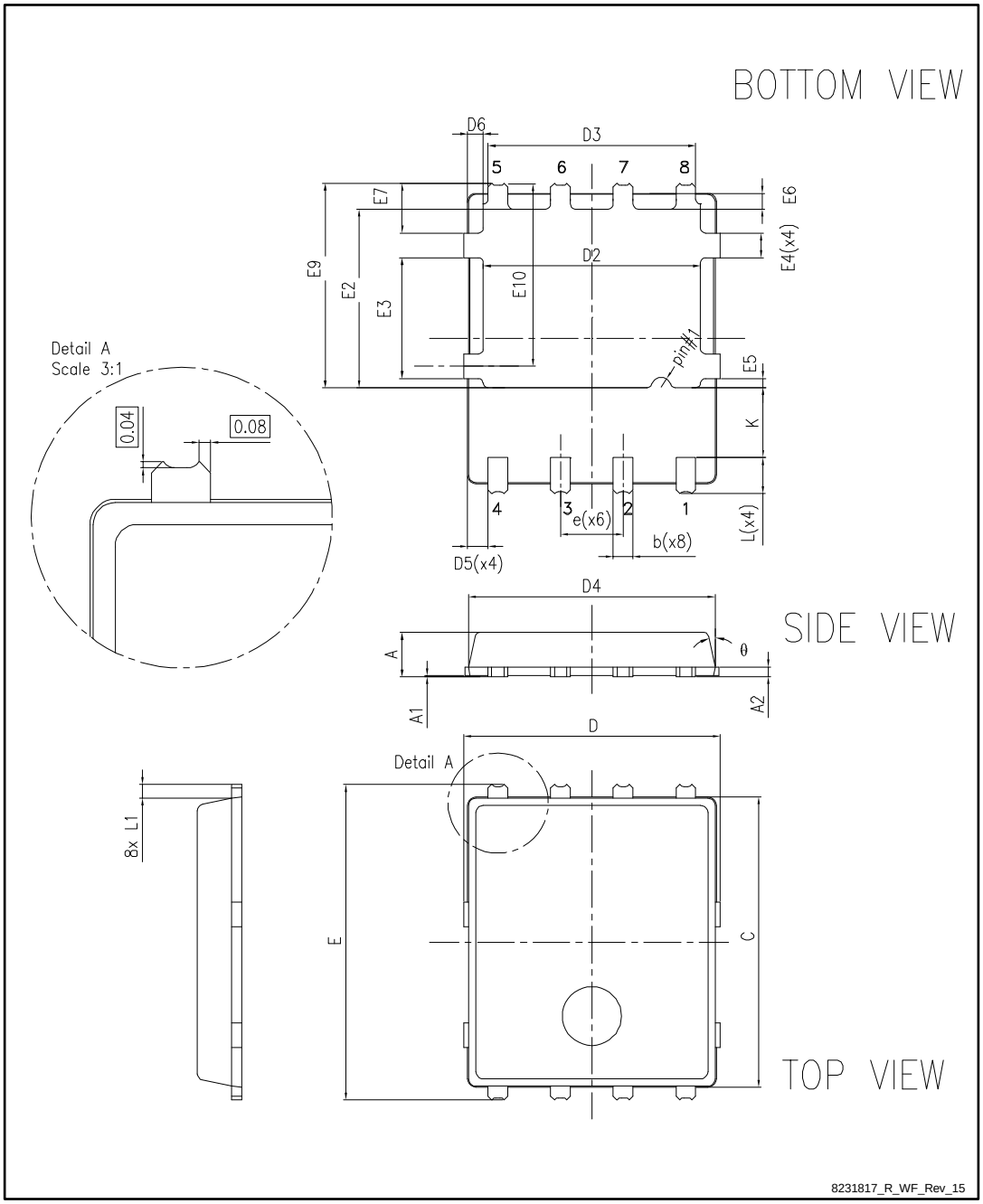
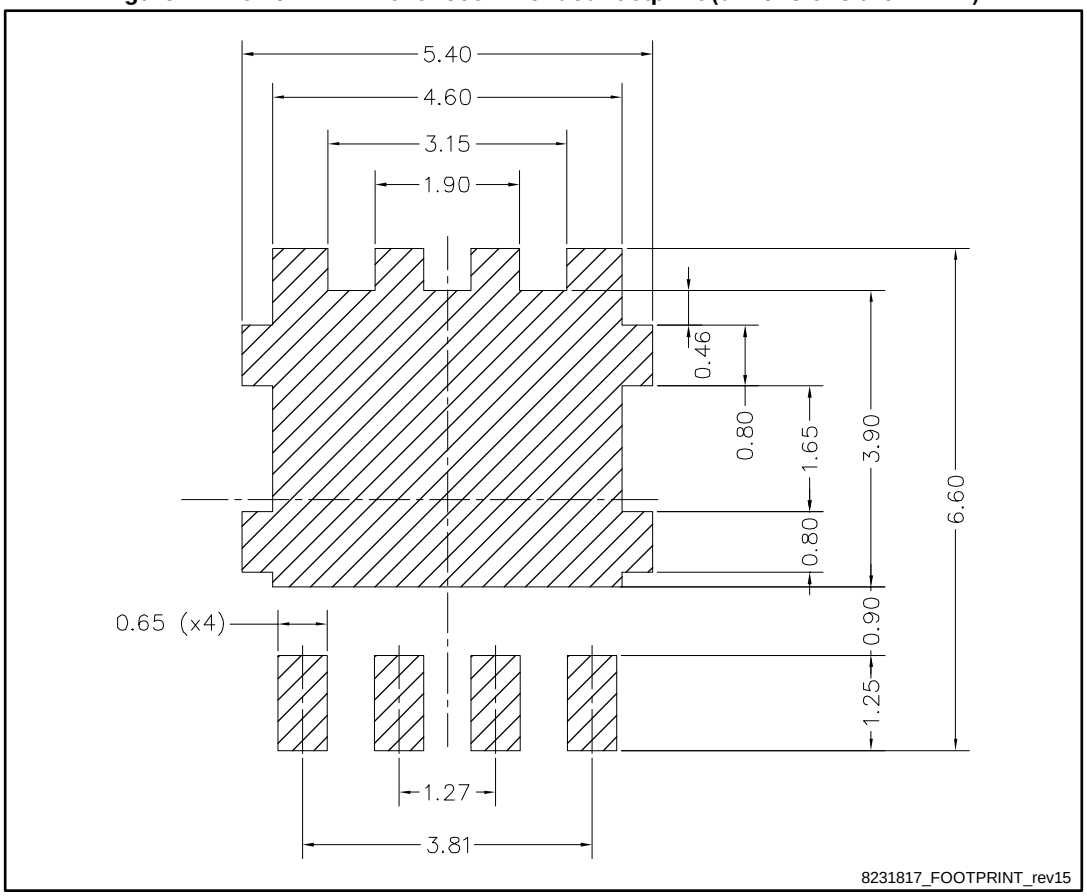


Table 8: PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.10
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.10
D5	0.25	0.4	0.55
D6	0.15	0.3	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.85	1.00	1.15
E9	4.00	4.20	4.40
E10	3.55	3.70	3.85
K	1.275		1.575
L	0.725	0.825	0.925
L1	0.175	0.275	0.375
Θ	0°		12°

Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



4.2 PowerFLAT™ 5x6 WF packing information

Figure 18: PowerFLAT™ 5x6 WF tape (dimensions are in mm)

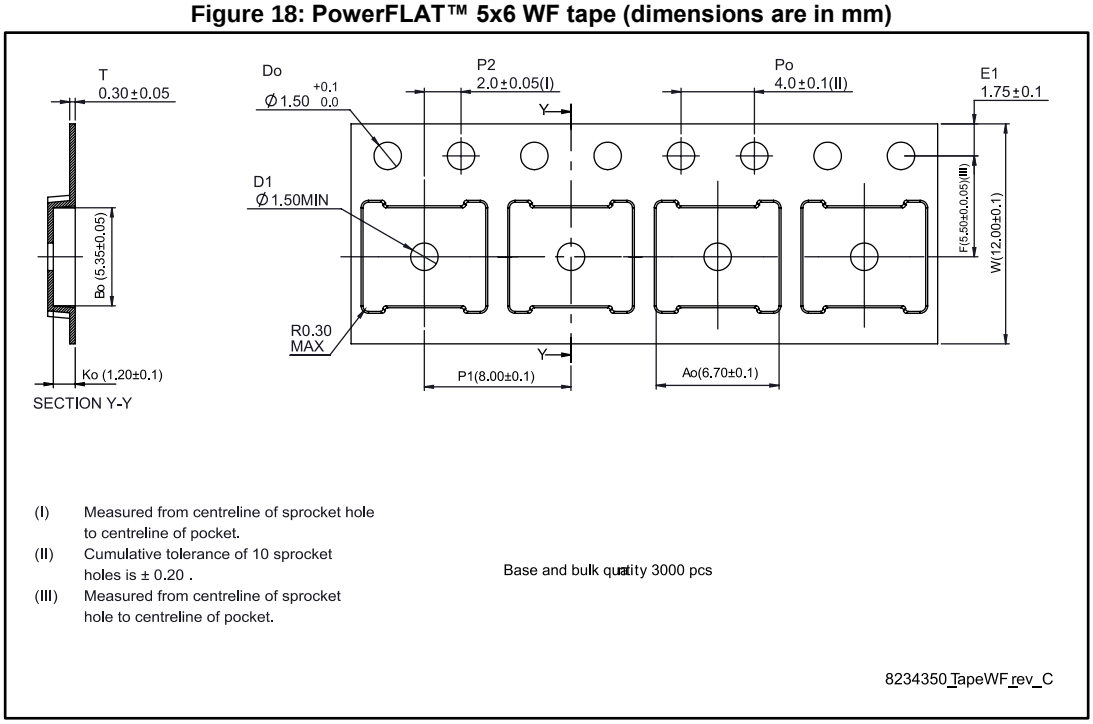


Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape

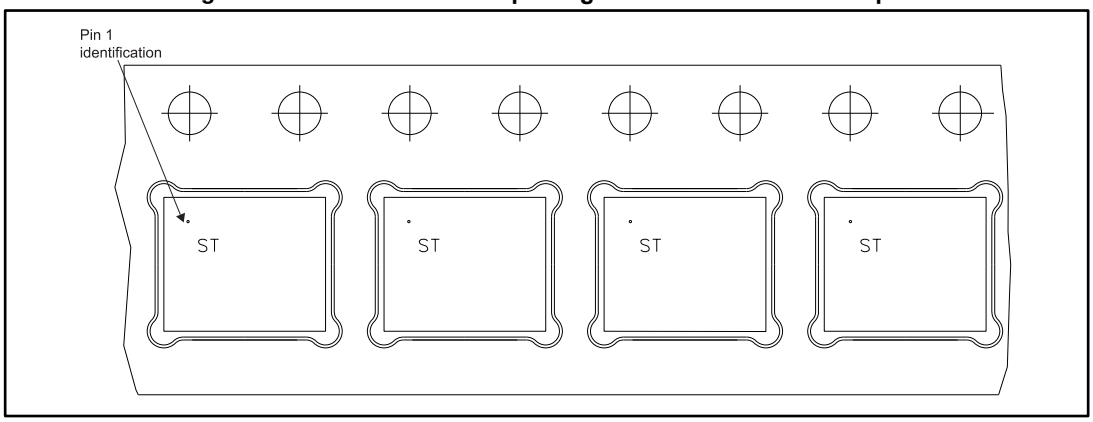
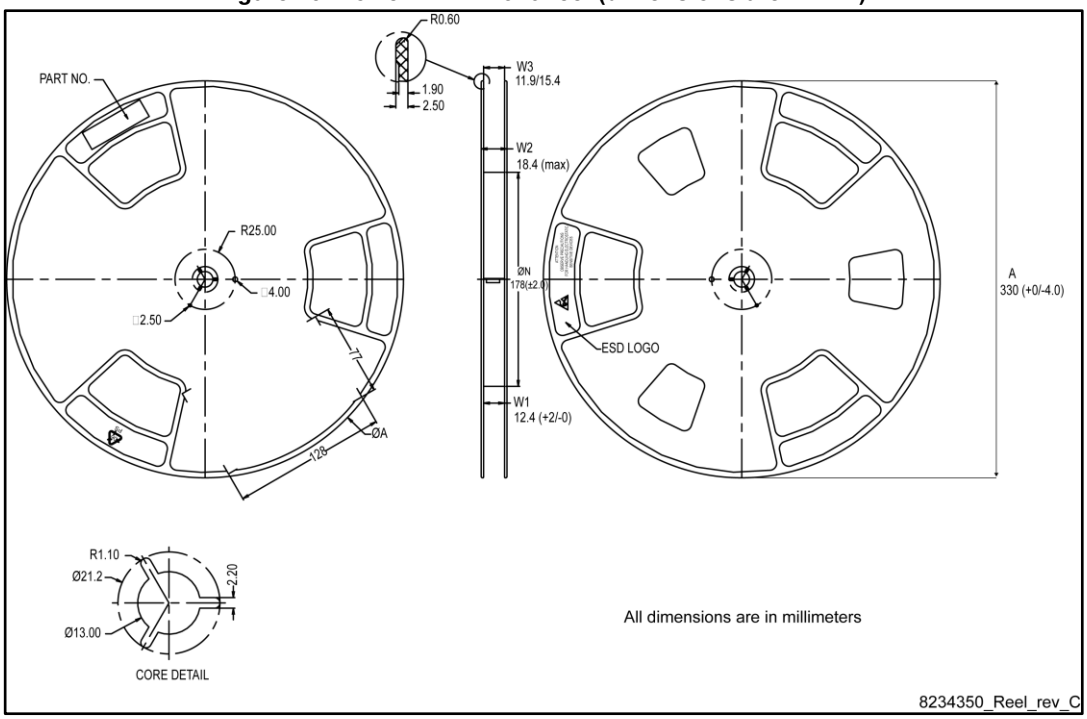


Figure 20: PowerFLAT™ 5x6 reel (dimensions are in mm)



5 Revision history

Table 9: Document revision history

Date	Revision	Changes
2-Jul-2016	1	Initial release.
19-Sep-2017	2	Updated *Section "Features"* in cover page. Updated *Table 2: "Absolute maximum ratings"* and *Table 3: "Thermal data"*. Updated *Table 4: "On/off states"*. Updated *Figure 6: "Gate charge vs gate-source voltage"*. Updated *Table 4: "On/off states"* and *Table 5: "Dynamic"*. Updated *Section 2.1: "Electrical characteristics (curves)"* Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.