

STY145N65M5

N-channel 650 V, 0.012 Ω typ., 138 A MDmesh™ M5 Power MOSFET in a Max247 package

Datasheet - production data

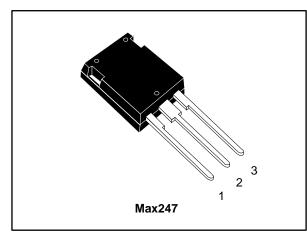
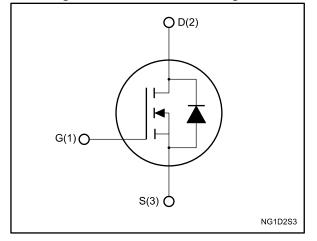


Figure 1: Internal schematic diagram



Features

Order code	V _{DS} @ T _{Jmax}	R _{DS(on)} max.	I _D
STY145N65M5	710 V	0.015 Ω	138 A

- Extremely low R_{DS(on)}
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

• Switching applications

Description

This device is an N-channel Power MOSFET based on the MDmesh[™] M5 innovative vertical process technology combined with the well-known PowerMESH[™] horizontal layout. The resulting product offers extremely low onresistance, making it particularly suitable for applications requiring high power and superior efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STY145N65M5	145N65M5	Max247	Tube

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STY145N65M5 Electrical ratings

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T _C = 25 °C	138	Α
I_D	Drain current (continuous) at T _C = 100 °C	87	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	552	Α
P _{TOT}	Total dissipation at $T_C = 25$ °C	625	W
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	12	Α
E _{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR} , V_{DD} = 50 V)	2420	mJ
dv/dt ⁽²⁾	Peak diode recovery voltage slope	15	V/ns
T _{stg}	Storage temperature	- 55 to 150	°C
Tj	Max. operating junction temperature	150	

Notes:

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case max	0.2	°C/W
R _{thj-amb}	Thermal resistance junction-ambient max	30	°C/W

 $[\]ensuremath{^{(1)}}\mbox{Pulse}$ width limited by safe operating area.

 $^{{\}rm (2)}I_{\rm SD} \leq 138~{\rm A,~di/dt} \leq 400~{\rm A/\mu s;~V_{\rm DS(peak)}} < V_{\rm (BR)DSS},~V_{\rm DD} = 400~{\rm V}.$

Electrical characteristics STY145N65M5

2 Electrical characteristics

 T_C = 25 °C unless otherwise specified

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	650			V
	Zava mata walta na duain	$V_{GS} = 0 \text{ V}, V_{DS} = 650 \text{ V}$			10	μΑ
I _{DSS}	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 650 \text{ V},$ $T_{C} = 125 \text{ °C}$			100	μΑ
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±100	nΑ
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 69 A		0.012	0.015	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	18500	1	pF
Coss	Output capacitance	V_{DS} = 100 V, f = 1 MHz,	-	413	ı	pF
C _{rss}	Reverse transfer capacitance	$V_{GS} = 0 V$	-	11	ı	pF
C _{o(er)} ⁽¹⁾	Equivalent output capacitance energy related	$V_{GS} = 0$, $V_{DS} = 0$ to 520 V	-	415	ı	pF
C _{o(tr)} ⁽²⁾	Equivalent output capacitance time related		-	1950	1	pF
R _G	Intrinsic gate resistance f = 1 MHz, open drain		-	0.7	ı	Ω
Q_g	Total gate charge	$V_{DD} = 520 \text{ V}, I_D = 69 \text{ A},$	-	414	-	nC
Q_{gs}	Gate-source charge	V _{GS} = 10 V (see Figure 15: "Test circuit for gate charge	-	114	1	nC
Q_{gd}	Gate-drain charge	behavior")	-	164	-	nC

Notes:

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 $^{^{(1)}}$ Co_(er) is defined as a constant equivalent capacitance giving the same stored energy as Coss when VDS increases from 0 to 80% VDSS

 $^{^{(2)}}C_{o(tr)} \ \text{is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}}$

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(V)}	Voltage delay time	$V_{DD} = 400 \text{ V}, I_D = 85 \text{ A}$	ı	255	-	ns
$t_{r(V)}$	Voltage rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$ (see Figure 16: "Test circuit	ı	11	-	ns
t _{f(i)}	Current fall time	for inductive load switching	-	82	-	ns
$t_{C(off)}$	Crossing time	and diode recovery times" and Figure 19: "Switching time waveform")	-	88	-	ns

Table 7: Source drain diode

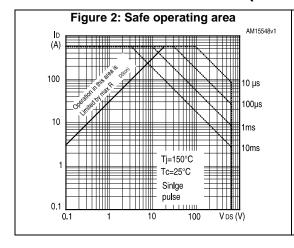
Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		138	Α
I _{SDM} , (1)	Source-drain current (pulsed)		-		552	Α
V _{SD} ⁽²⁾	Forward on voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 138 \text{ A}$	ı		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 138 A,	-	568		ns
Qrr	Reverse recovery charge	$di/dt = 100 \text{ A/}\mu\text{s},$ $V_{DD} = 100 \text{ V (see } Figure$	-	14.5		μC
I _{RRM}	Reverse recovery current	16: "Test circuit for inductive load switching and diode recovery times")	-	51		А
t _{rr}	Reverse recovery time	I _{SD} = 138 A,	-	728		ns
Q_{rr}	Reverse recovery charge	rge di/dt = 100 A/μs, V _{DD} = 100 V, T _i = 150 °C		24.5		μC
I _{RRM}	Reverse recovery current	(see Figure 16: "Test circuit for inductive load switching and diode recovery times")		67		А

Notes:

 $^{^{(1)}}$ Pulse width is limited by safe operating area

 $^{^{(2)}\}text{Pulsed:}$ pulse duration = 300 $\mu\text{s,}$ duty cycle 1.5%

2.2 Electrical characteristics (curves)



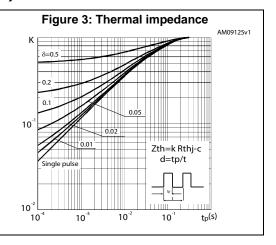
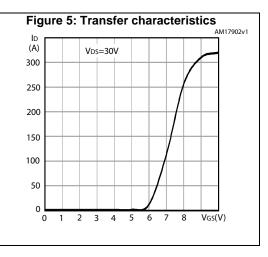
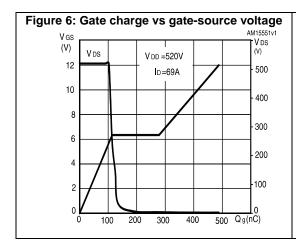
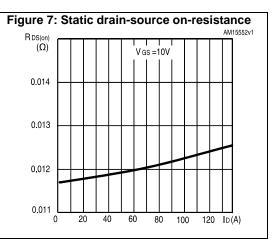


Figure 4: Output characteristics ID(A) Vgs=10V 300 8V 250 200 150 7V 100 50 6V 10 15 20 V_{DS}(V)







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STY145N65M5 Electrical characteristics

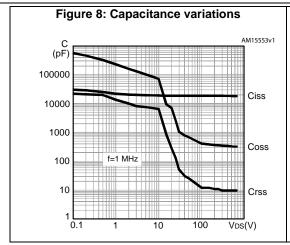


Figure 9: Normalized gate threshold voltage vs temperature

V_{GS(th)}
(norm)
1.10

1.00

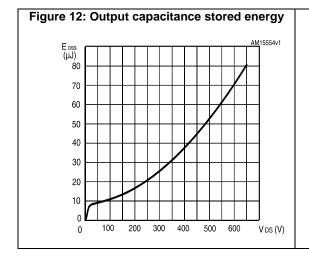
0.90

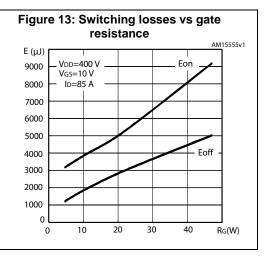
0.80

0.70

-50 -25 0 25 50 75 100 TJ(°C)

Figure 11: Normalized V_{(BR)DSS} vs temperature AM10399v1 1.08 ID = 1mA1.06 1.04 1.02 1.00 0.98 0.96 0.94 0.92 TJ(°C) -25 25 50 75 100 0





The previous figure E_{on} includes reverse recovery of a SiC diode.

Test circuits STY145N65M5

3 Test circuits

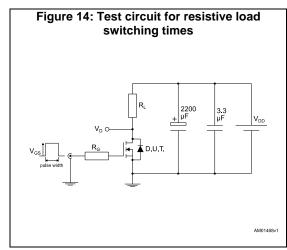
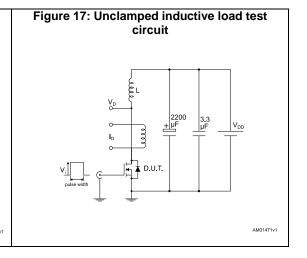


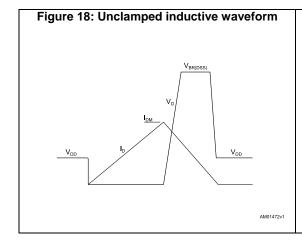
Figure 15: Test circuit for gate charge behavior

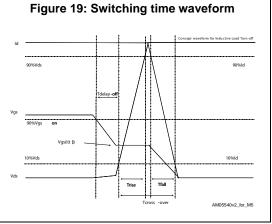
12 V 47 kΩ 100 nF 1 kΩ

Vos 1 Lo CONST 100 Ω D.U.T.

2200 VG AM01469v1







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STY145N65M5 Package information

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: **www.st.com**. ECOPACK® is an ST trademark.

4.1 Max247 package information

HEAT-SINK PLANE Gate D A 1 *b1 b2* BACK VIEW 0094330_Rev_D

Figure 20: Max247 package outline

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Table 8: Max247 package mechanical data

Dim.			
Dilli.	Min.	Тур.	Max.
А	4.70	-	5.30
A1	2.20	-	2.60
b	1.00	-	1.40
b1	2.00	-	2.40
b2	3.00	-	3.40
С	0.40	-	0.80
D	19.70	-	20.30
е	5.35	-	5.55
Е	15.30	-	15.90
L	14.20	-	15.20
L1	3.70	-	4.30

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STY145N65M5 Revision history

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
25-Sep-2012	1	First release.
17-Jan-2013	2	Modified: I _{AR} and E _{AS} values Modified: typical values on Table 5, 6 and 7
13-Nov-2015	3	Updated title, features and description on cover page. Document status promoted from preliminary to production data. Modified: Table 2: "Absolute maximum ratings" and Table 3: "Thermal data" Updated: Figure 4: "Output characteristics" and Figure 5: "Transfer characteristics" Minor text changes.



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