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MPSW45, MPSW45A

One Watt Darlington Transistors

NPN Silicon

Features

- Pb-Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector - Emitter Voltage MPSW45 MPSW45A	V_{CES}	40 50	Vdc
Collector - Base Voltage MPSW45 MPSW45A	V_{CBO}	50 60	Vdc
Emitter - Base Voltage	V_{EBO}	12	Vdc
Collector Current - Continuous	I_C	1.0	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	1.0 8.0	W mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	2.5 20	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	125	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	50	$^\circ\text{C}/\text{W}$

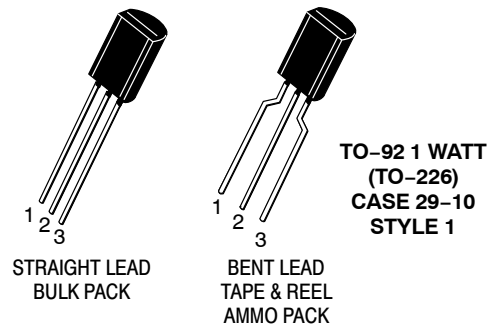
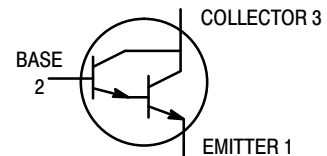
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

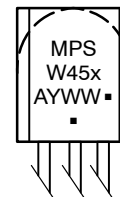


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MARKING DIAGRAM



MPSW45x = Device Code
 x = 45A Devices
 A = Assembly Location
 Y = Year
 WW = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MPSW45, MPSW45A

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $V_{BE} = 0$)	MPSW45 MPSW45A	$V_{(BR)CES}$	40 50	– –	Vdc
Collector – Base Breakdown Voltage ($I_C = 100 \mu\text{Adc}$, $I_E = 0$)	MPSW45 MPSW45A	$V_{(BR)CBO}$	50 60	– –	Vdc
Emitter – Base Breakdown Voltage ($I_E = 10 \mu\text{Adc}$, $I_C = 0$)		$V_{(BR)EBO}$	12	–	Vdc
Collector Cutoff Current ($V_{CB} = 30 \text{Vdc}$, $I_E = 0$) ($V_{CB} = 40 \text{Vdc}$, $I_E = 0$)	MPSW45 MPSW45A	I_{CBO}	– –	100 100	nAdc
Emitter Cutoff Current ($V_{EB} = 10 \text{Vdc}$, $I_C = 0$)		I_{EBO}	–	100	nAdc

ON CHARACTERISTICS (Note 1)

DC Current Gain ($I_C = 200 \text{mAdc}$, $V_{CE} = 5.0 \text{Vdc}$) ($I_C = 500 \text{mAdc}$, $V_{CE} = 5.0 \text{Vdc}$) ($I_C = 1.0 \text{Adc}$, $V_{CE} = 5.0 \text{Vdc}$)		h_{FE}	25,000 15,000 4,000	150,000 – –	–
Collector – Emitter Saturation Voltage ($I_C = 1.0 \text{Adc}$, $I_B = 2.0 \text{mAdc}$)		$V_{CE(sat)}$	–	1.5	Vdc
Base – Emitter Saturation Voltage ($I_C = 1.0 \text{Adc}$, $I_B = 2.0 \text{mAdc}$)		$V_{BE(sat)}$	–	2.0	Vdc
Base – Emitter On Voltage ($I_C = 1.0 \text{Adc}$, $V_{CE} = 5.0 \text{Vdc}$)		$V_{BE(on)}$	–	2.0	Vdc

SMALL-SIGNAL CHARACTERISTICS

Current – Gain – Bandwidth Product ($I_C = 200 \text{mAdc}$, $V_{CE} = 5.0 \text{Vdc}$, $f = 100 \text{MHz}$)		f_T	100	–	MHz
Collector – Base Capacitance ($V_{CB} = 10 \text{Vdc}$, $I_E = 0$, $f = 1.0 \text{MHz}$)		C_{cb}	–	6.0	pF

1. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$; Duty Cycle $\leq 2.0\%$.

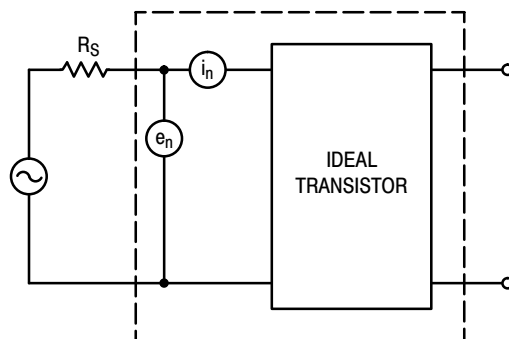


Figure 1. Transistor Noise Model

MPSW45, MPSW45A

NOISE CHARACTERISTICS

($V_{CE} = 5.0 \text{ Vdc}$, $T_A = 25^\circ\text{C}$)

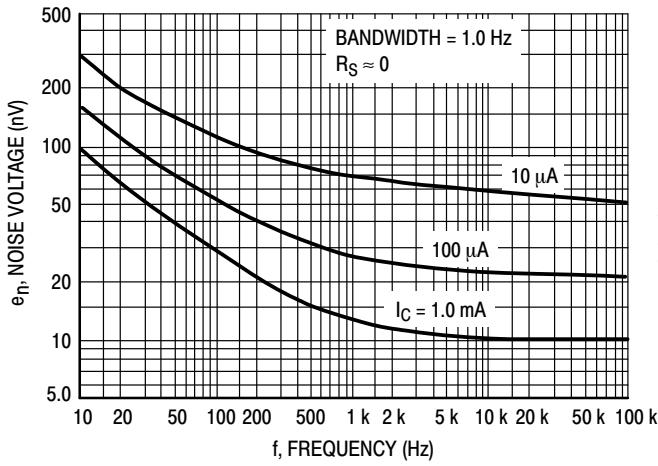


Figure 2. Noise Voltage

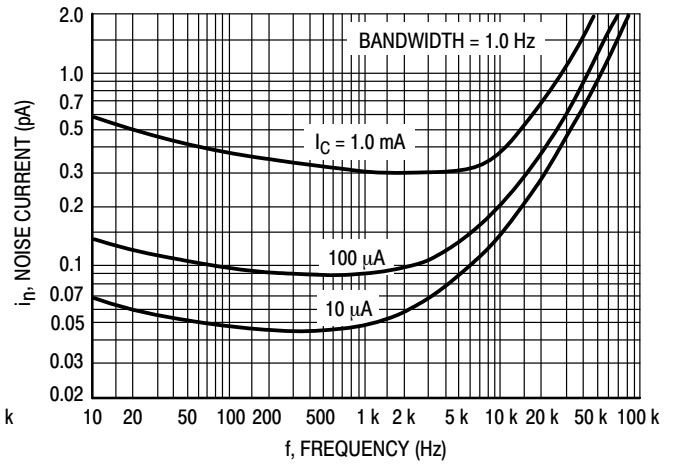


Figure 3. Noise Current

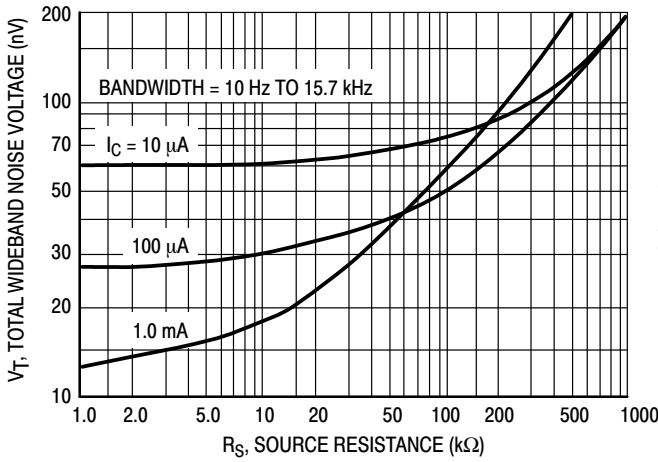


Figure 4. Total Wideband Noise Voltage

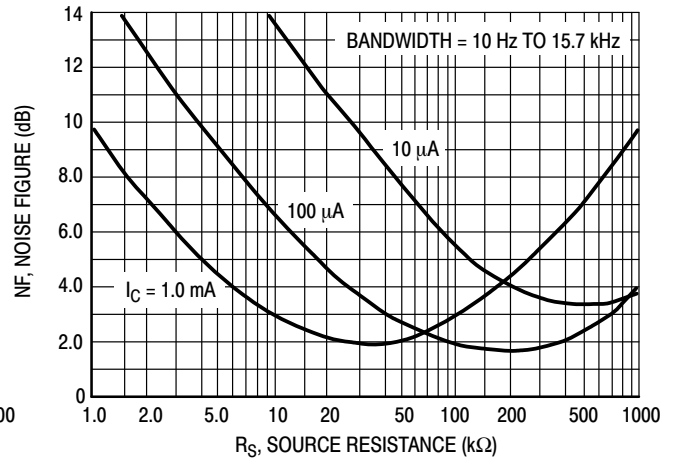


Figure 5. Wideband Noise Figure

MPSW45, MPSW45A

SMALL-SIGNAL CHARACTERISTICS

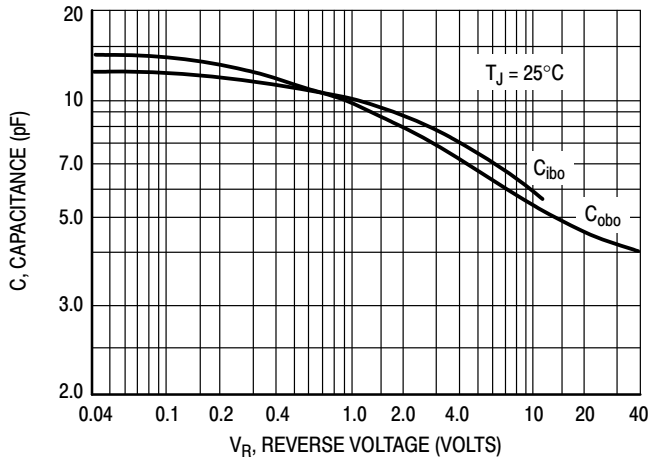


Figure 6. Capacitance

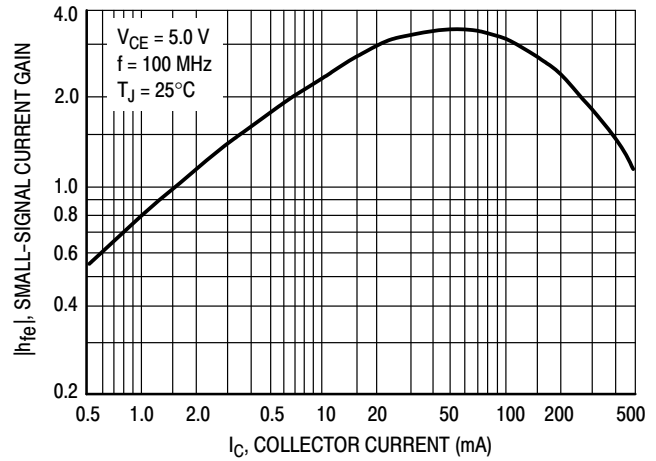


Figure 7. High Frequency Current Gain

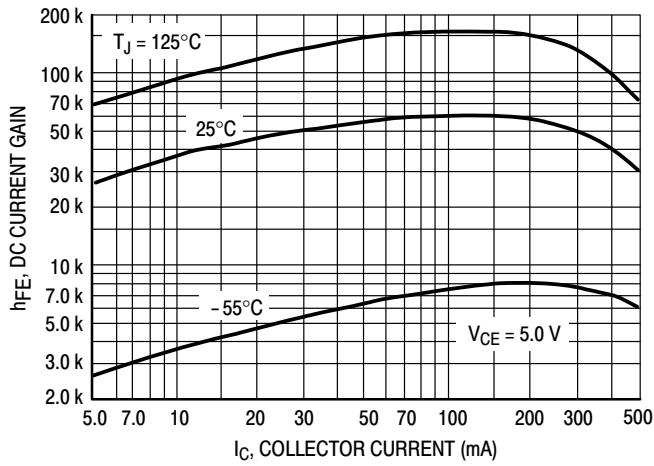


Figure 8. DC Current Gain

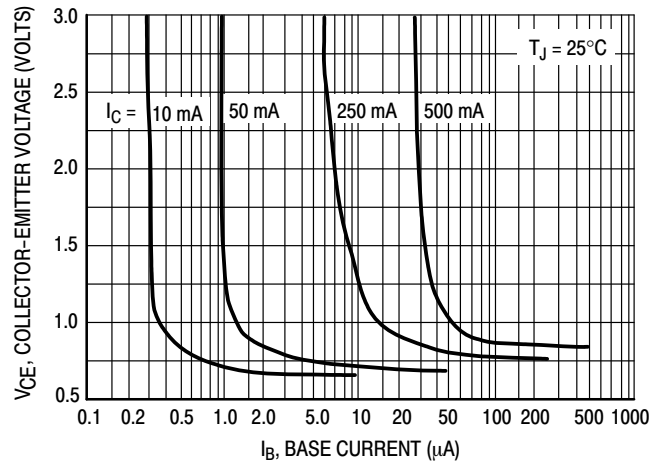


Figure 9. Collector Saturation Region

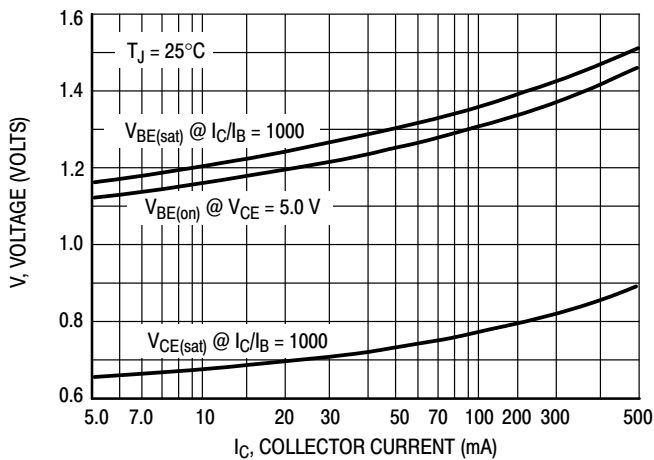


Figure 10. "On" Voltages

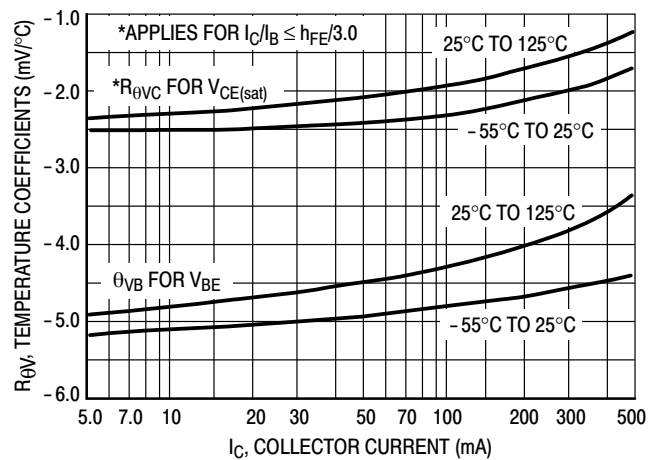


Figure 11. Temperature Coefficients

MPSW45, MPSW45A

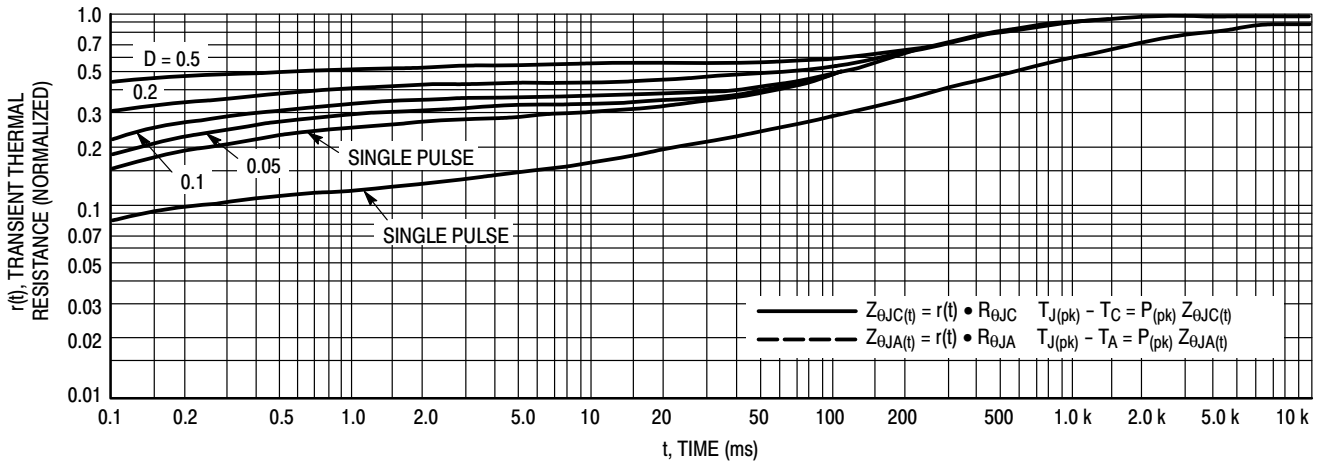


Figure 12. Thermal Response

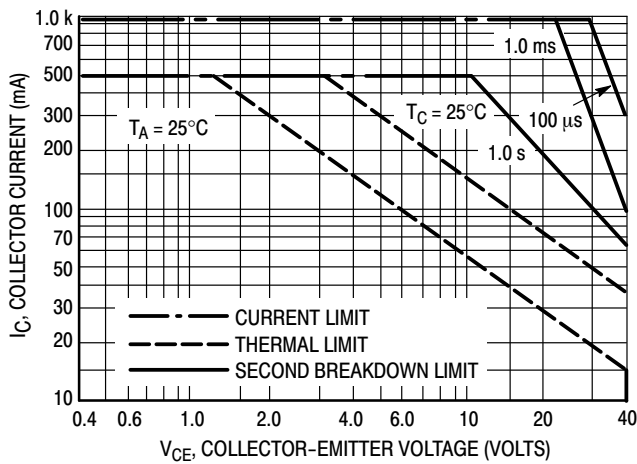
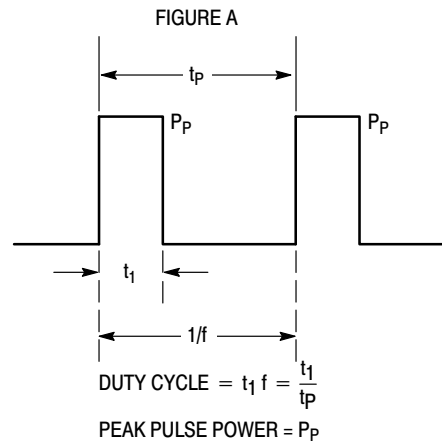


Figure 13. Active Region Safe Operating Area



Design Note: Use of Transient Thermal Resistance Data

ORDERING INFORMATION

Device	Package	Shipping†
MPSW45G	TO-92 (Pb-Free)	5,000 Units / Box
MPSW45RLREG	TO-92 (Pb-Free)	2,000 / Tape & Reel
MPSW45A	TO-92	5,000 Units / Box
MPSW45AG	TO-92 (Pb-Free)	5,000 Units / Box
MPSW45ARLRA	TO-92	2,000 / Tape & Reel
MPSW45ARLRAG	TO-92 (Pb-Free)	2,000 / Tape & Reel
MPSW45AZL1	TO-92	2,000 / Ammo Pack
MPSW45AZL1G	TO-92 (Pb-Free)	2,000 / Ammo Pack

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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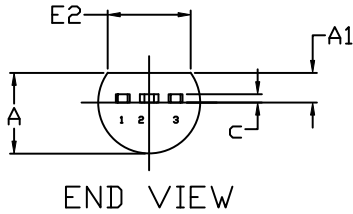
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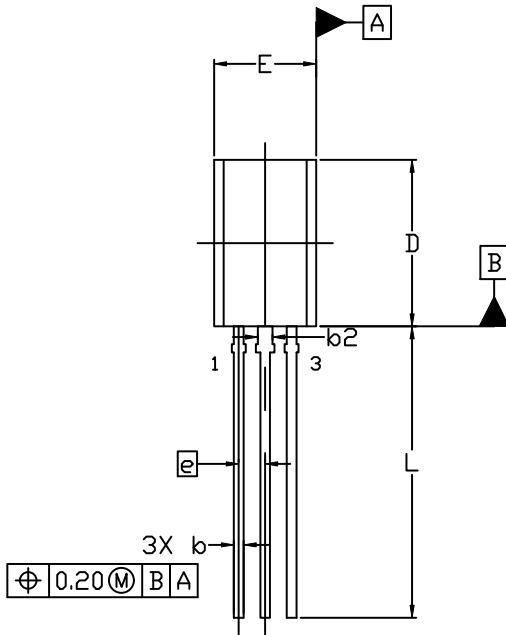
TO-92 (TO-226) 1 WATT
CASE 29-10
ISSUE D

DATE 05 MAR 2021

STRAIGHT LEAD



END VIEW



TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

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FORMED LEAD



END VIEW



TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
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D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

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CASE 29-10
ISSUE D**

DATE 05 MAR 2021

- | | | | | |
|-----------------------------------------------------------------------------|--------------------------------------------------------------------------------|----------------------------------------------------------------------------|---------------------------------------------------------------------------|-----------------------------------------------------------------------|
| <p>STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR</p> | <p>STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR</p> | <p>STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE</p> | <p>STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE</p> |
| <p>STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN</p> | <p>STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE</p> | <p>STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE</p> | <p>STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2</p> | <p>STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE</p> |
| <p>STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE</p> | <p>STYLE 12:
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2. GATE
3. MAIN TERMINAL 2</p> | <p>STYLE 13:
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2. GATE
3. CATHODE 2</p> | <p>STYLE 14:
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2. COLLECTOR
3. BASE</p> | <p>STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2</p> |
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2. GATE
3. CATHODE</p> | <p>STYLE 17:
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PIN 1. GATE
2. SOURCE
3. DRAIN</p> | <p>STYLE 24:
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3. CATHODE</p> | <p>STYLE 25:
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2. GATE
3. MT 2</p> |
| <p>STYLE 26:
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2. GROUND 2
3. OUTPUT</p> | <p>STYLE 27:
PIN 1. MT
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3. MT</p> | <p>STYLE 28:
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2. ANODE
3. GATE</p> | <p>STYLE 29:
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2. ANODE
3. CATHODE</p> | <p>STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE</p> |
| <p>STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE</p> | <p>STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER</p> | <p>STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT</p> | <p>STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC</p> | <p>STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER</p> |

**GENERIC
MARKING DIAGRAM***



- XXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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