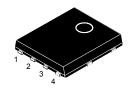
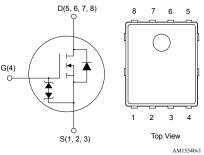


N-channel 600 V, 220 mΩ typ., 10 A, MDmesh™ M6 Power MOSFET in a PowerFLAT™ 5x6 HV package



PowerFLAT™ 5x6 HV





Product status link

STL22N60M6

Product summary		
Order code STL22N60M6		
Marking 22N60M6		
Package	PowerFLAT™ 5x6 HV	
Packing	Tape and reel	

Features

Order code	V _{DS}	R _{DS(on)} max.	l _D
STL22N60M6	600 V	250 mΩ	10 A

- Reduced switching losses
- Lower R_{DS(on)} per area vs previous generation
- · Low gate input resistance
- 100% avalanche tested
- · Zener-protected

Applications

- · Switching applications
- LLC converters
- Boost PFC converters

Description

The new MDmesh $^{\text{TM}}$ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±25	V
1_	Drain current (continuous) at T _{case} = 25 °C	10	
l _D	Drain current (continuous) at T _{case} = 100 °C	6	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	40	Α
P _{TOT}	Total power dissipation at T _{case} = 25 °C	57	W
dv/dt ⁽²⁾ .	Peak diode recovery voltage slope	15	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	100	V/IIS
T _{stg}	Storage temperature range	-55 to 150	°C
T _j	T _j Operating junction temperature range		C

- 1. Pulse width is limited by safe operating area.
- 2. $I_{SD} \leq 10~A,~di/dt = 400~A/\mu s,~V_{DS} < V_{(BR)DSS},~V_{DD} = 400~V$
- 3. $V_{DS} \le 480 \text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	2.2	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	50	°C/W

1. When mounted on 1 inch2 FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _{Jmax})	2.9	Α
E _{AS}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	230	mJ

DS12833 - Rev 1 page 2/15



2 Electrical characteristics

 $(T_{case} = 25 \, ^{\circ}C \text{ unless otherwise specified}).$

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}$	600			V
		V _{GS} = 0 V, V _{DS} = 600 V			1	
I_{DSS}	I _{DSS} Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 600 V,			100	μA
		$T_{case} = 125 ^{\circ}C^{(1)}$			100	
I _{GSS}	Gate-body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±5	μA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.25	4	4.75	V
R _{DS(on)}	Static drain-source on-resistance	I _D = 5 A, V _{GS} = 10 V		220	250	mΩ

^{1.} Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	800	-	
C _{oss}	Output capacitance	$V_{DS} = 100 \text{ V, f} = 1 \text{ MHz, V}_{GS} = 0 \text{ V}$	-	52.6	-	pF
C _{rss}	Reverse transfer capacitance		-	4.3	-	
Coss eq. (1)	Equivalent output capacitance	V _{DS} = 0 to 480 V, V _{GS} = 0 V	-	181	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	4.7	-	Ω
Qg	Total gate charge	V _{DD} = 480 V, I _D = 15 A,	-	20	-	
Q _{gs}	Gate-source charge	V _{GS} = 0 to 10 V	-	5.6	-	nC
Q _{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	9.5	-	

^{1.} $C_{\text{oss eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 7.5 A,	-	13.6	-	
t _r	Rise time	$R_G = 4.7 \Omega$, $V_{GS} = 10 V$	-	6.3	-	
t _{d(off)}	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and	-	32	-	ns
t _f	Fall time	Figure 18. Switching time waveform)	-	8.7	-	

DS12833 - Rev 1 page 3/15



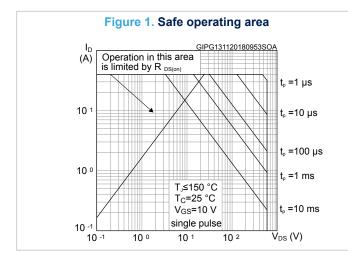
Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		10	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		40	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 10 A, V _{GS} = 0 V	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 15 A, di/dt = 100 A/μs,	-	217		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V	-	1.99		μC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	18.3		A
t _{rr}	Reverse recovery time	$I_{SD} = 15 \text{ A, di/dt} = 100 \text{ A/µs,}$	-	299		ns
Q _{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}, T_j = 150 \text{ °C}$	-	2.95		μC
I _{RRM}	Reverse recovery current	 (see Figure 15. Test circuit for inductive load switching and diode recovery times) 	-	19.7		Α

- 1. Pulse width is limited by safe operating area.
- 2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%



2.1 Electrical characteristics (curves)



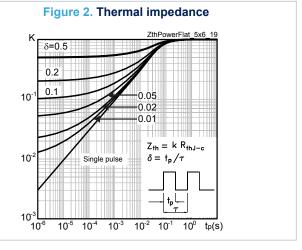
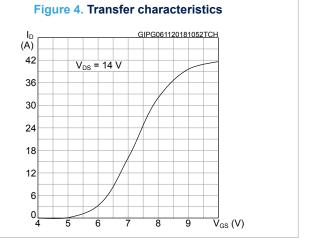
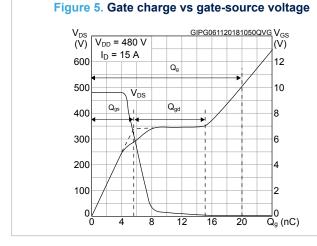
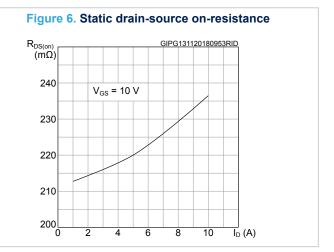


Figure 3. Output characteristics I_D (A) V_{GS} =10 V 42 V_{GS} =9 V 36 V_{GS} =8 V 30 24 18 V_{GS} =7 V12 V_{GS} =6 V12 14 10







DS12833 - Rev 1 page 5/15



Figure 7. Capacitance variations C (pF) GIPG061120181052CVR 10³ C_{ISS} 10² Coss 10 1 C_{RSS} f = 1 MHz 10 º $V_{DS}(V)$ 10 -1 10 0 10 ¹ 10²

E_{OSS} (μJ) (βADG061120181125EOS (μJ) 8 7 6 6 5 4 4 3 2 1 0 0 100 200 300 400 500 600 V_{DS} (V)

temperature

V_{GS(th)} (norm.)

1.1

I_D = 250 μA

0.9

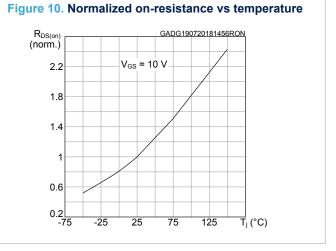
0.8

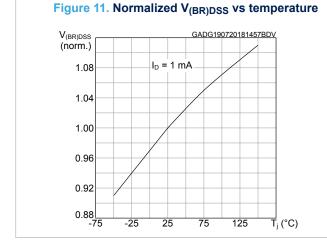
0.7

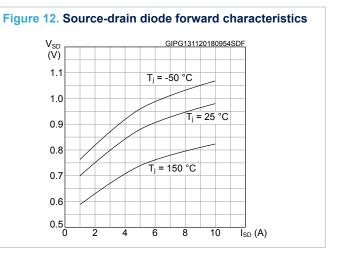
0.6

-75 -25 25 75 125 T_j (°C)

Figure 9. Normalized gate threshold voltage vs







DS12833 - Rev 1 page 6/15



3 Test circuits

Figure 13. Test circuit for resistive load switching times

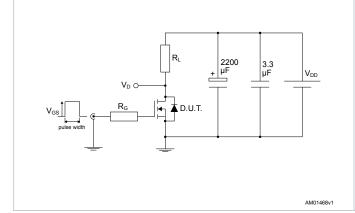


Figure 14. Test circuit for gate charge behavior

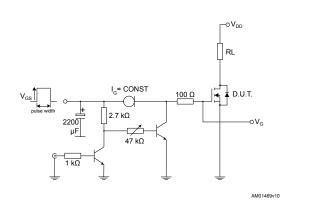


Figure 15. Test circuit for inductive load switching and diode recovery times

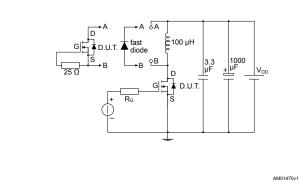


Figure 16. Unclamped inductive load test circuit

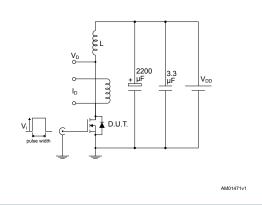


Figure 17. Unclamped inductive waveform

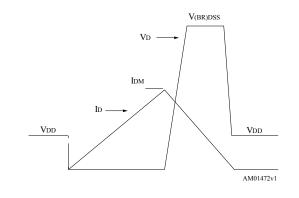
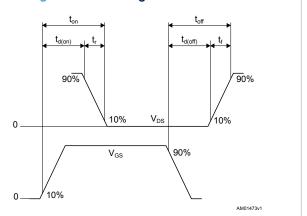


Figure 18. Switching time waveform



DS12833 - Rev 1 page 7/15



4 Package information

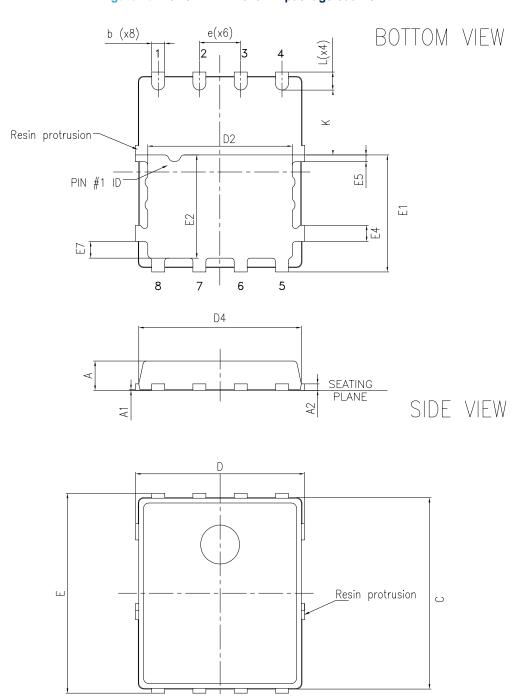
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

DS12833 - Rev 1 page 8/15



4.1 PowerFLAT™ 5x6 HV package information

Figure 19. PowerFLAT™ 5x6 HV package outline



8368143_Rev_4

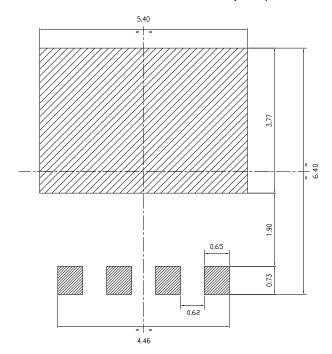
TOP VIEW



Table 8. PowerFLAT™ 5x6 HV mechanical data

Dim.		mm	
Dim.	Min.	Тур.	Max.
А	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
С	5.60	5.80	6.00
D	5.10	5.20	5.30
D2	4.30	4.40	4.50
D4	4.60	4.80	5.00
Е	6.05	6.15	6.25
E1	3.50	3.60	3.70
E2	3.10	3.20	3.30
E4	0.40	0.50	0.60
E5	0.10	0.20	0.30
E7	0.40	0.50	0.60
е		1.27	
L	0.50	0.55	0.60
К	1.90	2.00	2.10

Figure 20. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



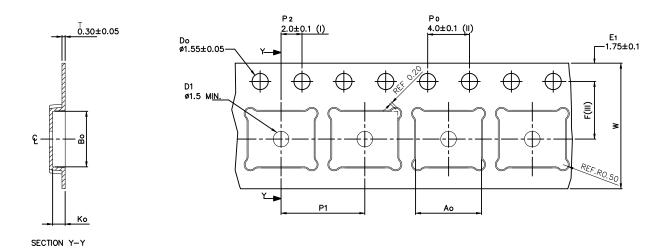
8368143_Rev_4_footprint

DS12833 - Rev 1 page 10/15



4.2 PowerFLAT™ 5x6 packing information

Figure 21. PowerFLAT™ 5x6 tape (dimensions are in mm)



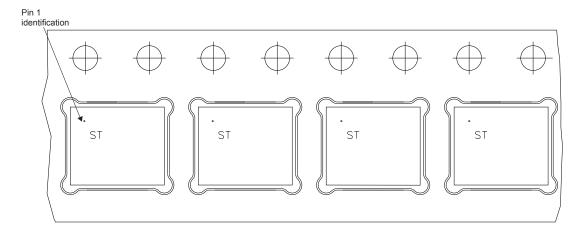
Ao	6.30 +/- 0.1
Во	5.30 +/- 0.1
Ko	1.20 +/- 0.1
F	5.50 +/- 0.1
P1	8.00 +/- 0.1
l w	12.00 +/- 0.3

- (I) Measured from centreline of sprocket hole to centreline of pocket.
- (II) Cumulative tolerance of 10 sprocket holes is ±0.20.
- (III) Measured from centreline of sprocket hole to centreline of pocket

Base and bulk quantity 3000 pcs All dimensions are in millimeters

8234350_Tape_rev_C

Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



DS12833 - Rev 1 page 11/15



PART NO

R25.00

R25.00

R25.00

R25.00

R1.10

R25.00

R1.10

R1.10

R1.10

R25.00

R25.0

Figure 23. PowerFLAT™ 5x6 reel

8234350_Reel_rev_C



Revision history

Table 9. Document revision history

Date	Version	Changes
16-Nov-2018	1	First release.

DS12833 - Rev 1 page 13/15





Contents

1	Elec	trical ratings	2
2	Electrical characteristics		
		Electrical characteristics (curves)	
3	Test	circuits	7
4	Package information		8
	4.1	PowerFLAT™ 5x6 HV package information	8
	4.2	PowerFLAT™ 5x6 packing information	10
Rev	Revision history		



IMPORTANT NOTICE - PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics - All rights reserved

DS12833 - Rev 1 page 15/15