

# 2N5190, 2N5191, 2N5192

## Silicon NPN Power Transistors

Silicon NPN power transistors are for use in power amplifier and switching circuits, — excellent safe area limits. Complement to PNP 2N5194, 2N5195.

### Features

- ESD Ratings: Machine Model, C; > 400 V  
Human Body Model, 3B; > 8000 V
- Epoxy Meets UL 94 V-0 @ 0.125 in.
- Pb-Free Packages are Available\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CE0}$	40 60 80	Vdc
Collector-Base Voltage	$V_{CBO}$	40 60 80	Vdc
Emitter-Base Voltage	$V_{EBO}$	5.0	Vdc
Collector Current	$I_C$	4.0	Adc
Base Current	$I_B$	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	40 320	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.12	$^\circ\text{C}/\text{W}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

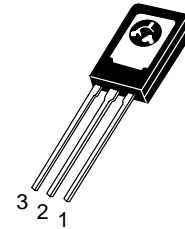
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



**ON Semiconductor®**

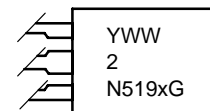
<http://onsemi.com>

**4.0 AMPERES  
NPN SILICON  
POWER TRANSISTORS  
40, 60, 80 VOLTS – 40 WATTS**



TO-225AA  
CASE 77  
STYLE 1

### MARKING DIAGRAM



Y = Year  
WW = Work Week  
2N519x = Device Code  
x = 0, 1, or 2  
G = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
2N5190	TO-225AA	500 Units/Box
2N5190G	TO-225AA (Pb-Free)	500 Units/Box
2N5191	TO-225AA	500 Units/Box
2N5191G	TO-225AA (Pb-Free)	500 Units/Box
2N5192	TO-225AA	500 Units/Box
2N5192G	TO-225AA (Pb-Free)	500 Units/Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## 2N5190, 2N5191, 2N5192

### ELECTRICAL CHARACTERISTICS\* ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
<b>OFF CHARACTERISTICS</b>				
Collector–Emitter Sustaining Voltage (Note 1) ( $I_C = 0.1\text{ A dc}$ , $I_B = 0$ )	2N5190 2N5191 2N5192	$V_{CEO(sus)}$	40 60 80	– – – Vdc
Collector Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 60\text{ Vdc}$ , $I_B = 0$ ) ( $V_{CE} = 80\text{ Vdc}$ , $I_B = 0$ )	2N5190 2N5191 2N5192	$I_{CEO}$	– – –	1.0 1.0 1.0 mAdc
Collector Cutoff Current ( $V_{CE} = 40\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ ) ( $V_{CE} = 40\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 60\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ ) ( $V_{CE} = 80\text{ Vdc}$ , $V_{EB(off)} = 1.5\text{ Vdc}$ , $T_C = 125^\circ\text{C}$ )	2N5190 2N5191 2N5192 2N5190 2N5191 2N5192	$I_{CEX}$	– – – – – –	0.1 0.1 0.1 2.0 2.0 2.0 mAdc
Collector Cutoff Current ( $V_{CB} = 40\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 60\text{ Vdc}$ , $I_E = 0$ ) ( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ )	2N5190 2N5191 2N5192	$I_{CBO}$	– – –	0.1 0.1 0.1 mAdc
Emitter Cutoff Current ( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )		$I_{EBO}$	–	1.0 mAdc
<b>ON CHARACTERISTICS (Note 1)</b>				
DC Current Gain ( $I_C = 1.5\text{ A dc}$ , $V_{CE} = 2.0\text{ Vdc}$ )  ( $I_C = 4.0\text{ A dc}$ , $V_{CE} = 2.0\text{ Vdc}$ )	2N5190/2N5191 2N5192 2N5190/2N5191 2N5192	$h_{FE}$	25 20 10 7.0	100 80 – – –
Collector–Emitter Saturation Voltage ( $I_C = 1.5\text{ A dc}$ , $I_B = 0.15\text{ A dc}$ ) ( $I_C = 4.0\text{ A dc}$ , $I_B = 1.0\text{ A dc}$ )		$V_{CE(sat)}$	– –	0.6 1.4 Vdc
Base–Emitter On Voltage ( $I_C = 1.5\text{ A dc}$ , $V_{CE} = 2.0\text{ Vdc}$ )		$V_{BE(on)}$	–	1.2 Vdc
<b>DYNAMIC CHARACTERISTICS</b>				
Current–Gain — Bandwidth Product ( $I_C = 1.0\text{ A dc}$ , $V_{CE} = 10\text{ Vdc}$ , $f = 1.0\text{ MHz}$ )		$f_T$	2.0	– MHz

\*JEDEC Registered Data.

1. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

# 2N5190, 2N5191, 2N5192

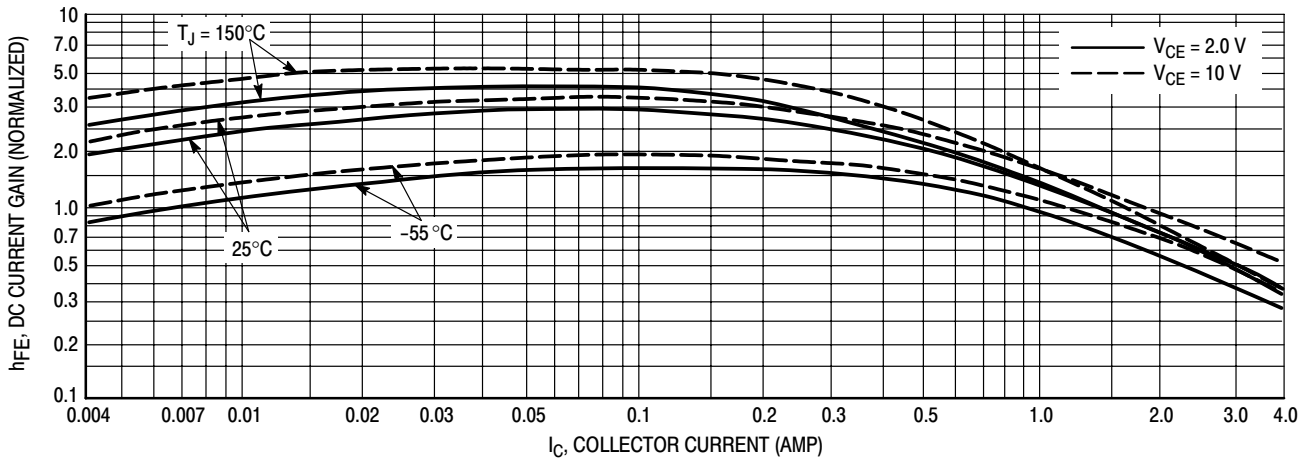


Figure 1. DC Current Gain

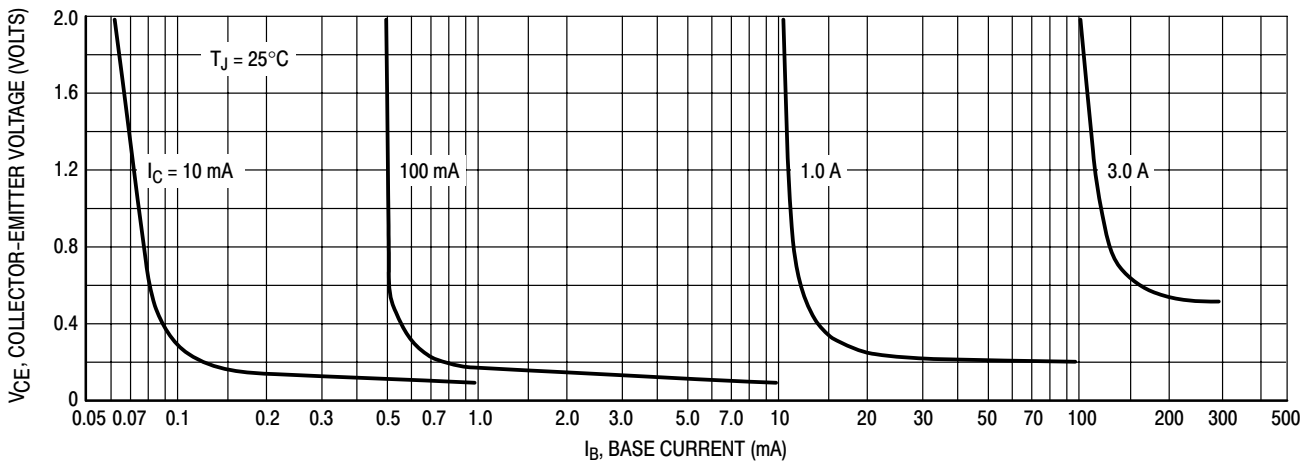


Figure 2. Collector Saturation Region

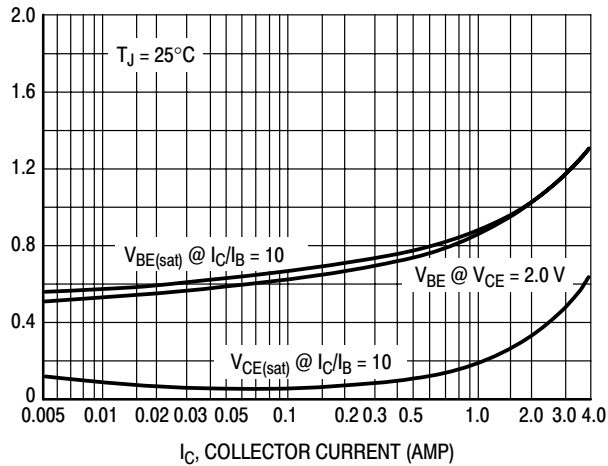


Figure 3. "On" Voltages

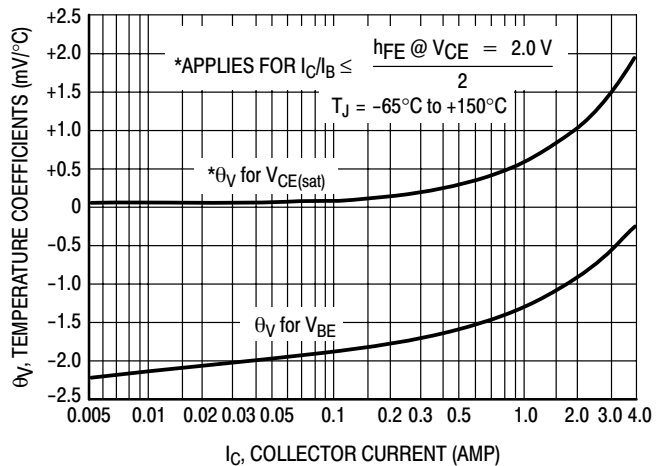


Figure 4. Temperature Coefficients

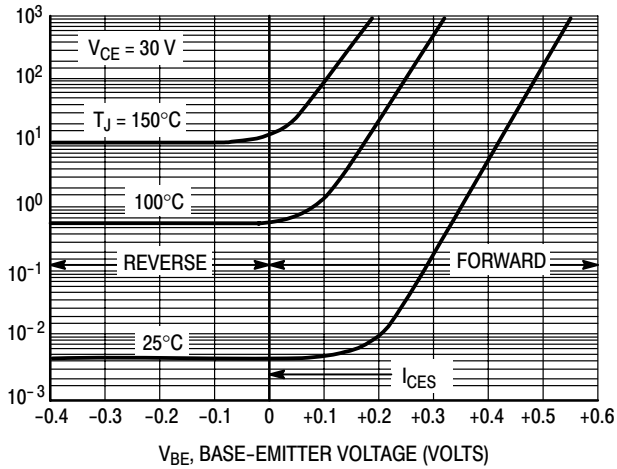


Figure 5. Collector Cut-Off Region

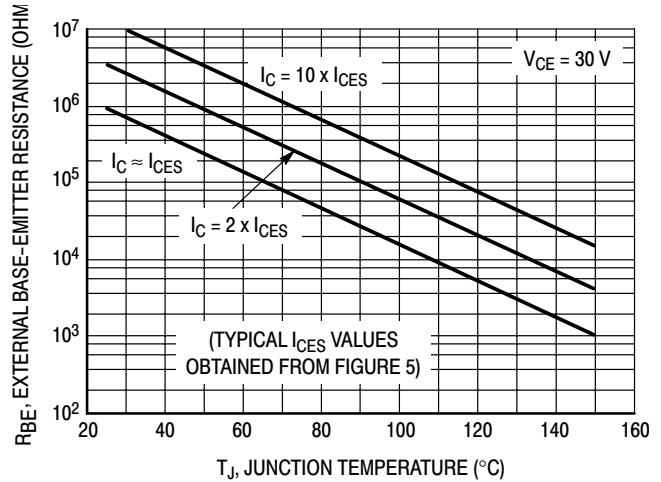


Figure 6. Effects of Base-Emitter Resistance

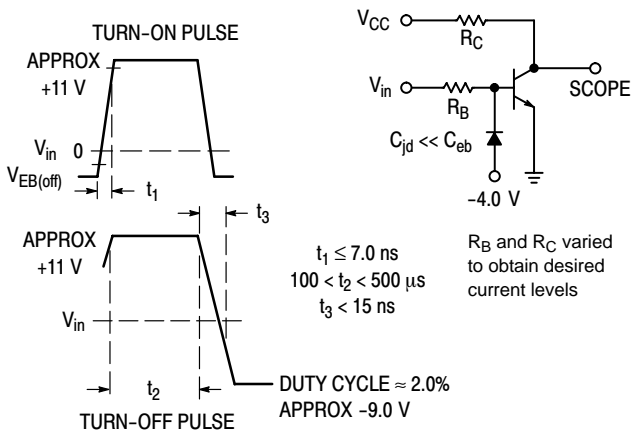


Figure 7. Switching Time Equivalent Test Circuit

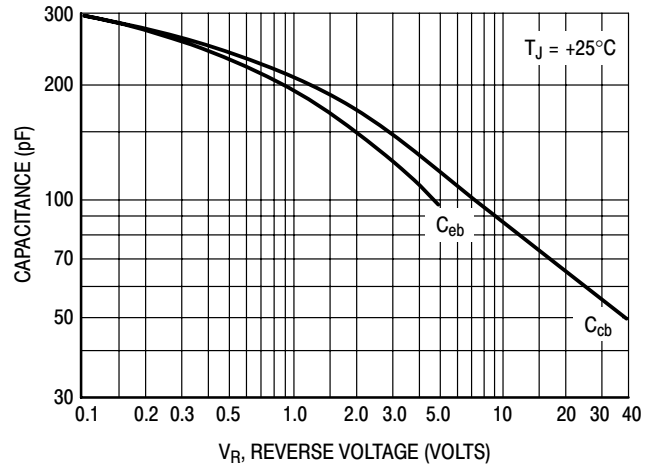


Figure 8. Capacitance

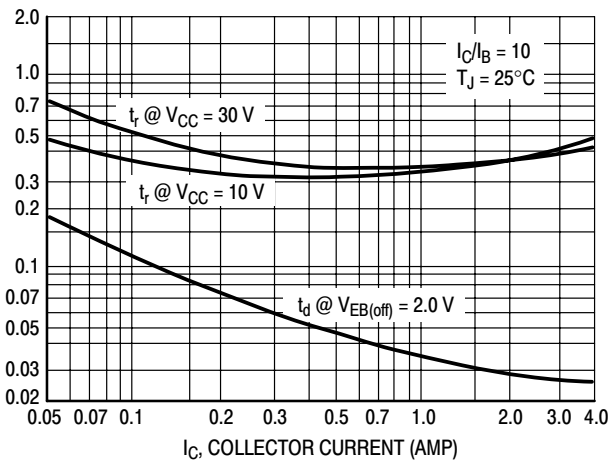


Figure 9. Turn-On Time

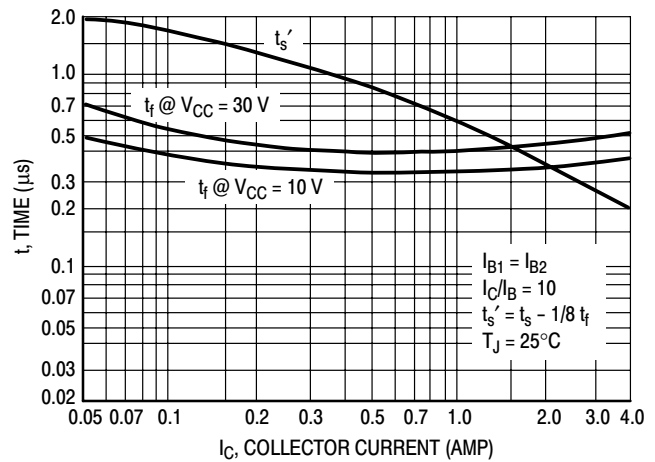
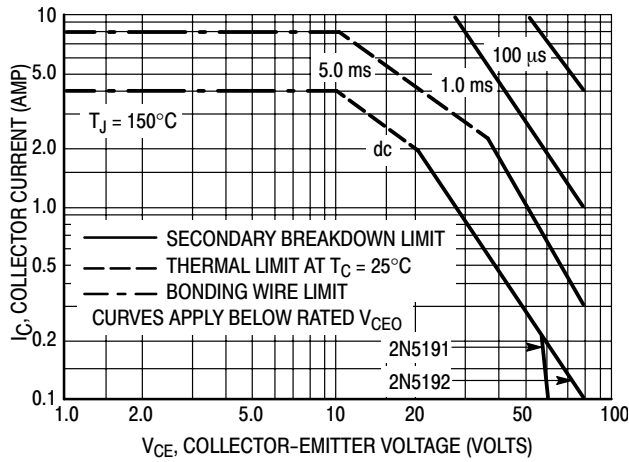


Figure 10. Turn-Off Time

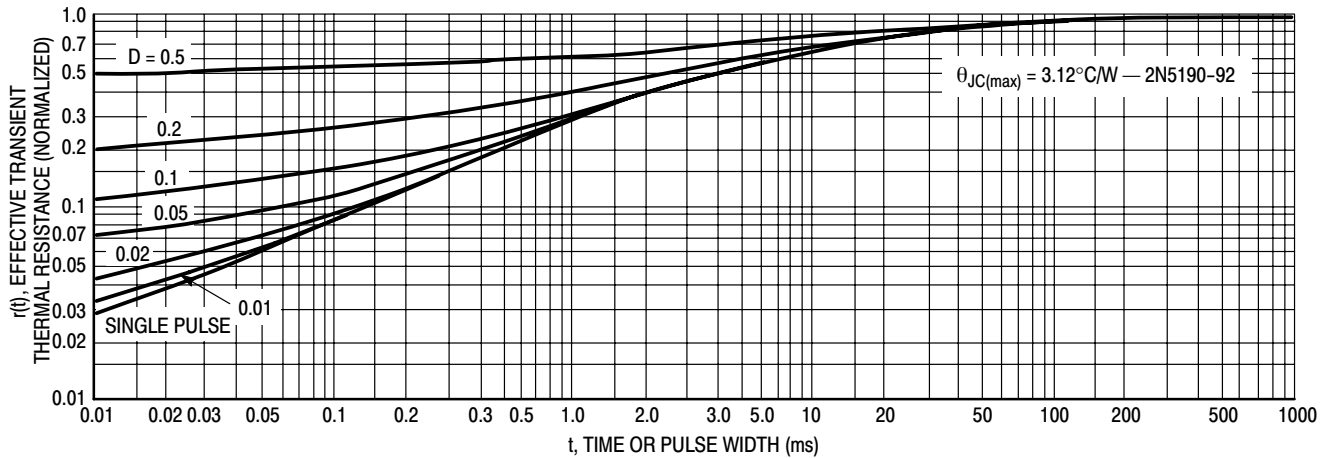
## 2N5190, 2N5191, 2N5192



**Figure 11. Rating and Thermal Data  
Active-Region Safe Operating Area**

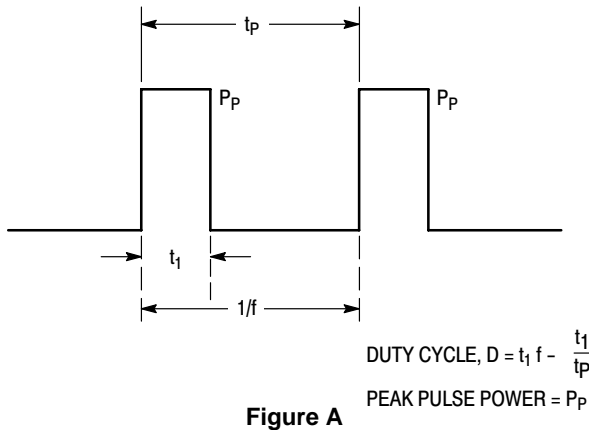
There are two limitations on the power handling ability of a transistor; average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on  $T_{J(pk)} = 150^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^\circ\text{C}$ . At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



**Figure 12. Thermal Response**

### DESIGN NOTE: USE OF TRANSIENT THERMAL RESISTANCE DATA



**Figure A**

A train of periodical power pulses can be represented by the model shown in Figure A. Using the model and the device thermal response, the normalized effective transient thermal resistance of Figure 12 was calculated for various duty cycles.

To find  $\theta_{JC}(t)$ , multiply the value obtained from Figure 12 by the steady state value  $\theta_{JC}$ .

Example:

The 2N5190 is dissipating 50 watts under the following conditions:  $t_1 = 0.1$  ms,  $t_p = 0.5$  ms. ( $D = 0.2$ ).

Using Figure 12, at a pulse width of 0.1 ms and  $D = 0.2$ , the reading of  $r(t_1, D)$  is 0.27.

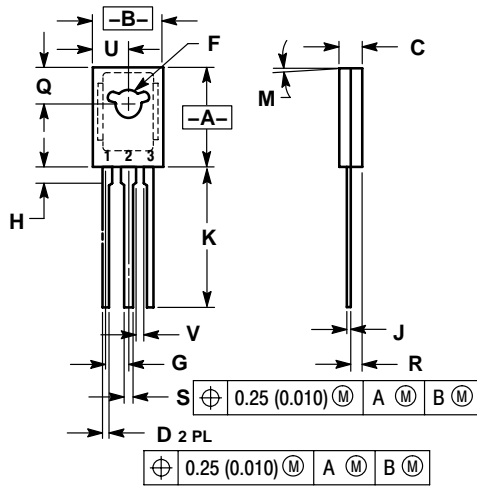
The peak rise in function temperature is therefore:

$$\Delta T = r(t) \times P_p \times \theta_{JC} = 0.27 \times 50 \times 3.12 = 42.2^\circ\text{C}$$

# 2N5190, 2N5191, 2N5192

## PACKAGE DIMENSIONS

TO-225AA  
CASE 77-09  
ISSUE Z



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 077-01 THRU -08 OBSOLETE, NEW STANDARD 077-09.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.425	0.435	10.80	11.04
B	0.295	0.305	7.50	7.74
C	0.095	0.105	2.42	2.66
D	0.020	0.026	0.51	0.66
F	0.115	0.130	2.93	3.30
G	0.094 BSC		2.39 BSC	
H	0.050	0.095	1.27	2.41
J	0.015	0.025	0.39	0.63
K	0.575	0.655	14.61	16.63
M	5° TYP		5° TYP	
Q	0.148	0.158	3.76	4.01
R	0.045	0.065	1.15	1.65
S	0.025	0.035	0.64	0.88
U	0.145	0.155	3.69	3.93
V	0.040	---	1.02	---

### STYLE 1:

1. EMITTER
2. COLLECTOR
3. BASE

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85062-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.

2N5191/D