



## PD84001-E

RF power transistor  
The LdmoST plastic family

Preliminary Data

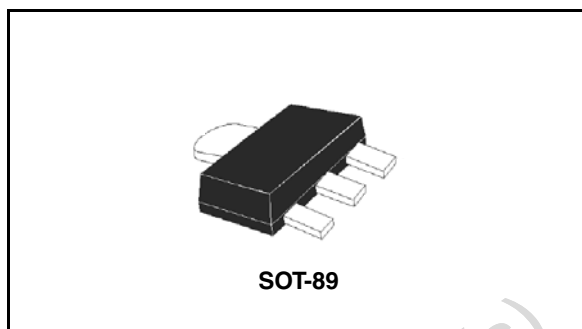
### General features

- Excellent thermal stability
- Common source configuration
- Broadband performances  $P_{OUT} = 1W$  with 15dB gain @ 870MHz
- Plastic package
- ESD protection
- Supplied in tape and reel
- In compliance with the 2002/93/EC european directive

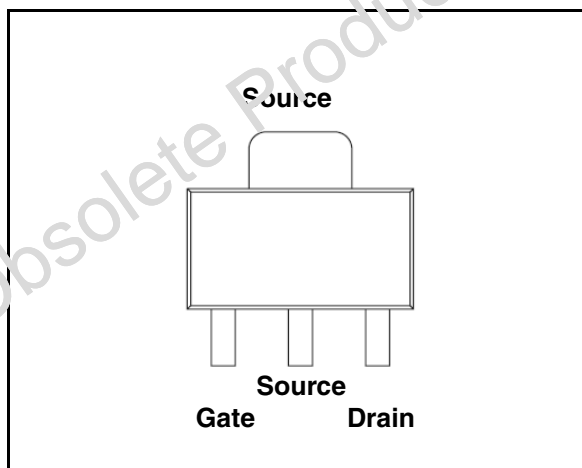
### Description

The PD84001-E is a common source N-Channel, enhancement-mode lateral Field-Effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 7V in common source mode at frequencies of up to 1GHz.

PD84001-E's superior gain and efficiency makes it an ideal solution for portable radio and UHF RFID reader.



### Pin connection



### Order codes

Part number	Marking	Package	Packaging
PD84001-E	84001	SOT-89	Tape and reel

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# 1 Electrical data

## 1.1 Maximum ratings

Table 1. Absolute maximum ratings ( $T_{CASE} = +25^{\circ}C$ )

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	25	V
$V_{GS}$	Gate-source voltage	-0.5 to +15	V
$I_D$	Drain current	1.5	A
$P_{DISS}$	Power dissipation	6	W
$T_J$	Max. operating junction temperature	150	$^{\circ}C$
$T_{STG}$	Storage temperature	-65 to +150	$^{\circ}C$

## 1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}$	Junction - case thermal resistance	21	$^{\circ}C/W$

## 2 Electrical characteristics

### 2.1 Static

**Table 3. Static**  $T_{CASE} = +25\text{ }^{\circ}\text{C}$

Symbol	Test conditions			Min.	Typ.	Max.	Unit
$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 28\text{ V}$				1	$\mu\text{A}$
$I_{GSS}$	$V_{GS} = 15\text{ V}$	$V_{DS} = 0\text{ V}$				1	$\mu\text{A}$
$V_{GS(Q)}$	$V_{DS} = 10\text{ V}$	$I_D = 250\text{ }\mu\text{A}$		2.0	3.0	5.0	V
$V_{DS(ON)}$	$V_{GS} = 10\text{ V}$	$I_D = 0.4\text{ A}$			0.5		V
$C_{ISS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 7\text{ V}$	$f = 1\text{ MHz}$		14.7		pF
$C_{OSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 7\text{ V}$	$f = 1\text{ MHz}$		13.3		pF
$C_{RSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 7\text{ V}$	$f = 1\text{ MHz}$		1.3		pF

### 2.2 Dynamic

**Table 4. Dynamic**

Symbol	Test conditions	Min.	Typ.	Max.	Unit
$P_{OUT}$	$V_{DD} = 7.5\text{ V}$ , $I_{DQ} = 50\text{ mA}$ , $P_{IN} = 17\text{ dBm}$ , $f = 870\text{ MHz}$	30	31		dBm
$G_{PS}$	$V_{DD} = 7.5\text{ V}$ , $I_{DQ} = 50\text{ mA}$ , $P_{OUT} = 30\text{ dBm}$ , $f = 870\text{ MHz}$	13	15		dB
$h_D$	$V_{DD} = 7.5\text{ V}$ , $I_{DQ} = 50\text{ mA}$ , $P_{IN} = 17\text{ dBm}$ , $f = 870\text{ MHz}$	55	60		%
Load mismatch	$V_{DD} = 7.5\text{ V}$ , $I_{DQ} = 50\text{ mA}$ , $P_{OUT} = 1\text{ W}$ , $f = 870\text{ MHz}$ All phase angles	20:1			VSWR

### 2.3 ESD protection characteristics

**Table 5. ESD protection characteristics**

Test conditions	Class
Human body model	2
Machine model	M3

### 2.4 Moisture sensitivity level

**Table 6. Moisture sensitivity level**

Test methodology	Rating
J-STD-020B	MSL 3

### 3 Impedance

Figure 1. Current conventions

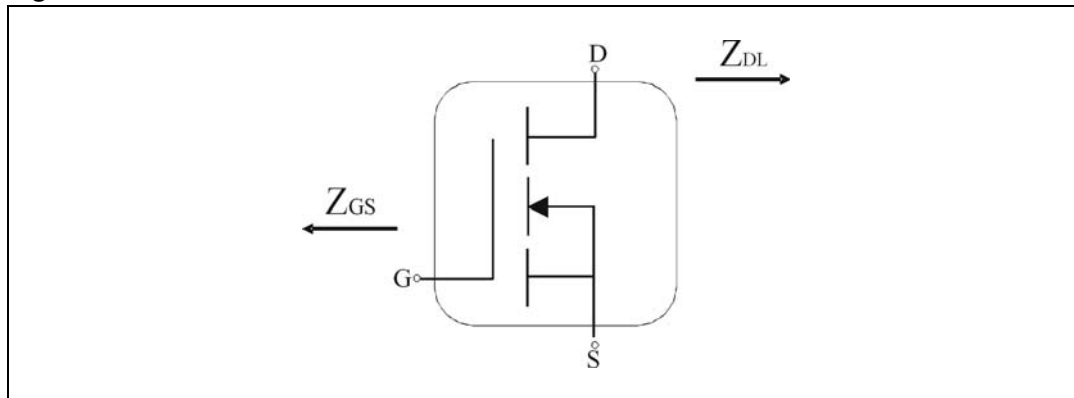


Table 7. Impedance data

Freq. (MHz)	$Z_{GS} (\Omega)$	$Z_{DL} (\Omega)$
920	$4.0 + j4.3$	$3.7 + j6.2$
900	$3.6 + j4.3$	$3.9 + j5.5$
880	$3.3 + j4.1$	$4.1 + j4.7$
860	$3.1 + j3.7$	$4.3 + j4.0$
840	$2.9 + j3.4$	$4.5 + j3.2$
820	$2.8 + j3.0$	$4.8 + j2.4$
800	$2.7 + j2.5$	$5.0 + j1.6$

## 4 Typical performance

Figure 2.  $V_{GS}$  vs  $I_D$

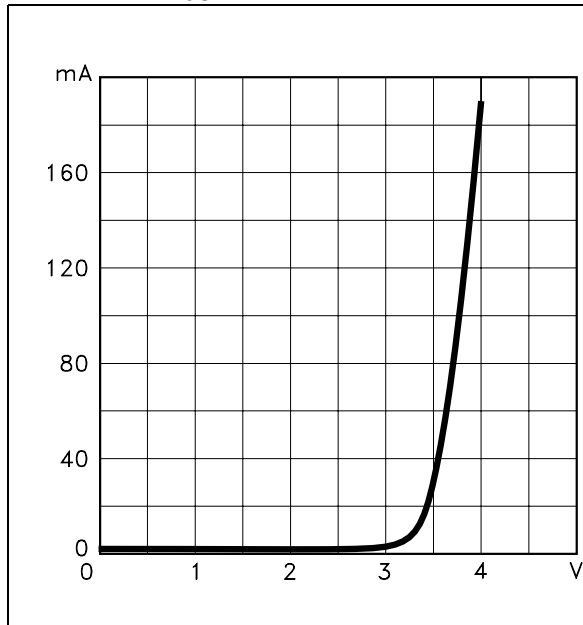
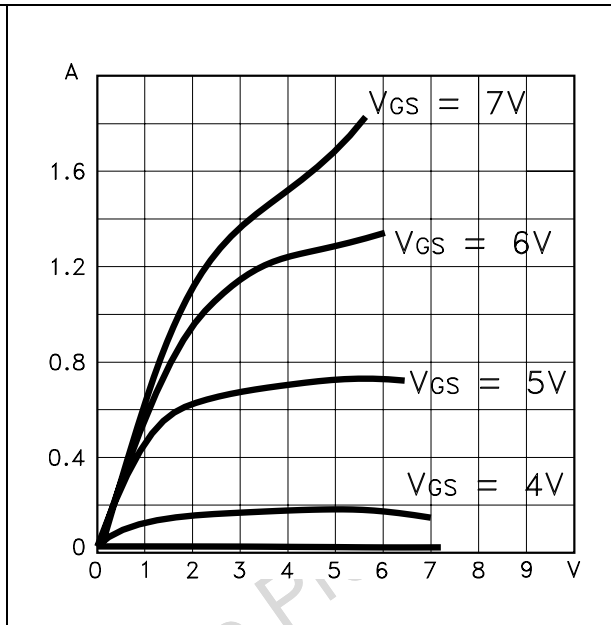


Figure 3. DC output characteristics



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Figure 4.  $C_{RSS}$  vs  $V_{DS}$

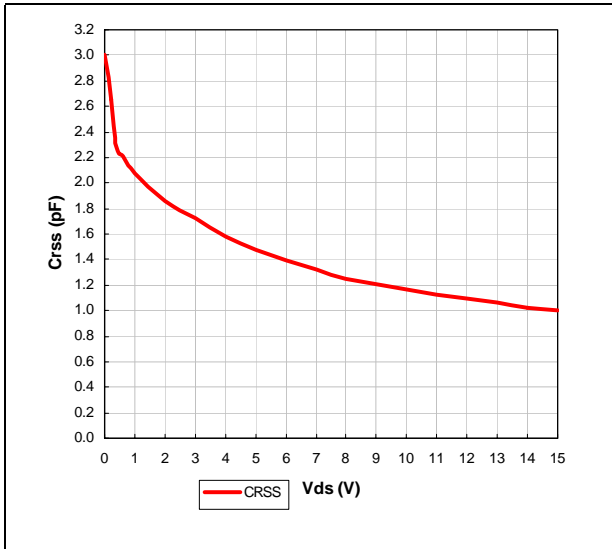


Figure 5.  $C_{ISS}$  vs  $V_{DS}$

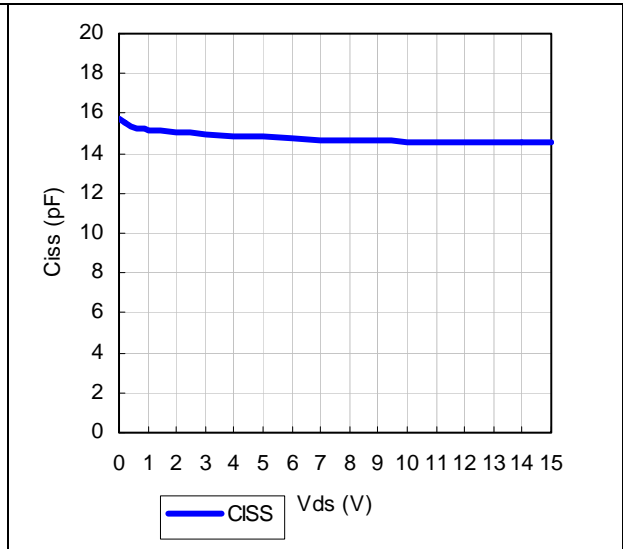


Figure 6.  $C_{OSS}$  vs  $V_{DS}$

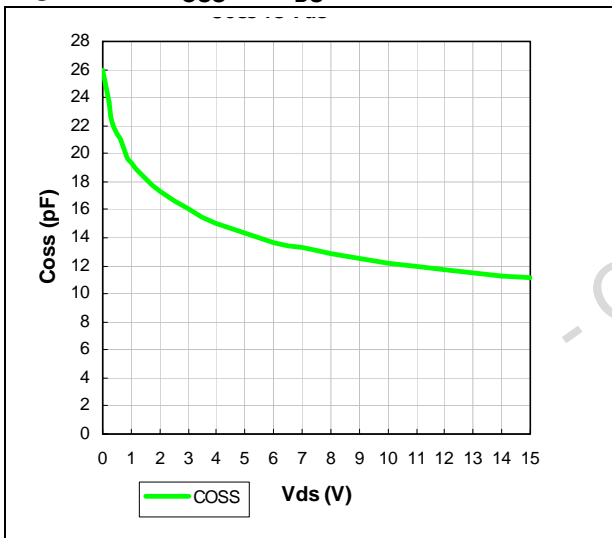


Figure 7. Gain vs output power & frequency

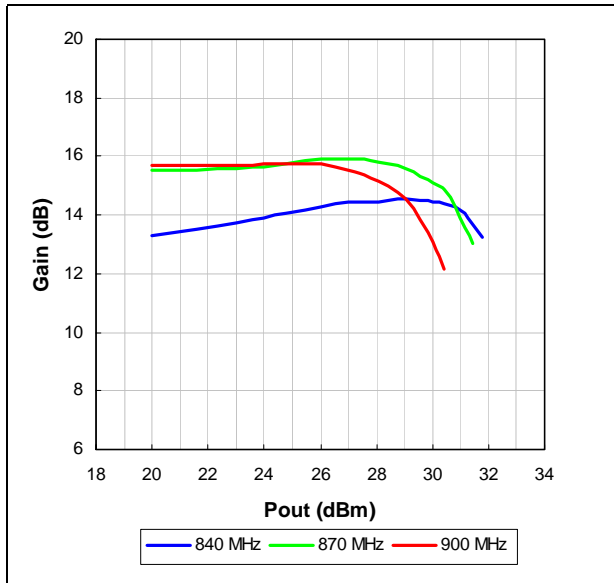


Figure 8. Output power vs input power & frequency

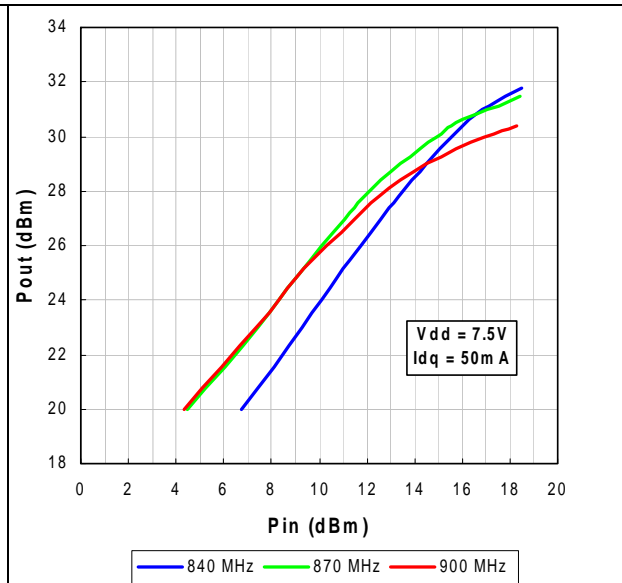


Figure 9. Efficiency vs output power & frequency

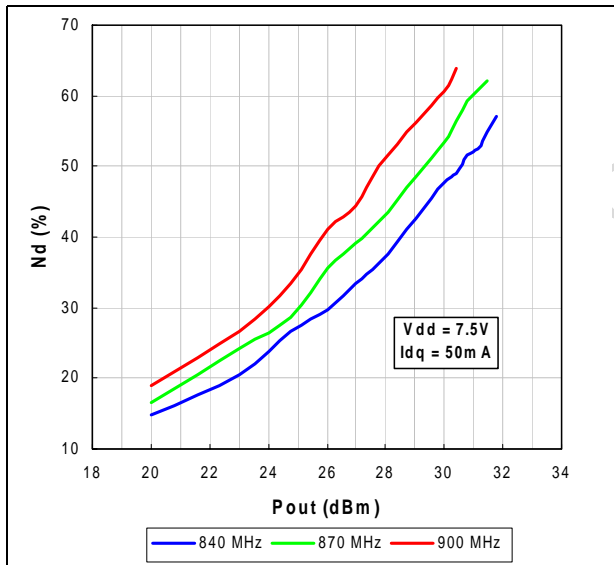


Figure 10. Gain & efficiency vs frequency

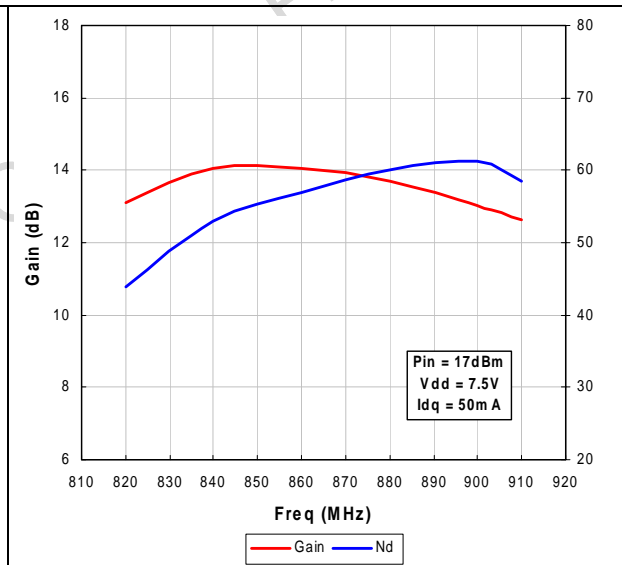




Figure 11. Input return loss vs frequency

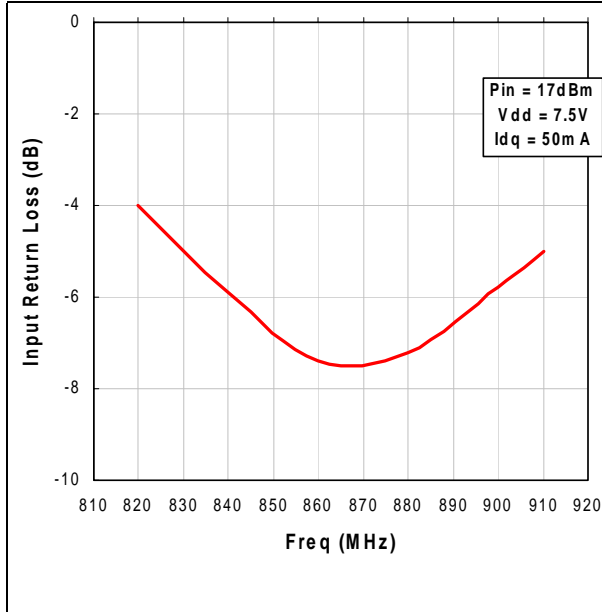


Figure 12. Output power vs input power & V<sub>DD</sub>

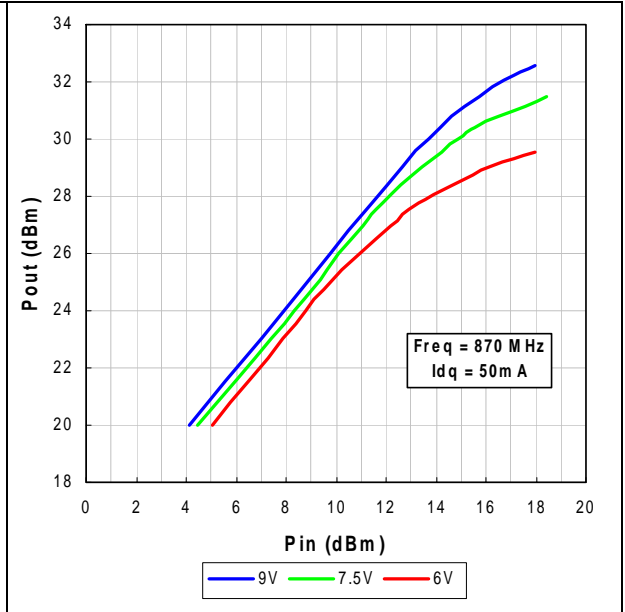


Figure 13. Efficiency vs output power & V<sub>DD</sub>

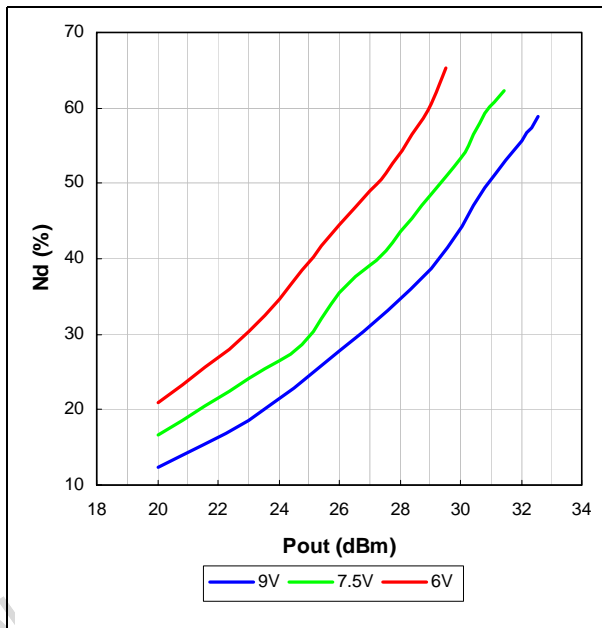


Figure 14. Output power & drain current vs drain supply voltage

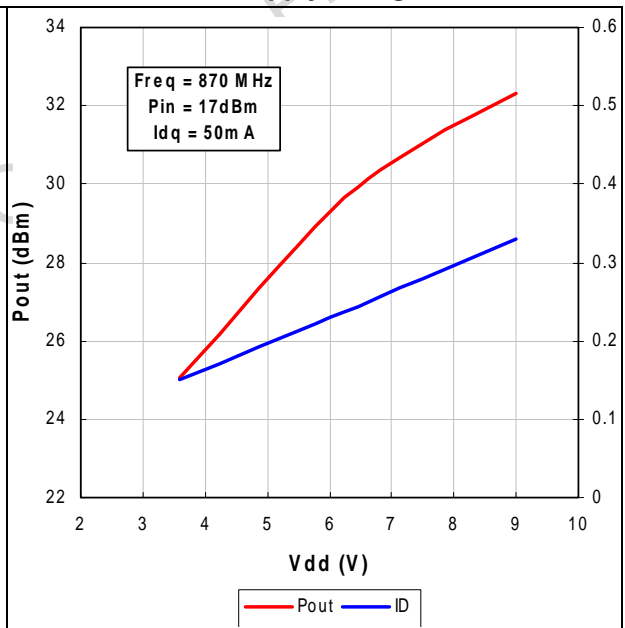
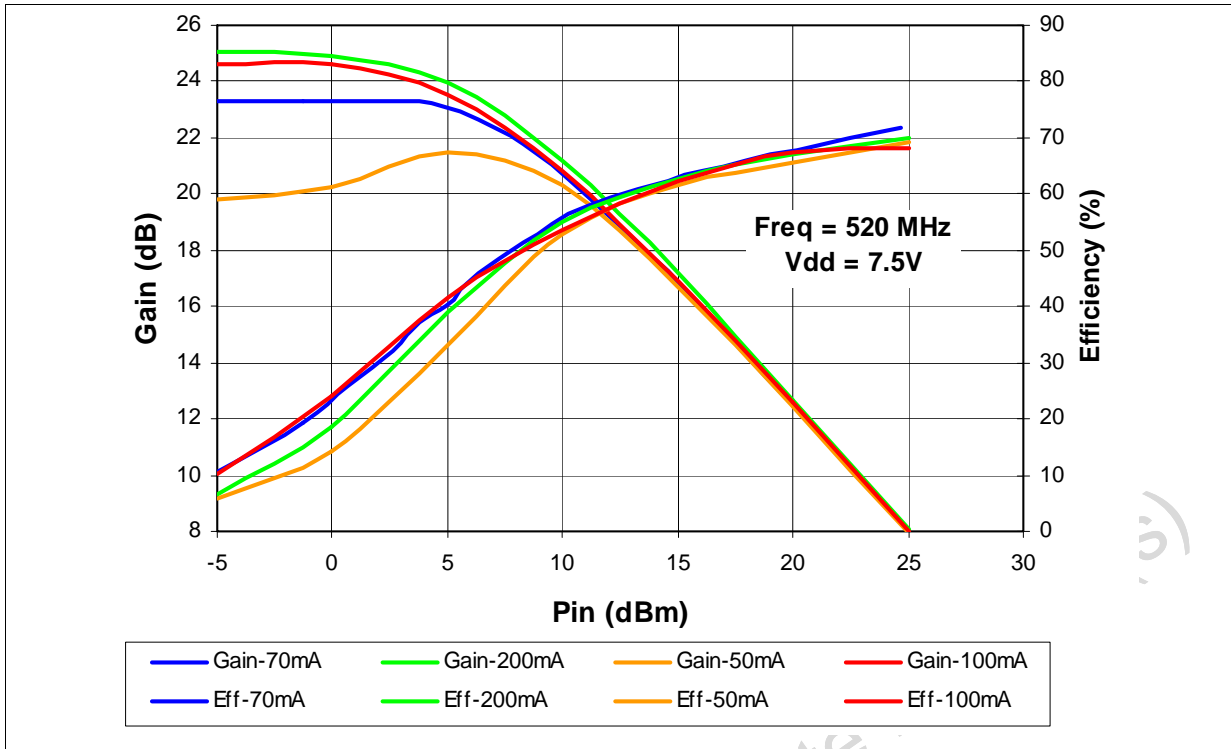


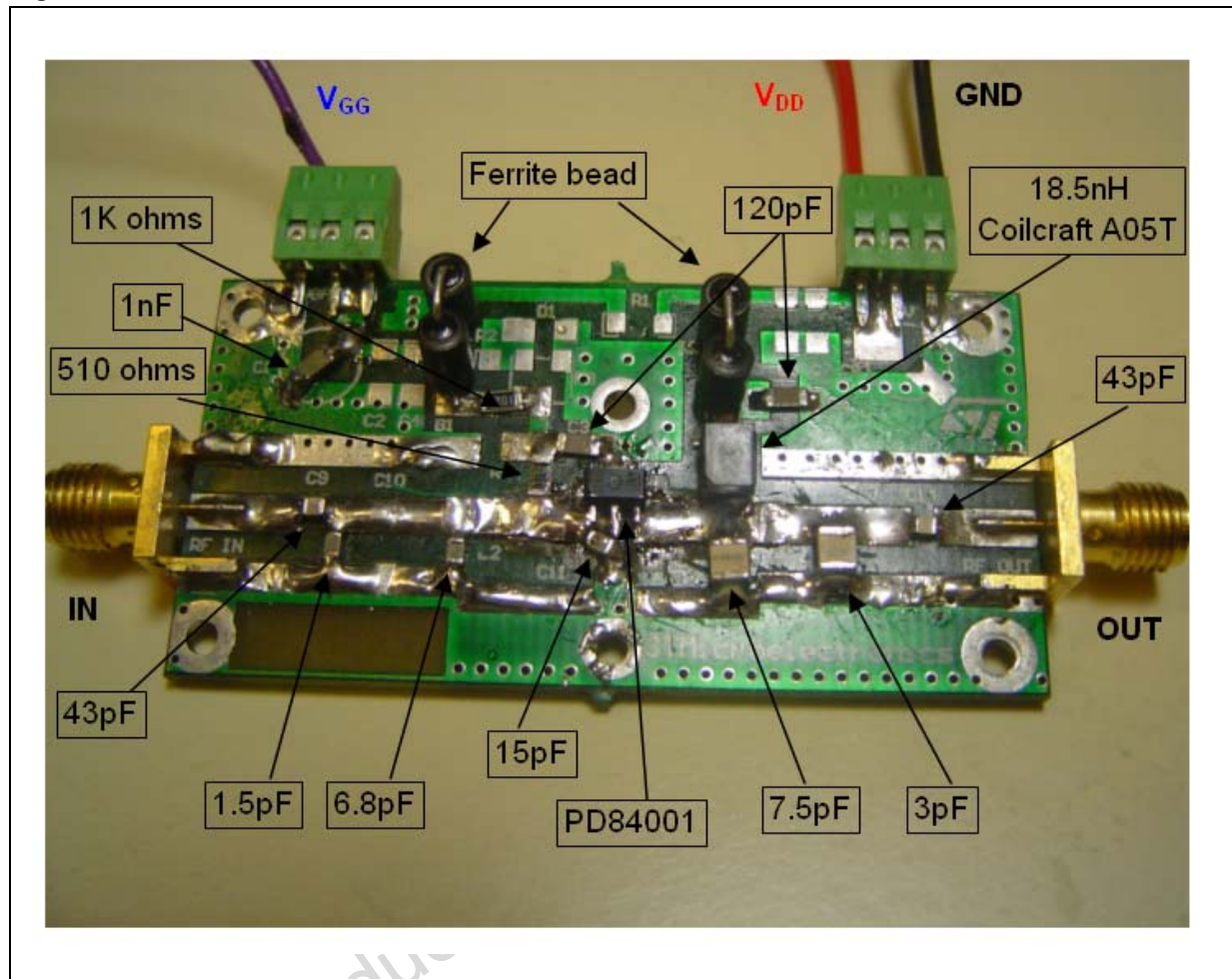
Figure 15. Gain & efficiency vs pin



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## 5 Test circuit

Figure 16. Test circuit schematic / 840-900 MHz



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## 6 Package mechanical data

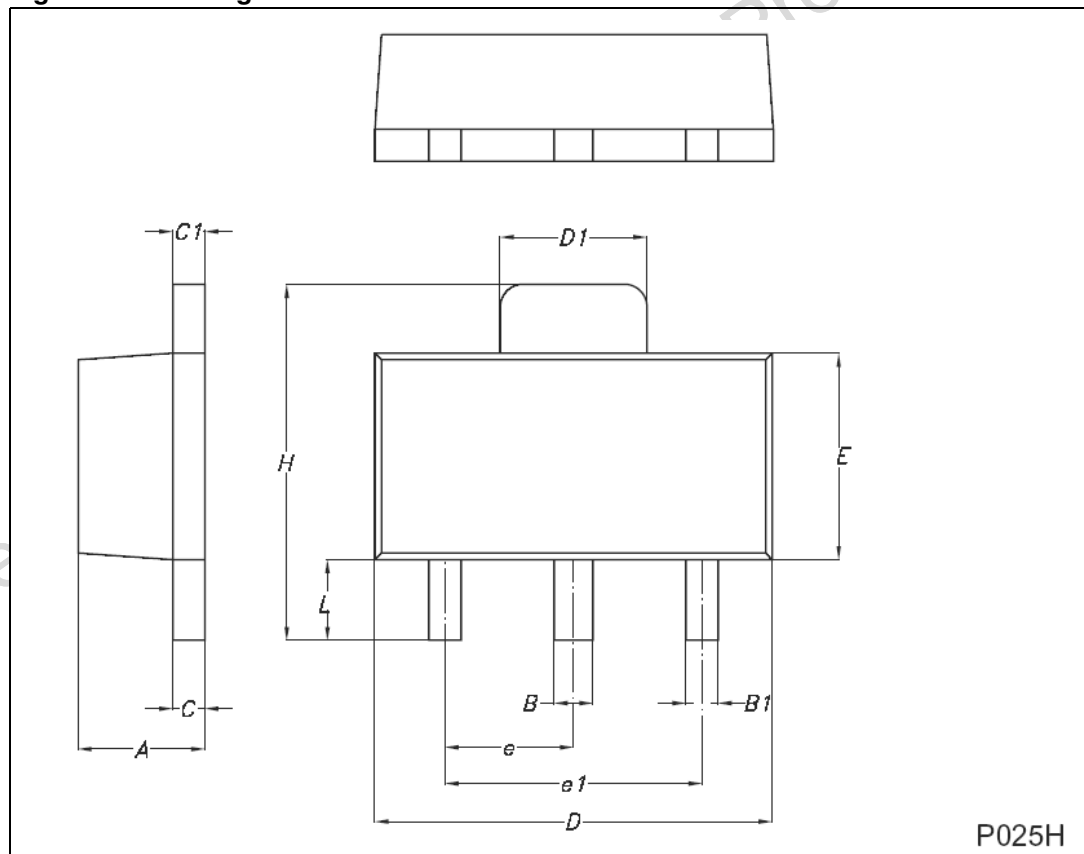
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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**Table 8. SOT-89 mechanical data**

Dim.	mm.			Inch		
	Min	Typ	Max	Min	Typ	Max
A	1.4		1.6	55.1		63.0
B	0.44		0.56	17.3		22.0
B1	0.36		0.48	14.2		18.9
C	0.35		0.44	13.8		17.3
C1	0.35		0.44	13.8		17.3
D	4.4		4.6	173.2		181.1
D1	1.62		1.83	63.8		72.0
E	2.29		2.6	90.2		102.4
e	1.42		1.57	55.9		61.8
e1	2.92		3.07	115.0		120.9
H	3.94		4.25	155.1		167.3
L	0.89		1.2	35.0		47.2

**Figure 17. Package dimensions**

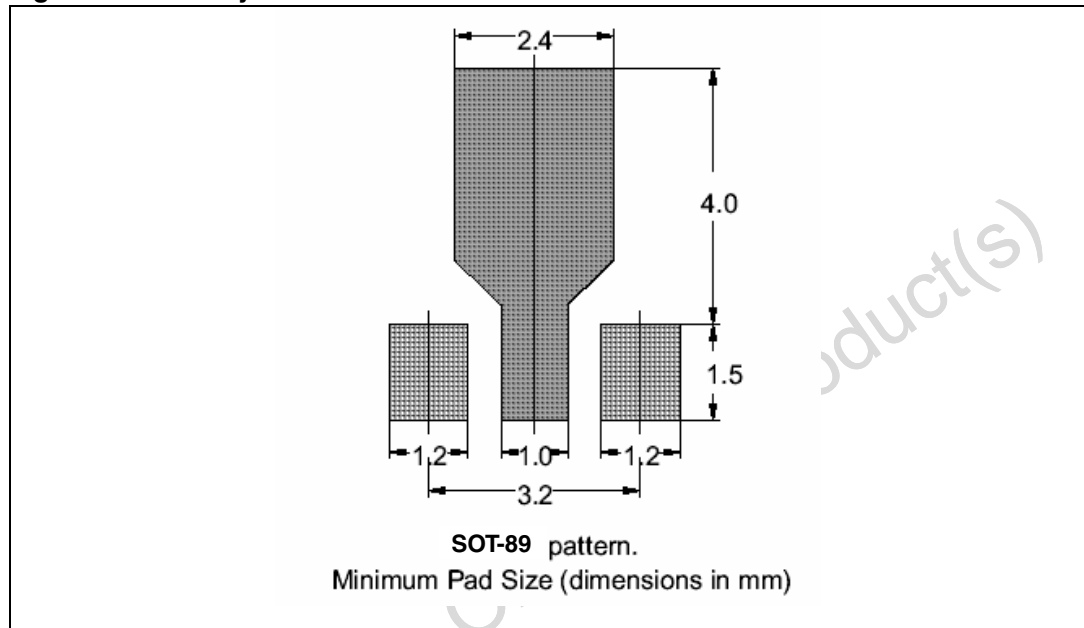


### 6.1 Thermal Pad and Via design

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device.

The via pattern is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025 plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.

Figure 18. Pad layout details



## 6.2 Soldering profile

Figure 19 shows the recommended solder for devices that have Pb-free terminal plating and where a Pb-free solder is used.

Figure 19. Recommended solder profile

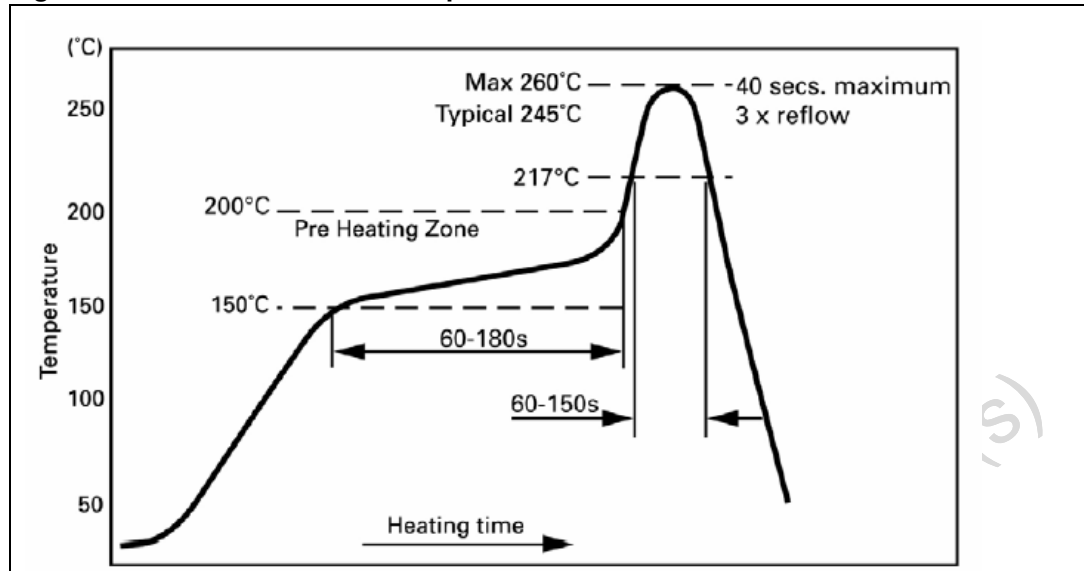


Figure 20 shows the recommended solder for devices with Pb-free terminal plating used with leaded solder, or for devices with leaded terminal plating used with a leaded solder.

Figure 20. Recommended solder profile for leaded devices

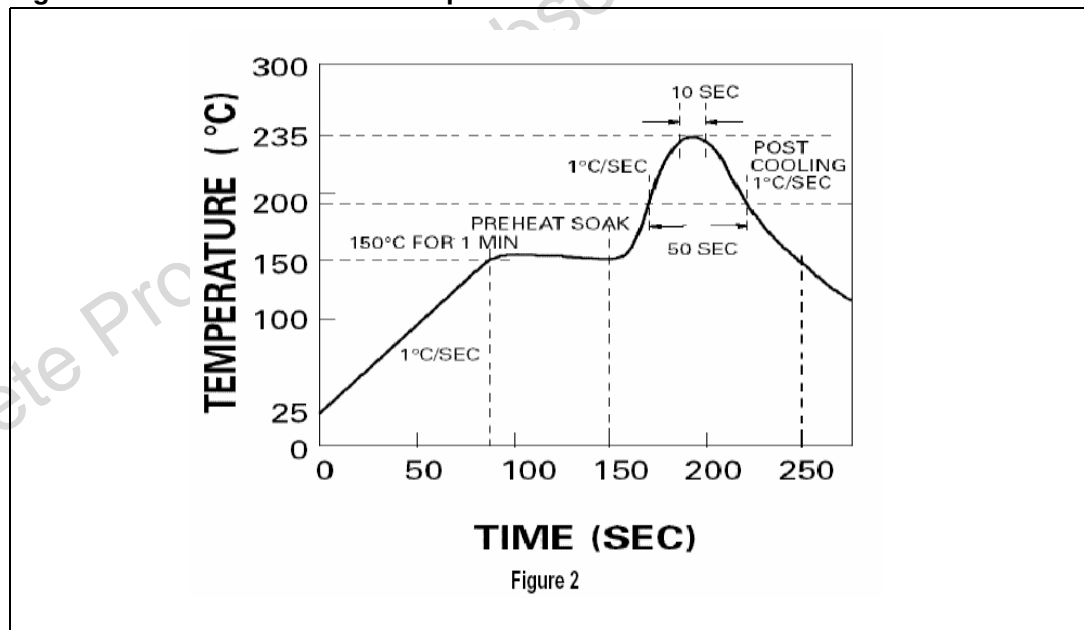
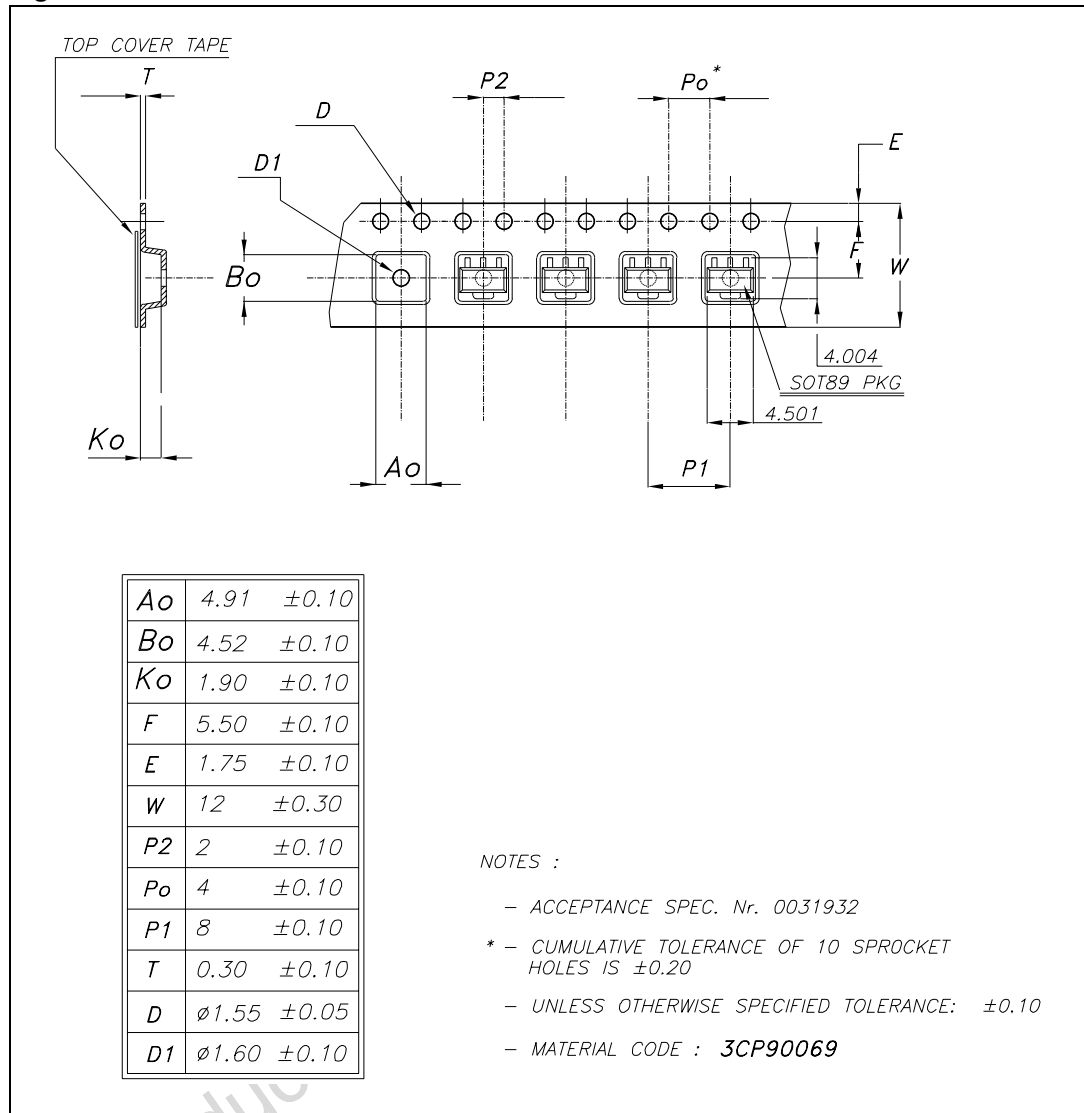


Figure 2

Figure 21. Reel information



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## 7 Revision history

**Table 9. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
02-May-2006	1	Initial release
24-Nov-2006	2	Added "-E" suffix

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