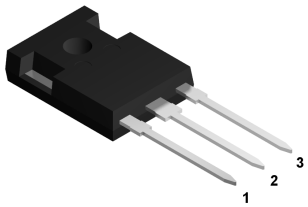
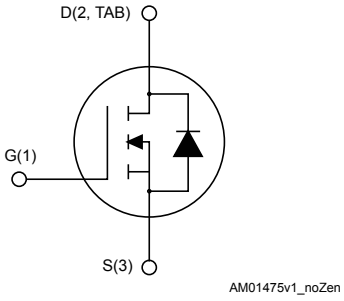
SCTWA35N65G2VAG

Datasheet

Automotive-grade silicon carbide Power MOSFET 650 V, 45 A, 55 mΩ (typ., T_J = 25 °C) in an HiP247 long leads package



HiP247 long leads



Features

Order code	V_{DS}	$R_{DS(on)}$ typ.	I_D
SCTWA35N65G2VAG	650 V	55 mΩ	45 A

- AEC-Q101 qualified
- Very fast and robust intrinsic body diode
- Low capacitance

Applications

- Switching mode power supply
- EV chargers
- DC-DC converters

Description

This silicon carbide Power MOSFET device has been developed using ST's advanced and innovative 2nd generation SiC MOSFET technology. The device features remarkably low on-resistance per unit area and very good switching performance. The variation of switching loss is almost independent of junction temperature.

Product status link
SCTWA35N65G2VAG

Product summary	
Order code	SCTWA35N65G2VAG
Marking	35N65G2VAG
Package	HiP247 long leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage (recommended operating range)	-5 to 18	
I_D	Drain current (continuous) at T_C = 25 °C	45	A
	Drain current (continuous) at T_C = 100 °C	35	
I_{DM}(1)	Drain current (pulsed)	90	A
P_{TOT}	Total power dissipation at T_C = 25 °C	240	W
T_{stg}	Storage temperature range	-55 to 200	°C
T_J	Operating junction temperature range		°C

1. *Pulse width is limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.72	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	40	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			50	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_J = 200 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = -10 to 22 V			±250	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 1 mA	1.8	3.2	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 20 V, I_D = 20 A		45	67	mΩ
		V_{GS} = 18 V, I_D = 20 A		55		
		V_{GS} = 20 V, I_D = 20 A, T_J = 200 °C		68		

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 400 V, f = 1 MHz	-	1370	-	pF
C_{oss}	Output capacitance		-	125	-	pF
C_{rss}	Reverse transfer capacitance		-	30	-	pF
R_g	Gate input resistance	f = 1 MHz, I_D = 0 A	-	2	-	Ω
Q_g	Total gate charge	V_{DD} = 400 V, I_D = 20 A, V_{GS} = 0 to 20 V	-	73	-	nC
Q_{gs}	Gate-source charge		-	14	-	nC
Q_{gd}	Gate-drain charge		-	27	-	nC

Table 5. Switching energy (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	V_{DD} = 400 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = -5 to 20 V	-	100	-	µJ
E_{off}	Turn-off switching energy		-	35	-	µJ

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 400 V, I_D = 20 A, R_G = 4.7 Ω, V_{GS} = -5 to 20 V	-	16	-	ns
t_f	Fall time		-	14	-	ns
$t_{d(off)}$	Turn-off delay time		-	35	-	ns
t_r	Rise time		-	9	-	ns

Table 7. Reverse diode characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage	V_{GS} = 0 V, I_F = 20 A,	-	3.3	-	V
t_{rr}	Reverse recovery time	V_{DD} = 400 V, I_F = 20 A, di/dt = 1000 A/µs	-	18	-	ns
Q_{rr}	Reverse recovery charge		-	85	-	nC
I_{RRM}	Reverse recovery current		-	7	-	A

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

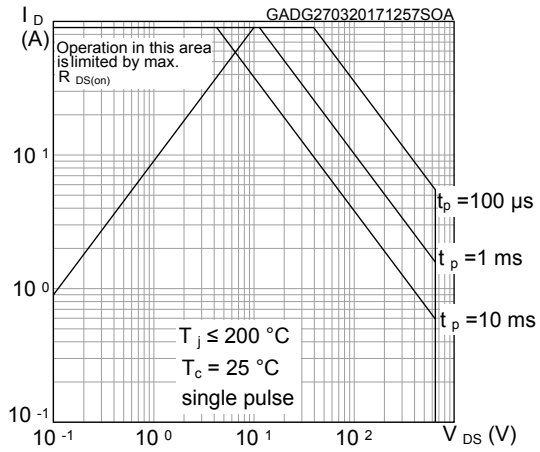


Figure 2. Thermal impedance

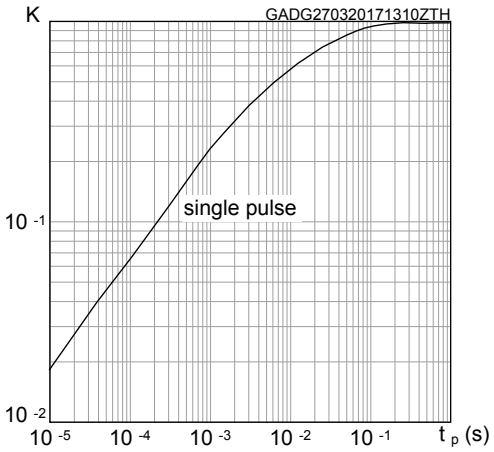


Figure 3. Output characteristics (T_J = 25 °C)

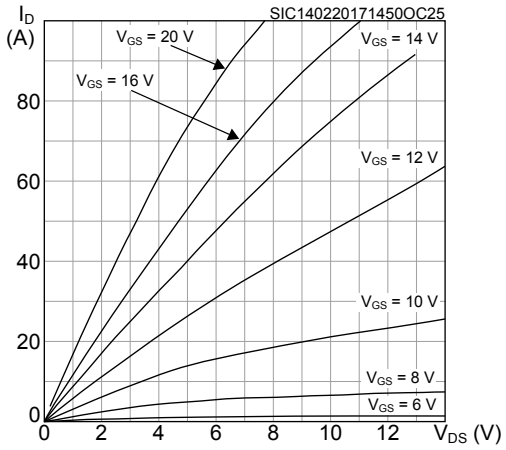


Figure 4. Output characteristics (T_J = 175 °C)

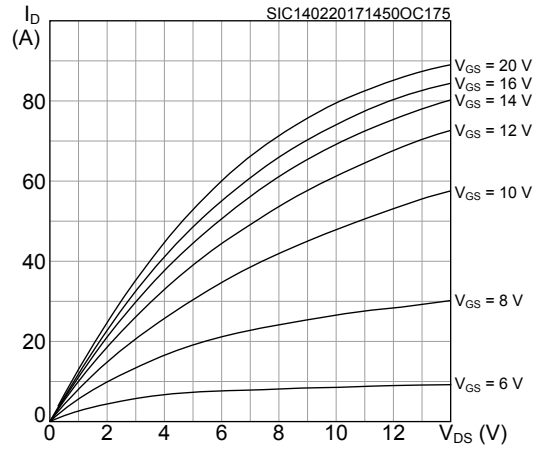


Figure 5. Transfer characteristics

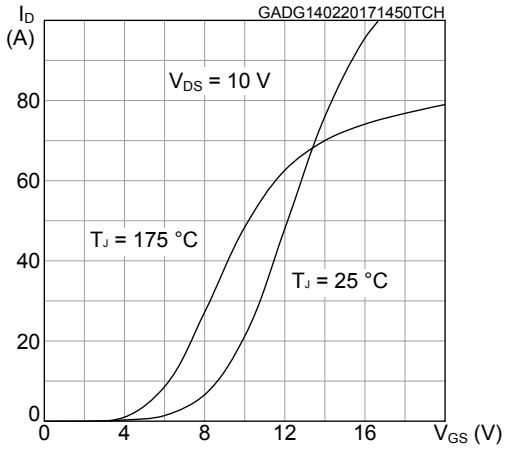


Figure 6. Power dissipation

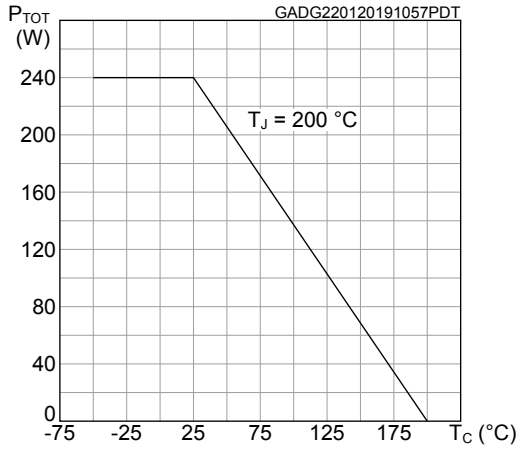


Figure 7. Gate charge vs gate-source voltage

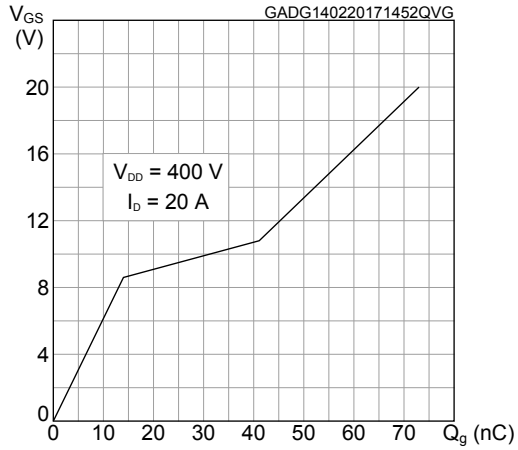


Figure 8. Capacitance variations

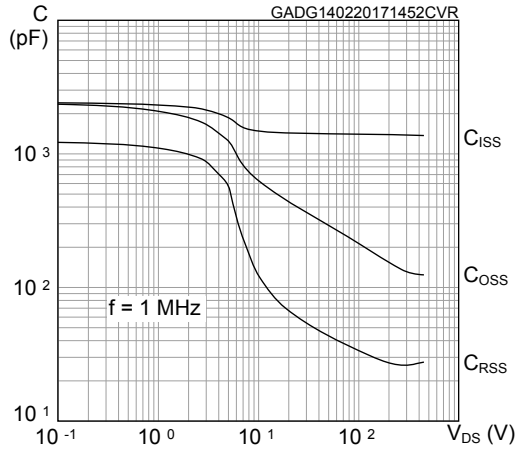


Figure 9. Switching energy vs drain current

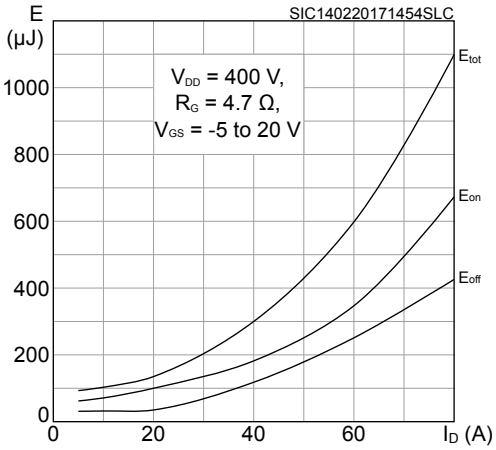


Figure 10. Switching energy vs junction temperature

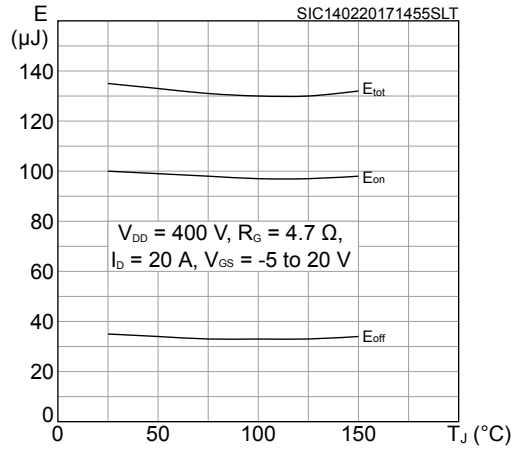


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

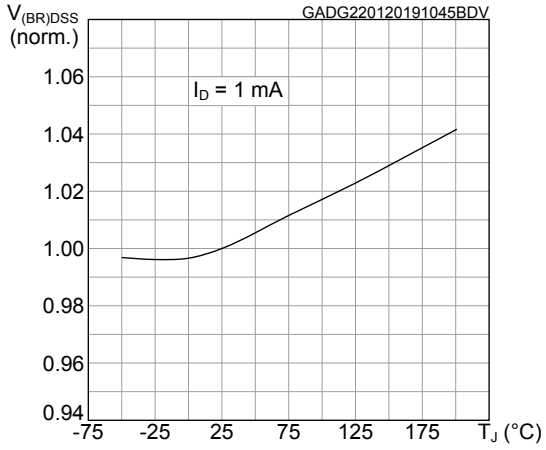


Figure 12. Normalized gate threshold voltage vs temperature

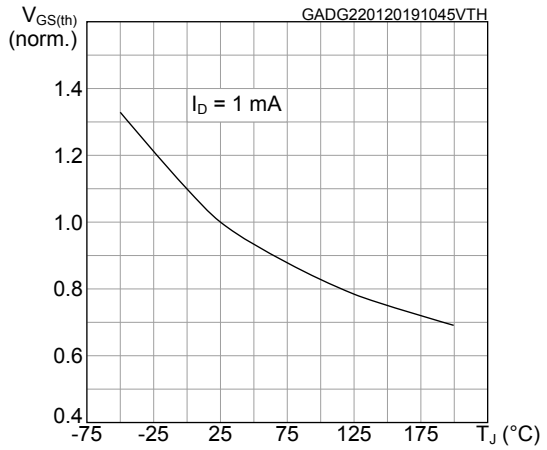


Figure 13. Normalized on-resistance vs temperature

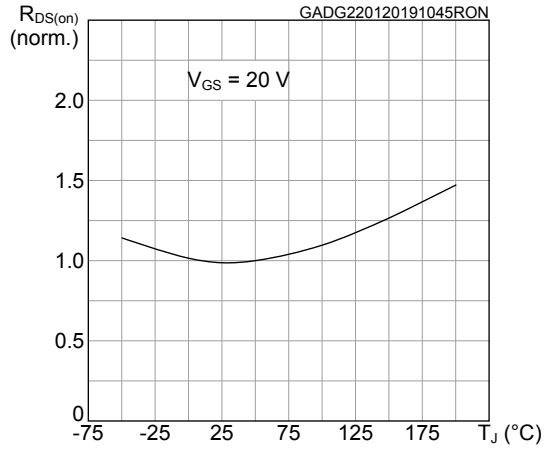


Figure 14. Reverse conduction characteristics (T_J = 25 °C)

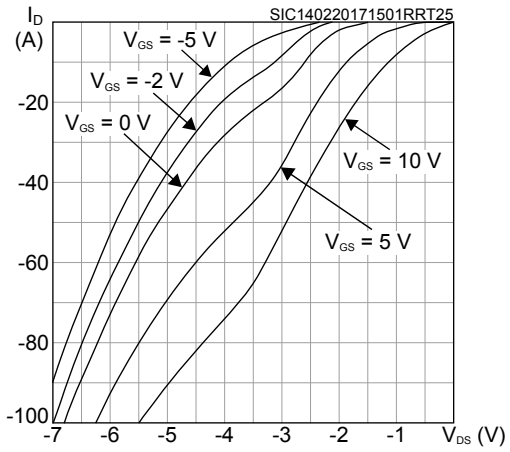
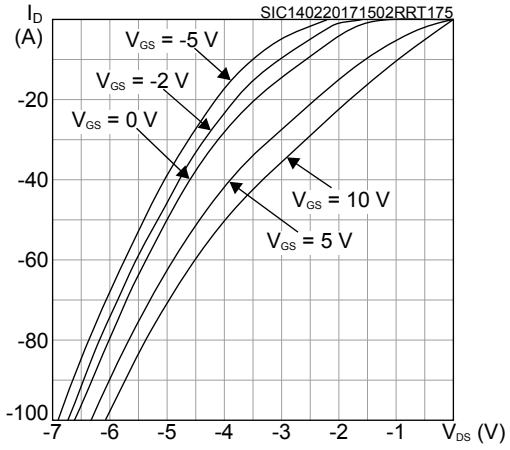


Figure 15. Reverse conduction characteristics (T_J = 175 °C)



3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

3.1 HiP247 long leads package information

Figure 16. HiP247 long leads package outline

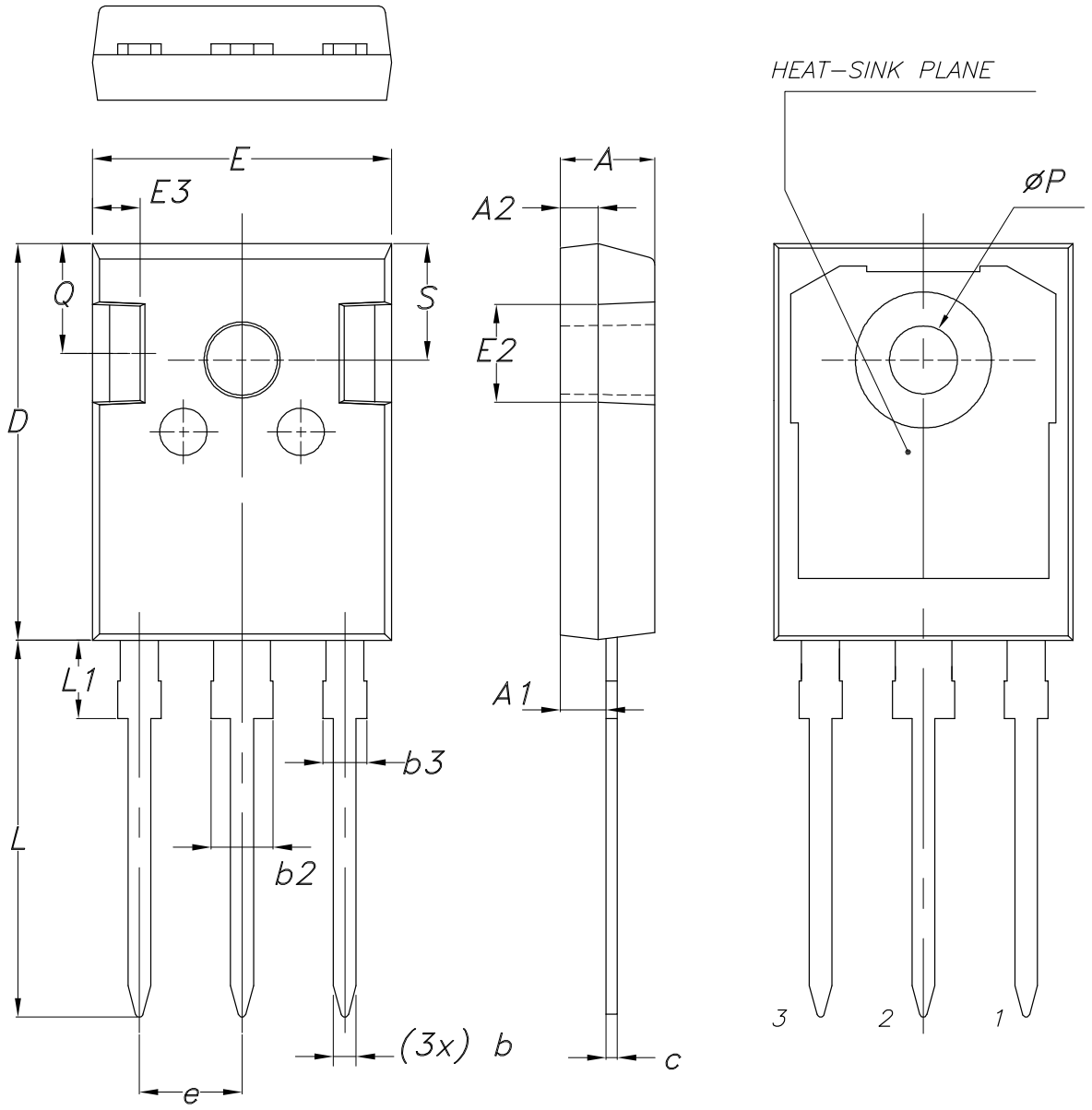


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Table 8. **HiP247 long leads package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
11-Aug-2020	1	First release.

Contents