MPSA13, MPSA14

MPSA14 is a Preferred Device

Darlington Transistors

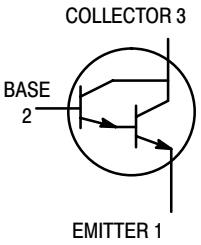
NPN Silicon

ON Semiconductor®

http://onsemi.com

Features

- Pb−Free Packages are Available*



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CES}	30	Vdc
Collector−Base Voltage	V_{CBO}	30	Vdc
Emitter−Base Voltage	V_{EBO}	10	Vdc
Collector Current − Continuous	I_C	500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	W mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150	°C

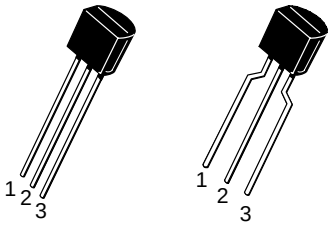
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/mW
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	83.3	°C/mW

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

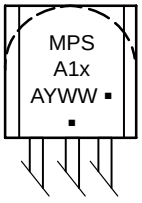
TO−92
CASE 29
STYLE 1



STRAIGHT LEAD
BULK PACK

BENT LEAD
TAPE & REEL
AMMO PACK

MARKING DIAGRAM



x = 3 or 4
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Breakdown Voltage (I_C = 100 μAdc, I_B = 0)		$V_{(BR)CES}$	30	−	Vdc
Collector Cutoff Current (V_{CB}= 30 Vdc, I_E = 0)		I_{CBO}	−	100	nAdc
Emitter Cutoff Current (V_{EB}= 10 Vdc, I_C = 0)		I_{EBO}	−	100	nAdc
ON CHARACTERISTICS (Note 1)					
DC Current Gain		h_{FE}			−
(I_C = 10 mAdc, V_{CE} = 5.0 Vdc)	MPSA13		5,000	−	
	MPSA14		10,000	−	
(I_C = 100 mAdc, V_{CE} = 5.0 Vdc)	MPSA13		10,000	−	
	MPSA14		20,000	−	
Collector−Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 0.1 mAdc)		$V_{CE(sat)}$	−	1.5	Vdc
Base−Emitter On Voltage (I_C = 100 mAdc, V_{CE} = 5.0 Vdc)		$V_{BE(on)}$	−	2.0	Vdc
SMALL−SIGNAL CHARACTERISTICS					
Current−Gain − Bandwidth Product (Note 2) (I_C = 10 mAdc, V_{CE} = 5.0 Vdc, f = 100 MHz)		f_T	125	−	MHz

1. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

ORDERING INFORMATION

Device	Package	Shipping†
MPSA13	TO−92	5000 Units / Bulk
MPSA13G	TO−92 (Pb−Free)	5000 Units / Bulk
MPSA13RLRA	TO−92	2000 / Tape & Reel
MPSA13RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
MPSA13RLRMG	TO−92 (Pb−Free)	2000 / Ammo Pack
MPSA13RLRPG	TO−92 (Pb−Free)	2000 / Ammo Pack
MPSA13ZL1G	TO−92 (Pb−Free)	2000 / Ammo Pack
MPSA14G	TO−92 (Pb−Free)	5000 Units / Bulk
MPSA14RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
MPSA14RLRPG	TO−92 (Pb−Free)	2000 / Ammo Pack

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

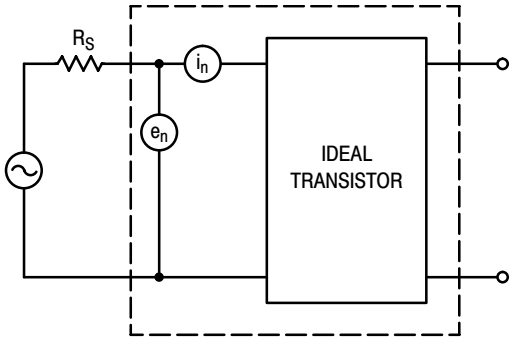


Figure 1. Transistor Noise Model

NOISE CHARACTERISTICS

(V_{CE} = 5.0 Vdc, T_A = 25°C)

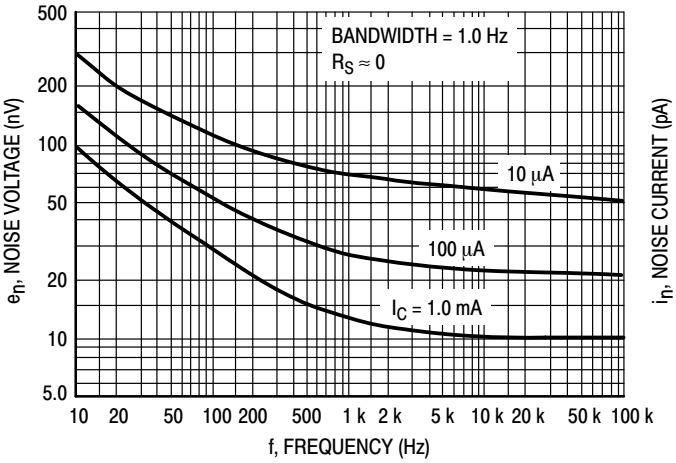


Figure 2. Noise Voltage

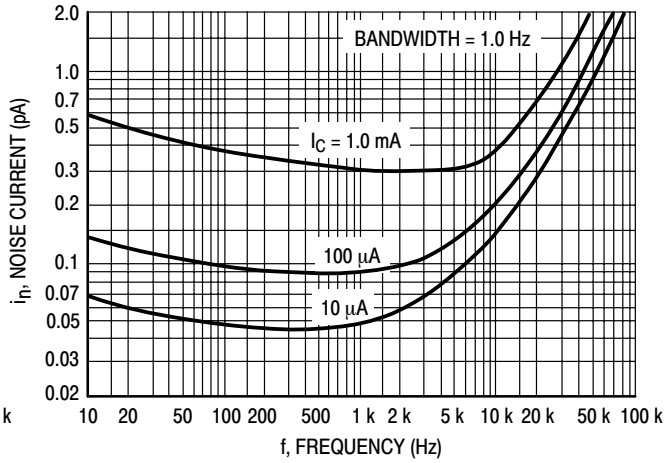


Figure 3. Noise Current

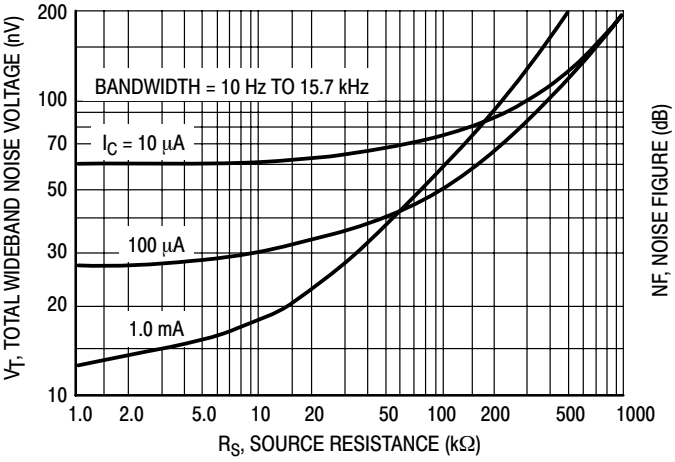


Figure 4. Total Wideband Noise Voltage

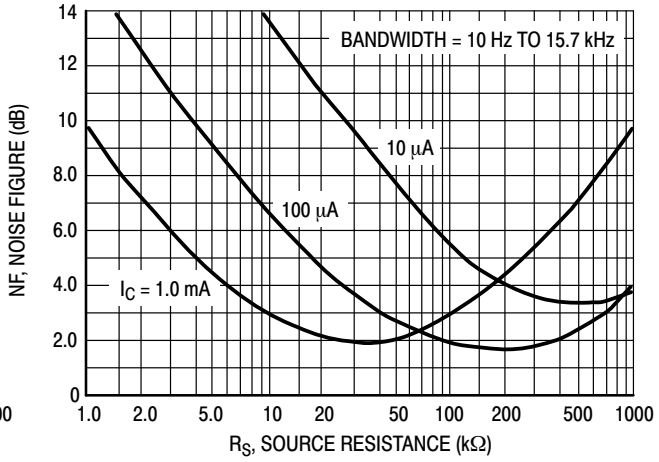


Figure 5. Wideband Noise Figure

SMALL−SIGNAL CHARACTERISTICS

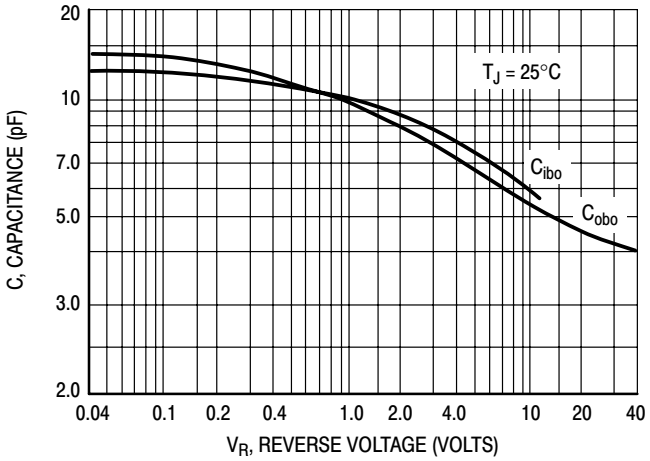


Figure 6. Capacitance

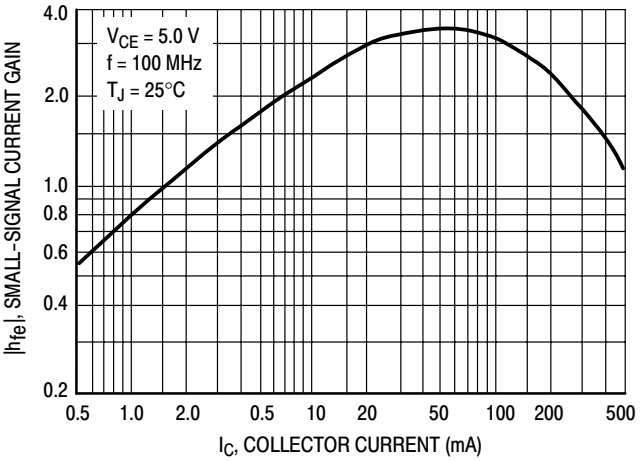


Figure 7. High Frequency Current Gain

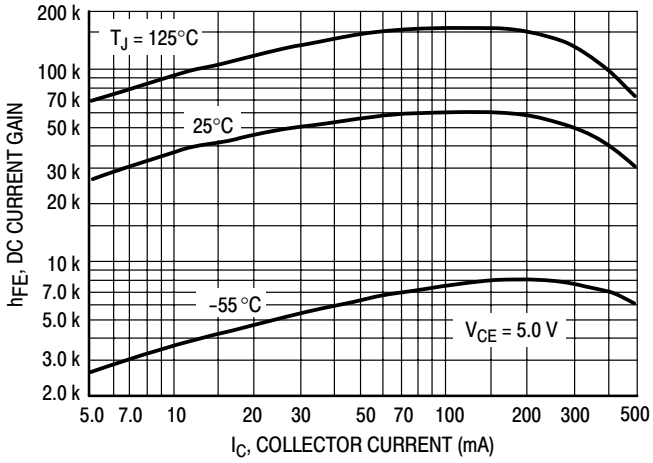


Figure 8. DC Current Gain

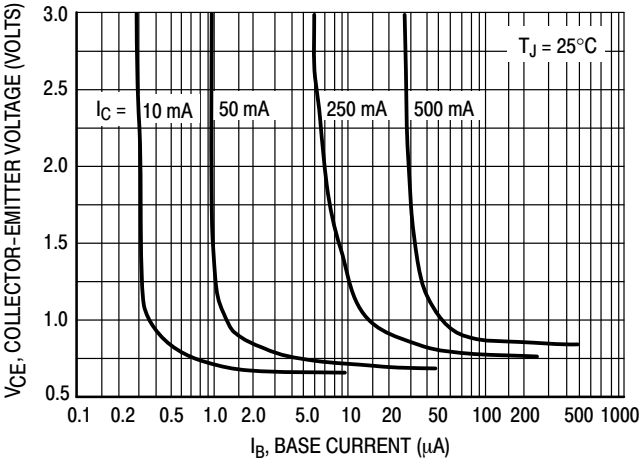


Figure 9. Collector Saturation Region

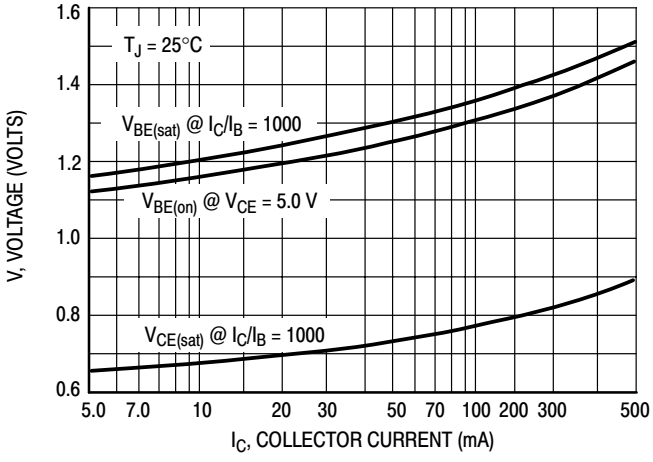


Figure 10. “On” Voltages

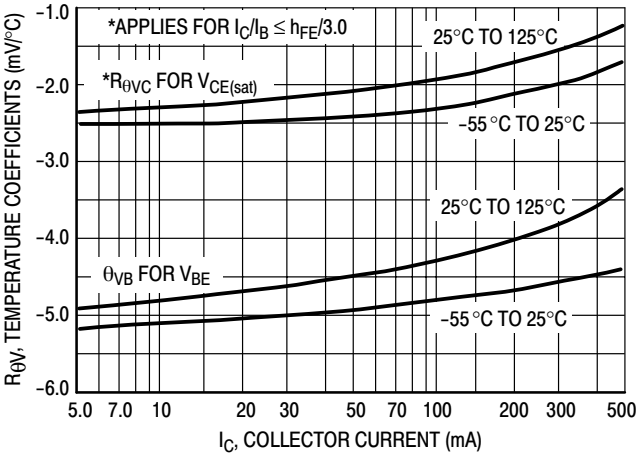


Figure 11. Temperature Coefficients

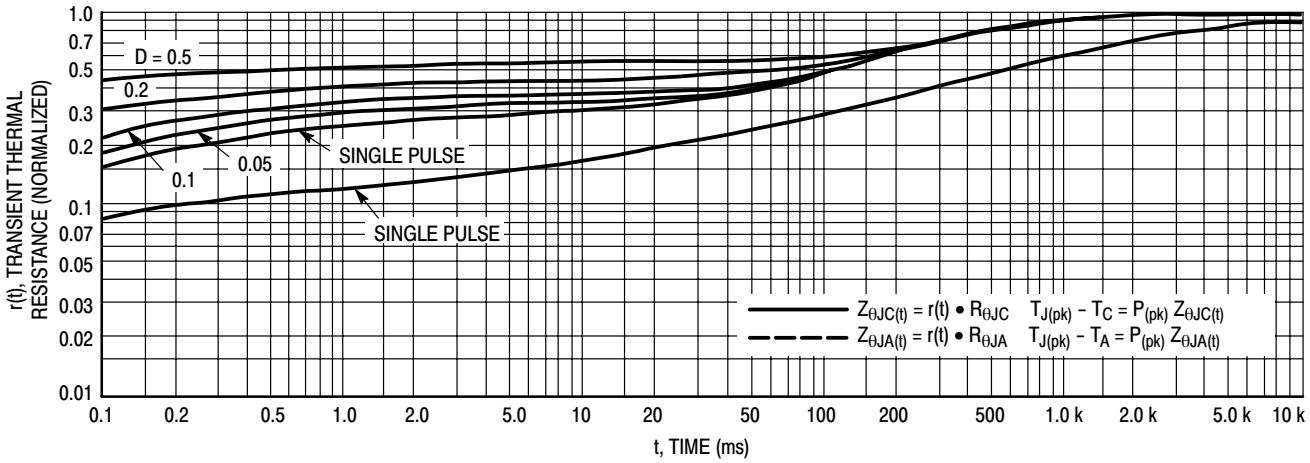


Figure 12. Thermal Response

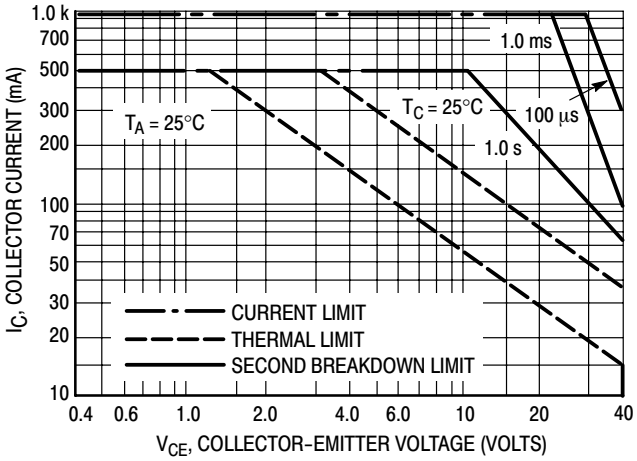
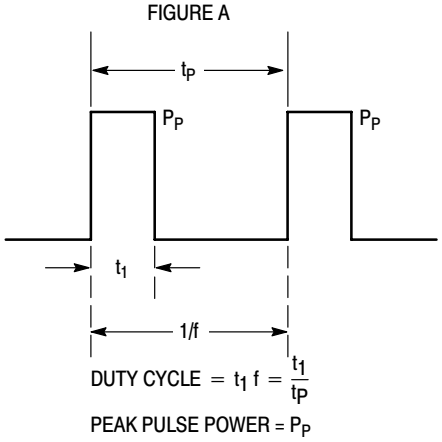


Figure 13. Active Region Safe Operating Area



Design Note: Use of Transient Thermal Resistance Data

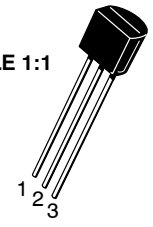
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

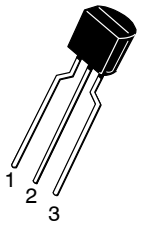
TO−92 (TO−226)
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

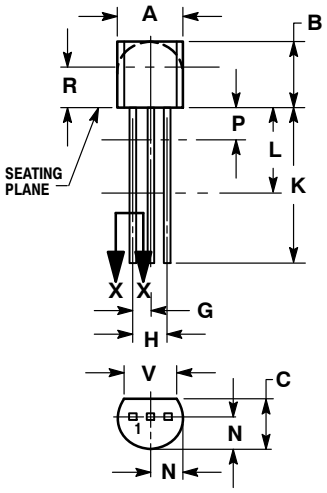
SCALE 1:1



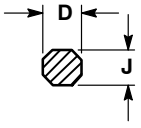
STRAIGHT LEAD
BULK PACK



BENT LEAD
TAPE & REEL
AMMO PACK



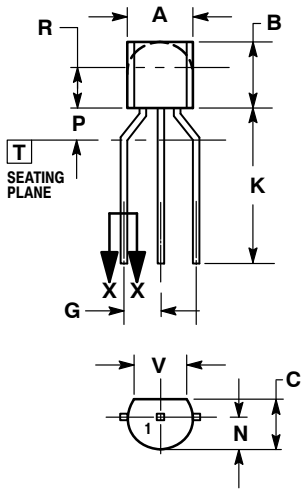
STRAIGHT LEAD
BULK PACK



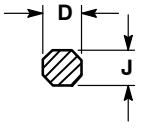
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD
TAPE & REEL
AMMO PACK



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS	
DIM	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

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NEW STANDARD:		
DESCRIPTION:	**TO−92 (TO−226)**	**PAGE 1 OF 3**

TO−92 (TO−226)
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

ISSUE	REVISION	DATE
AM	ADDED BENT−LEAD TAPE & REEL VERSION. REQ. BY J. SUPINA.	09 MAR 2007

PUBLICATION ORDERING INFORMATION

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