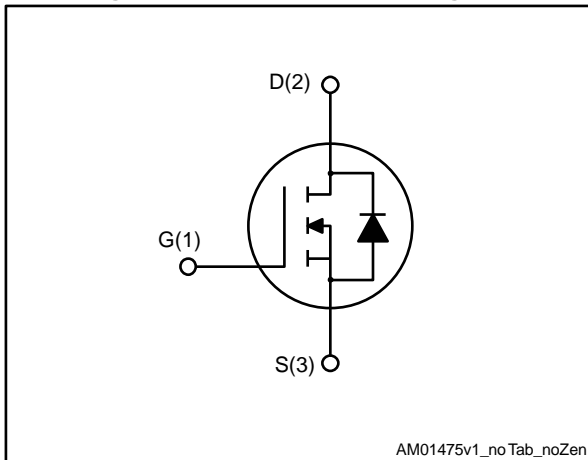


N-channel 600 V, 0.135 Ω typ., 20 A MDmesh™ II Power MOSFET in a TO-220FP package

Datasheet - production data



Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max	I _D
STF26NM60N	600 V	0.165 Ω	20 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packaging
STF26NM60N	26NM60N	TO-220FP	Tube

Contents

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	600	V
V _{GS}	Gate-source voltage	±30	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	20	A
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100 °C	12.6	A
I _{DM} ⁽¹⁾⁽²⁾	Drain current (pulsed)	80	A
P _{TOT}	Total dissipation at T _C = 25 °C	35	W
dv/dt ⁽³⁾	Peak diode recovery voltage slope	15	V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2500	V
T _{stg}	Storage temperature range	-55 to 150	°C
T _j	Operating junction temperature range		

Notes:

⁽¹⁾Limited by package.

⁽²⁾Pulse width limited by safe operating area.

⁽³⁾I_{SD} ≤ 20 A, di/dt ≤ 400 A/μs, V_{DS(peak)} ≤ V_{(BR)DSS}, V_{DD} ≤ 80% V_{(BR)DSS}

Table 3: Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	3.6	°C/W
R _{thj-amb}	Thermal resistance junction-ambient	62.5	°C/W

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AS}	Single pulse avalanche current (pulse width limited by T _{jmax})	6	A
E _{AS}	Single pulse avalanche energy (starting T _J =25 °C, I _D =I _{AR} , V _{DD} =50 V)	610	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	600			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			100	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 25\text{ V}$			± 0.1	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 10\text{ A}$		0.135	0.165	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 50\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	1800	-	pF
C_{oss}	Output capacitance		-	115	-	pF
C_{rss}	Reverse transfer capacitance		-	6	-	pF
$C_{oss\text{ eq.}}$ ⁽¹⁾	Equivalent output capacitance	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }480\text{ V}$	-	310	-	pF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 20\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 14: "Test circuit for gate charge behavior")	-	60	-	nC
Q_{gs}	Gate-source charge		-	8.5	-	nC
Q_{gd}	Gate-drain charge		-	30	-	nC
R_G	Gate input resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	2.8	-	Ω

Notes:

⁽¹⁾ $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 10\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13: "Test circuit for resistive load switching times" and Figure 18: "Switching time waveform")	-	13	-	ns
t_r	Rise time		-	25	-	ns
$t_{d(off)}$	Turn-off delay time		-	85	-	ns
t_f	Fall time		-	50	-	ns

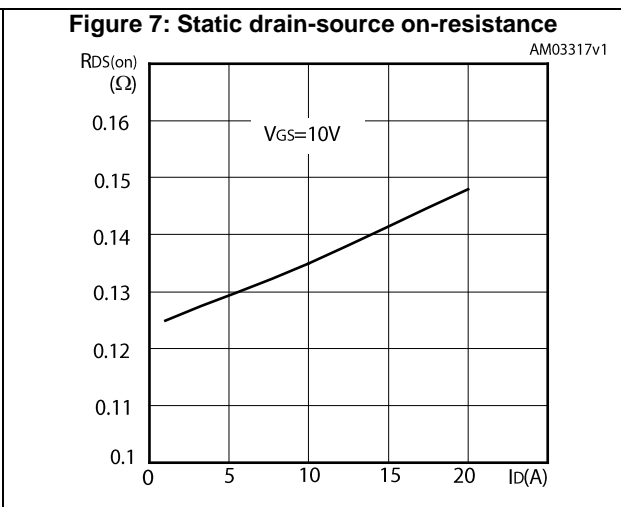
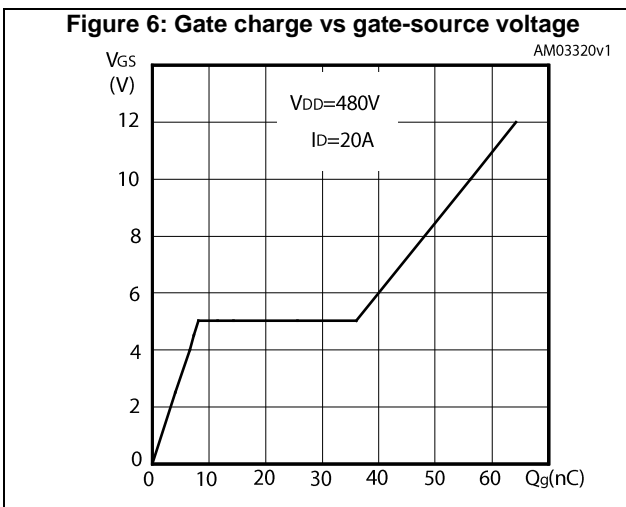
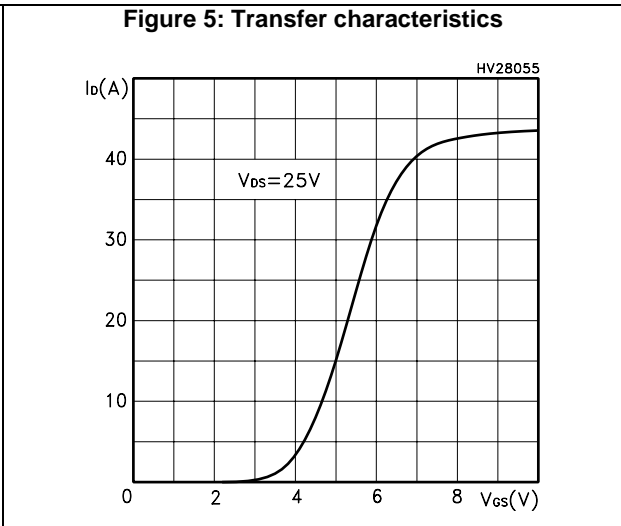
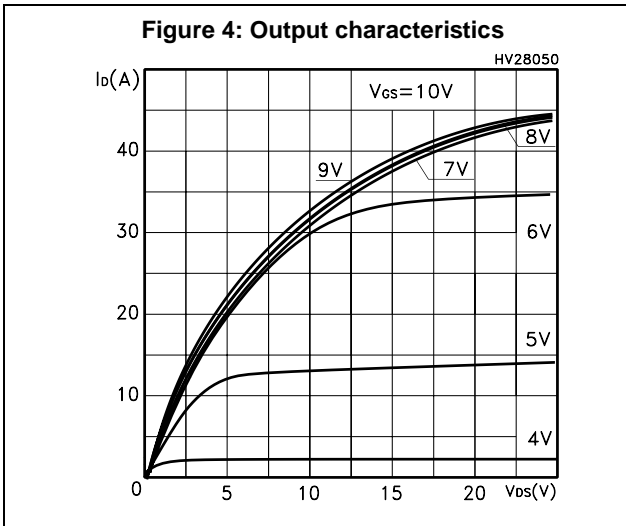
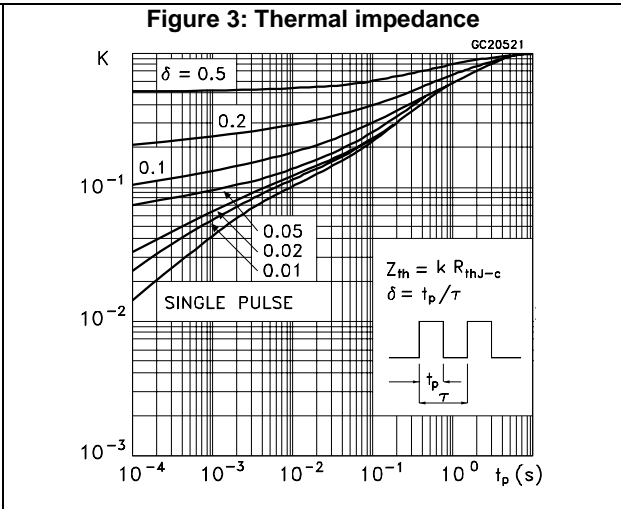
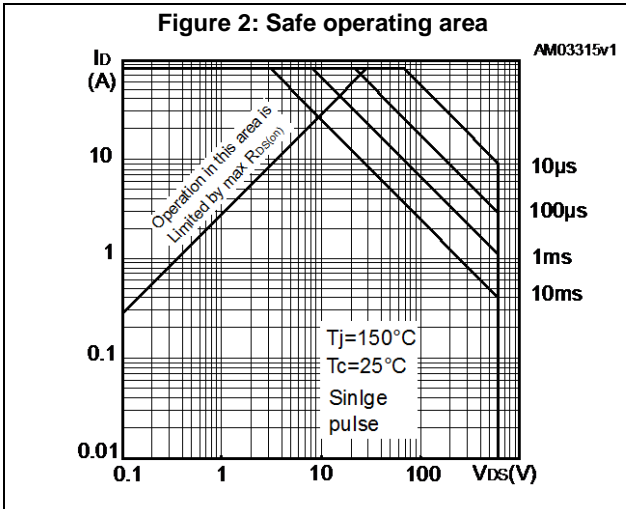
Table 8: Source-drain diode

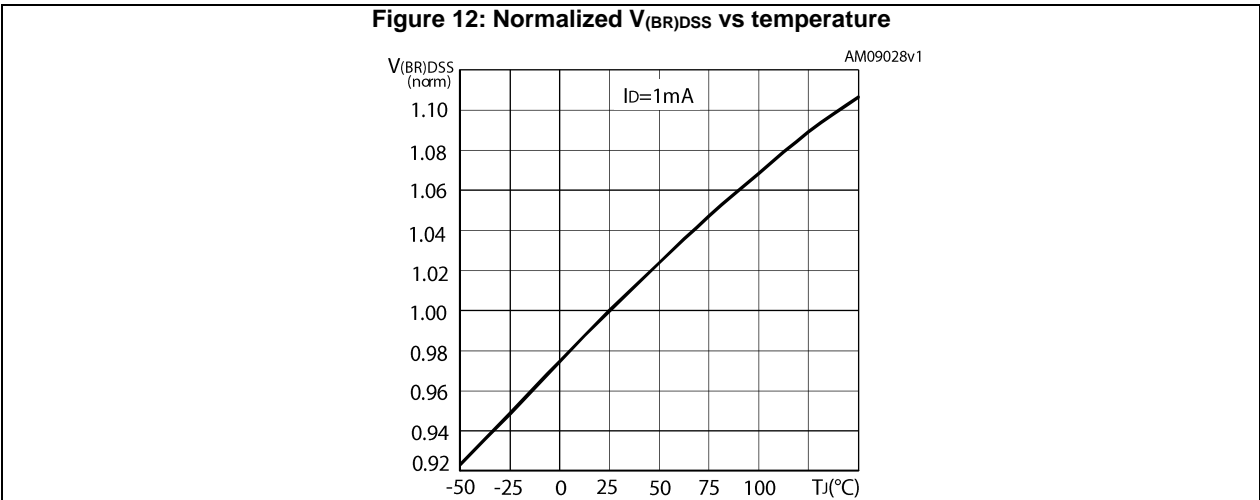
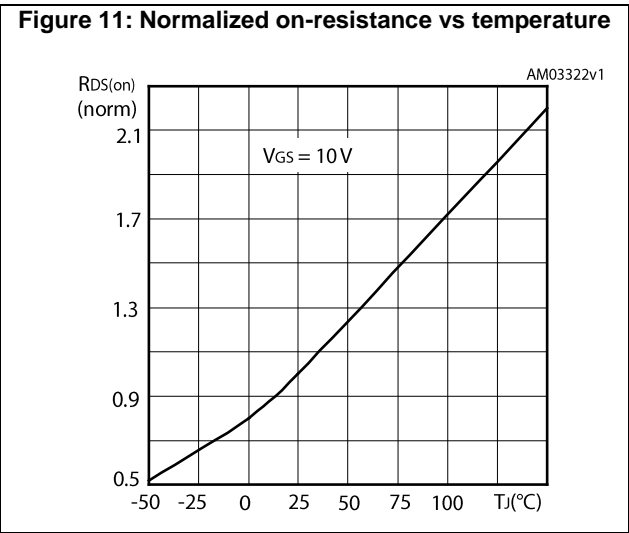
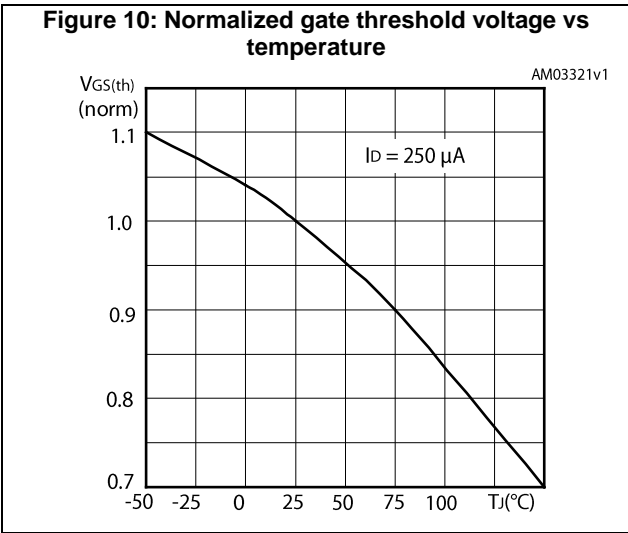
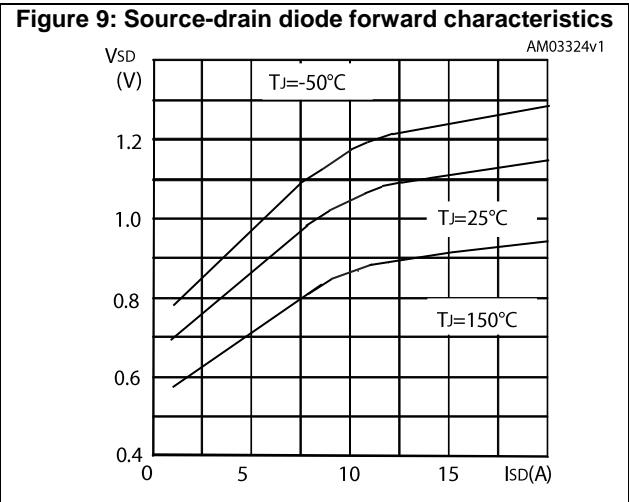
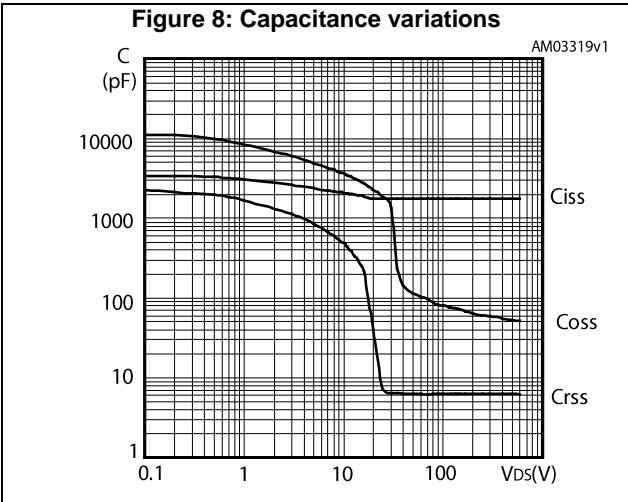
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		20	A
$I_{SDM}^{(2)}$	Source-drain current (pulsed)		-		80	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 20 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 20 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	370		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$	-	5.8		μC
I_{RRM}	Reverse recovery current	(see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	31.6		A
t_{rr}	Reverse recovery time	$I_{SD} = 20 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	450		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	7.5		μC
I_{RRM}	Reverse recovery current	(see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	32.5		A

Notes:

- (1) Pulse width limited by package.
(2) Pulse width limited by safe operating area.
(3) Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)





3 Test circuits

Figure 13: Test circuit for resistive load switching times



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Figure 14: Test circuit for gate charge behavior



AM01469v1

Figure 15: Test circuit for inductive load switching and diode recovery times



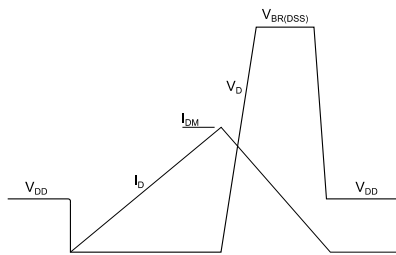
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Figure 16: Unclamped inductive load test circuit



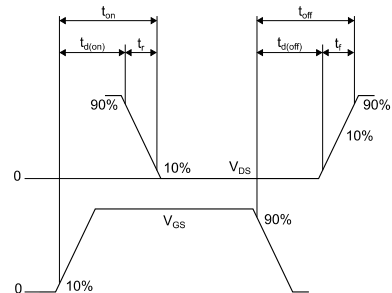
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Figure 17: Unclamped inductive waveform



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Figure 18: Switching time waveform



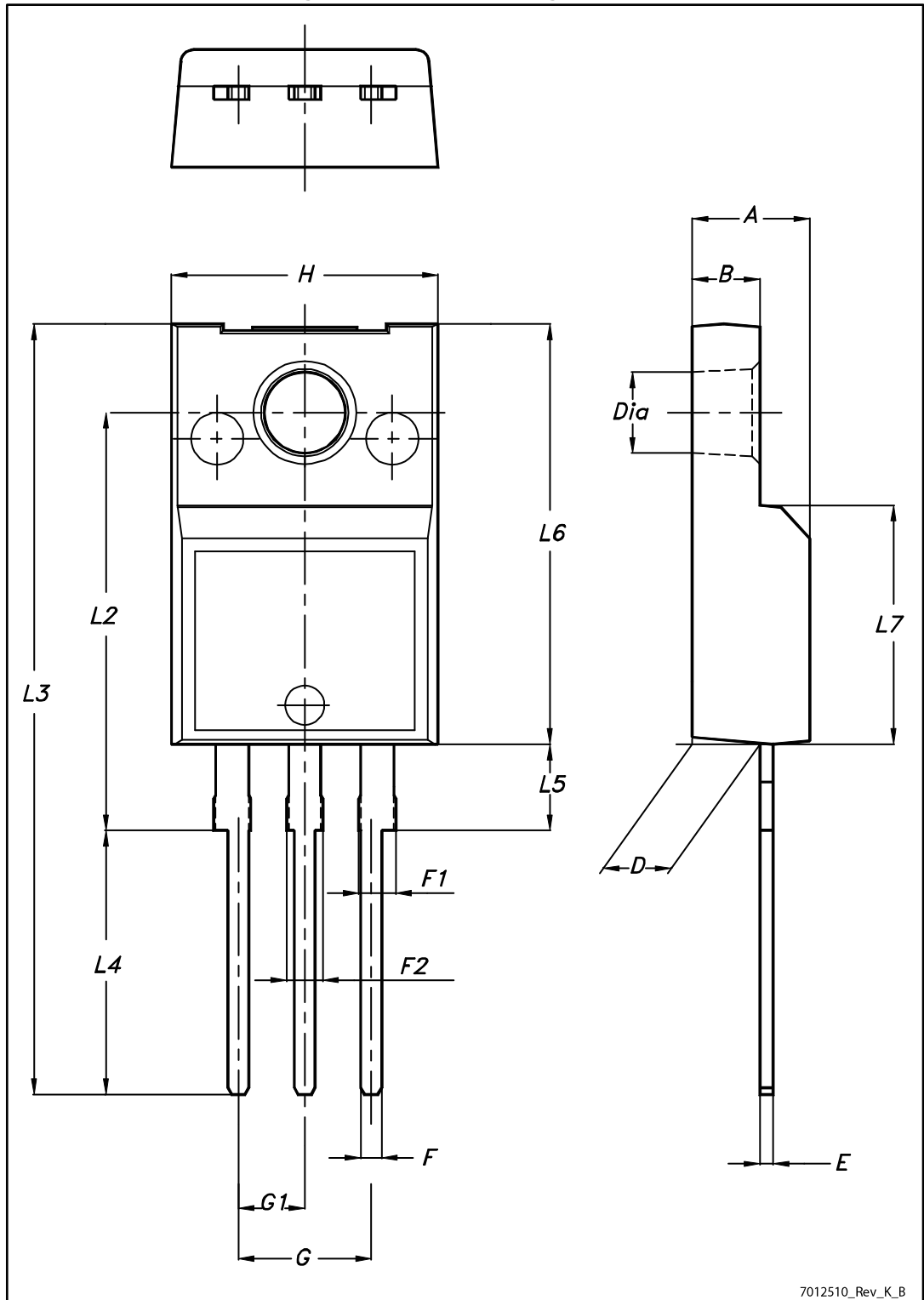
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 19: TO-220FP package outline



7012510_Rev_K_B

Table 9: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
13-Dec-2016	1	First release. Part number previously included in datasheet DocID15642

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