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October 2001

FDS6892A

## Dual N-Channel Logic Level PWM Optimized PowerTrench® MOSFET

General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 7.5 A, 20 V. $R_{DS(ON)} = 18$ mΩ @ $V_{GS} = 4.5$ V
  $R_{DS(ON)} = 24$ mΩ @ $V_{GS} = 2.5$ V

- Low gate charge (12 nC)

- High performance trench technology for extremely low $R_{DS(ON)}$

- High power and current handling capability

SO-8

Pin 1
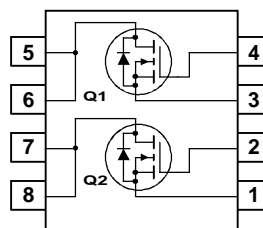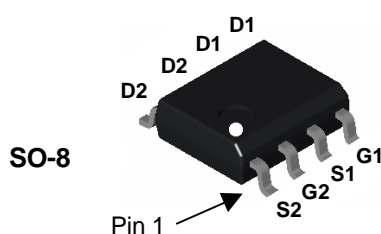
Absolute Maximum Ratings

$T_A = 25^{o}C$ unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		20	V
V_{GSS}	Gate-Source Voltage		$\pm$ 12	V
I_D	Drain Current – Continuous	(Note 1a)	7.5	A
	– Pulsed		30	
P_D	Power Dissipation for Dual Operation		2	W
	Power Dissipation for Single Operation	(Note 1a)	1.6	
		(Note 1b)	1	
		(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6892A	FDS6892A	13''	12mm	2500 units

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Electrical Characteristics T_A = 25°C unless otherwise noted

| Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV$_{DSS}$	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		5		mV/°C
I$_{DSS}$	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V V_{DS} = 16 V, V_{GS} = 0 V, T_J = 55°C			1 10	µA
I$_{GSSF}$	Gate–Body Leakage, Forward	V_{GS} = 12 V, V_{DS} = 0 V			100	nA
I$_{GSSR}$	Gate–Body Leakage, Reverse	V_{GS} = –12 V, V_{DS} = 0 V			–100	nA
On Characteristics (Note 2)						
V$_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.6	0.9	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		–3		mV/°C
R$_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 7.5 A V_{GS} = 2.5 V, I_D = 6.5 A V_{GS} = 4.5 V, I_D = 7.5 A, T_J = 125°C		13 17 18	18 24 27	mΩ
I$_{D(on)}$	On–State Drain Current	V_{GS} = 4.5V, V_{DS} = 5 V	15			A
g$_{FS}$	Forward Transconductance	V_{DS} = 5 V, I_D = 7.5 A		37		S
Dynamic Characteristics						
C$_{iss}$	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		1333		pF
C$_{oss}$	Output Capacitance			301		pF
C$_{rss}$	Reverse Transfer Capacitance			160		pF
Switching Characteristics (Note 2)						
t$_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		8	16	ns
t$_r$	Turn–On Rise Time			15	27	ns
t$_{d(off)}$	Turn–Off Delay Time			26	42	ns
t$_f$	Turn–Off Fall Time			9	18	ns
Q$_g$	Total Gate Charge	V_{DS} = 10 V, I_D = 7.5 A, V_{GS} = 4.5 V		12	17	nC
Q$_{gs}$	Gate–Source Charge			2.5		nC
Q$_{gd}$	Gate–Drain Charge			3		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I$_S$	Maximum Continuous Drain–Source Diode Forward Current				1.3	A
V$_{SD}$	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)		0.7	1.2	V

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
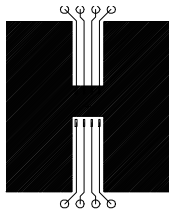
a) 78°C/W when mounted on a 0.5in^2 pad of 2 oz copper
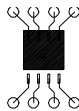
b) 125°C/W when mounted on a 0.02 in^2 pad of 2 oz copper
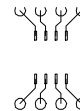
c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

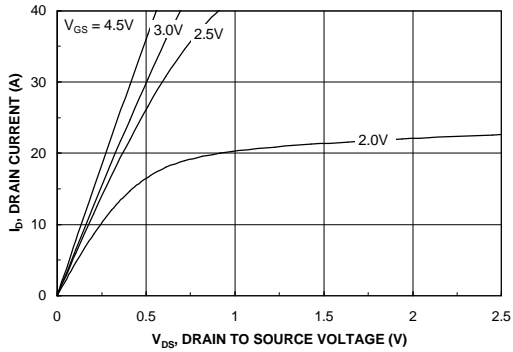FDS6892A Rev C (W)

Typical Characteristics
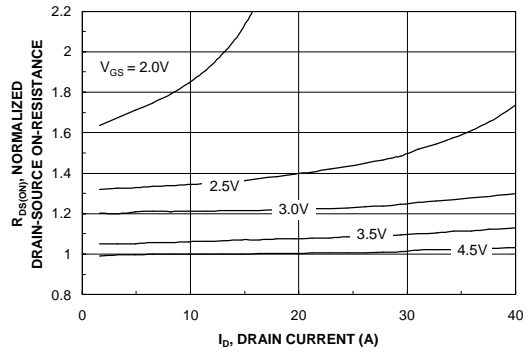

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.
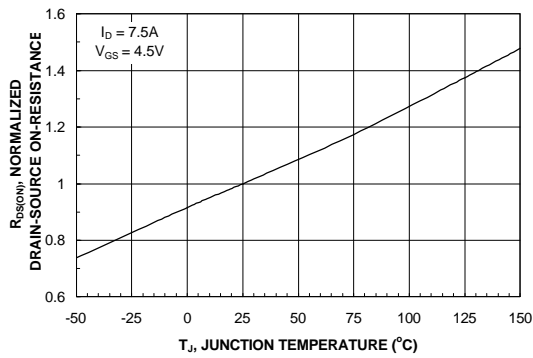

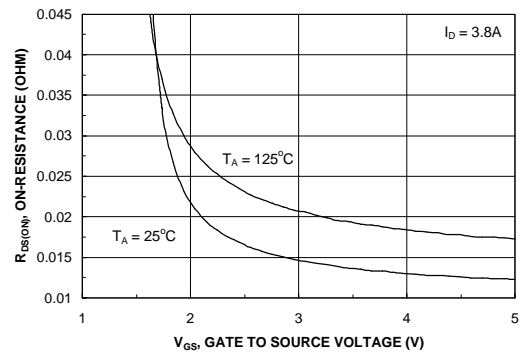Figure 3. On-Resistance Variation with Temperature.

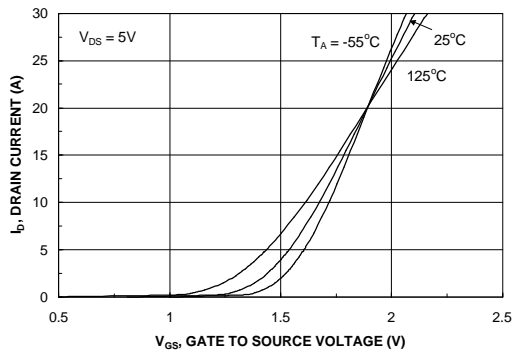Figure 4. On-Resistance Variation with Gate-to-Source Voltage.
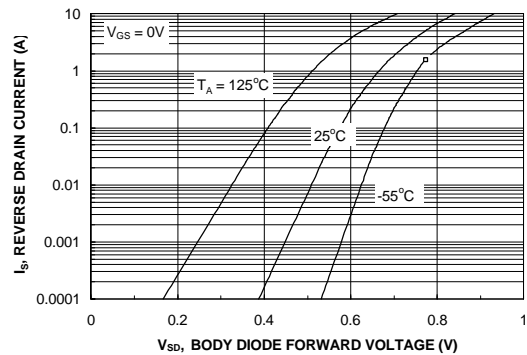

Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

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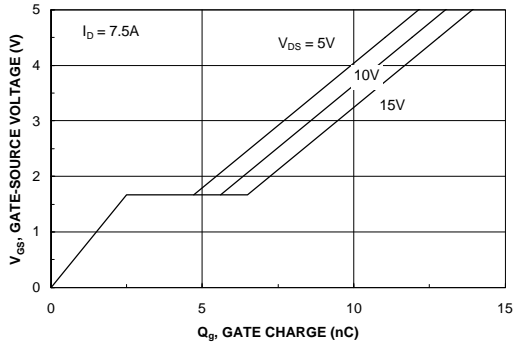## Typical Characteristics

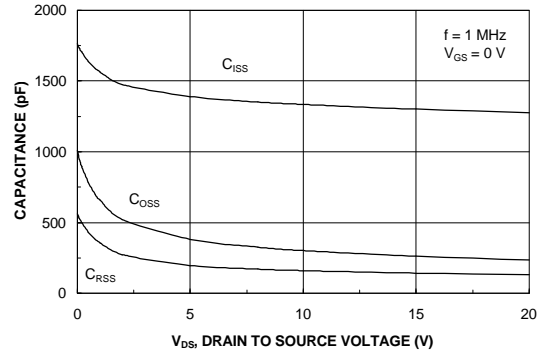**Figure 7. Gate Charge Characteristics.**

Figure 8. Capacitance Characteristics.
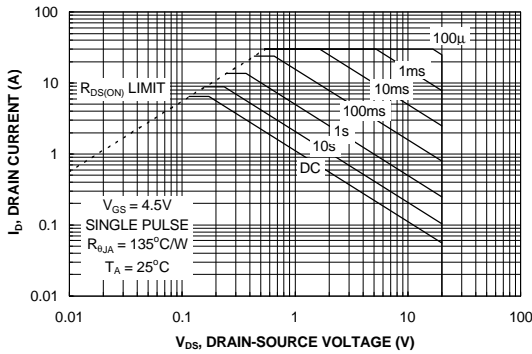
Figure 9. Maximum Safe Operating Area.
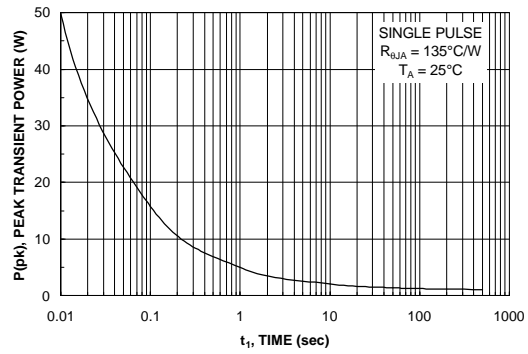
Figure 10. Single Pulse Maximum Power Dissipation.

$$R_{\theta JA}(t) = r(t) * R_{\theta JA}$$
$$R_{\theta JA} = 135^{\circ}C/W$$
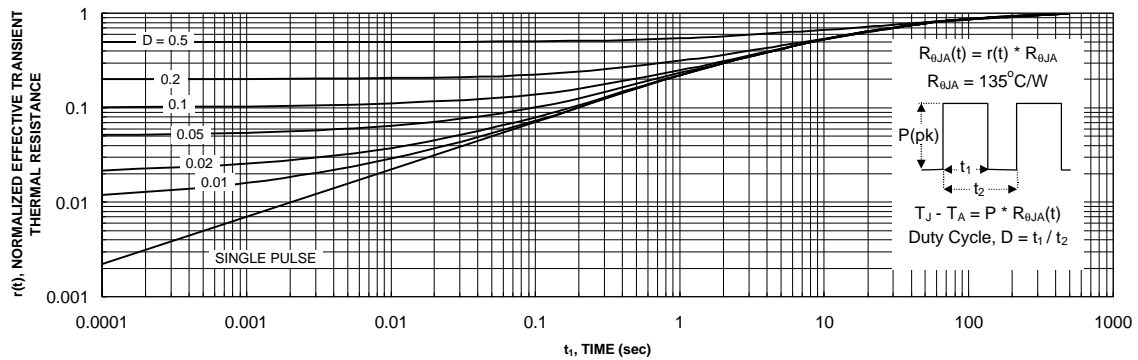$$T_J - T_A = P * R_{\theta JA}(t)$$
Duty Cycle, $D = t_1 / t_2$

Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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Rev. H4

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