NTGD3148N

MOSFET – Power, Dual, N-Channel, TSOP-6

20 V, 3.5 A

Features

- Low Threshold Levels, VGS(th) < 1.5 V
- Low Gate Charge (3.8 nC)
- Leading Edge Trench Technology of Low $R_{DS(on)}$
- High Power and Current Handling Capability
- This is a Pb−Free Device

Applications

- DC−DC Converters (Buck and Boost Circuits)
- Low Side Load Switch
- Optimized for Battery and Load Management Applications in Portable Equipment Like Cell Phones, DSCs, Media Player, Etc
- Battery Charging and Protection Circuits

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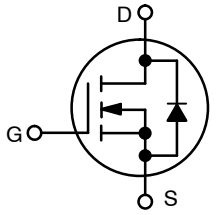
N−CHANNEL MOSFET

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
20 V	70 mΩ @ 4.5 V	3.5 A
	100 mΩ @ 2.5 V	



N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	3.0	A
		T_A = 85°C		2.2	
Continuous Drain Current (Note 1)	t ≤ 5 s	T_A = 25°C	I_D	3.5	A
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.9	W
	t ≤ 5 s			1.1	
Pulsed Drain Current		t_p = 10 μs	I_{DM}	10	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−50 to 150	°C
Source Current (Body Diode)			I_S	0.8	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

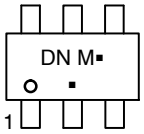
Parameter	Symbol	Value	Unit
Junction−to−Ambient – Steady State (Note 1)	$R_{\theta JA}$	140	°C/W
Junction−to−Ambient – t ≤ 5 s (Note 1)	$R_{\theta JA}$	110	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

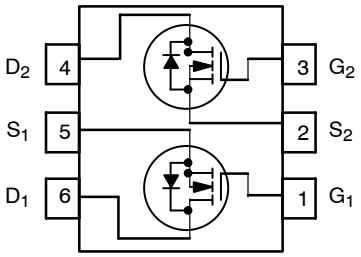
TSOP−6
CASE 318G
STYLE 13

MARKING DIAGRAM



DN = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN CONNECTION



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, Ref to 25°C			12.5		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±12 V				100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		0.5		1.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				3.28		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V	I_D = 3.5 A		41.7	70	mΩ
		V_{GS} = 2.5 V	I_D = 2.8 A		58	100	
Forward Transconductance	g_{FS}	V_{DS} = 5.0 V, I_D = 3.5 A			6.2		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 10 V			300		pF
Output Capacitance	C_{OSS}				73		
Reverse Transfer Capacitance	C_{RSS}				44		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.5 A			3.8		nC
Threshold Gate Charge	$Q_{G(TH)}$				0.3		
Gate−to−Source Charge	Q_{GS}				0.7		
Gate−to−Drain Charge	Q_{GD}				1.1		
Gate Resistance	RG				2.8		Ω
SWITCHING CHARACTERISTICS (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 3.5 A, R_G = 3.0 Ω			7.4		ns
Rise Time	t_r				11.2		
Turn−Off Delay Time	$t_{d(OFF)}$				12.8		
Fall Time	t_f				1.6		
DRAIN−TO−SOURCE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_D = 0.8 A	T_J = 25°C		0.71		V
			T_J = 125°C		0.57		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = 0.8 A			9.0		ns
Charge Time	T_a				5.0		
Discharge Time	T_b				4.0		
Reverse Recovery Time	Q_{RR}				2.5		nC

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping†
NTGD3148NT1G	TSOP−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

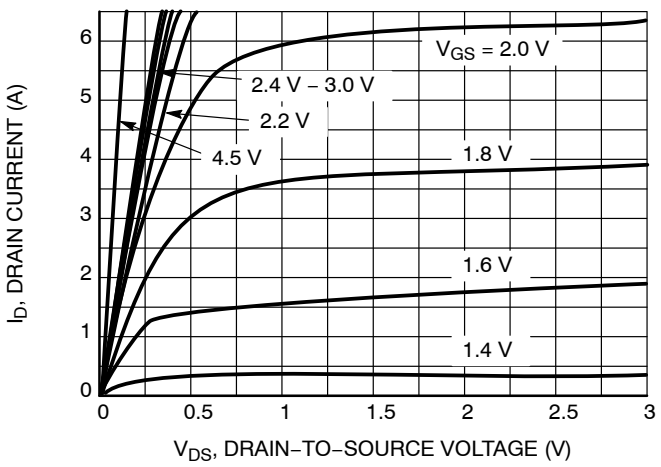


Figure 1. On–Region Characteristics

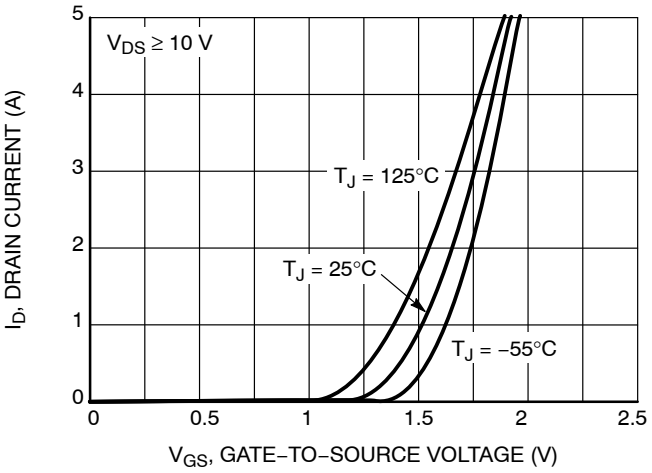


Figure 2. Transfer Characteristics

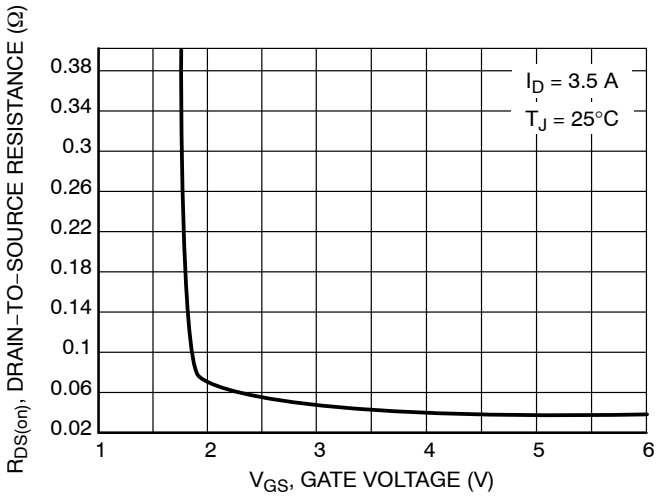


Figure 3. On–Resistance vs. Voltage

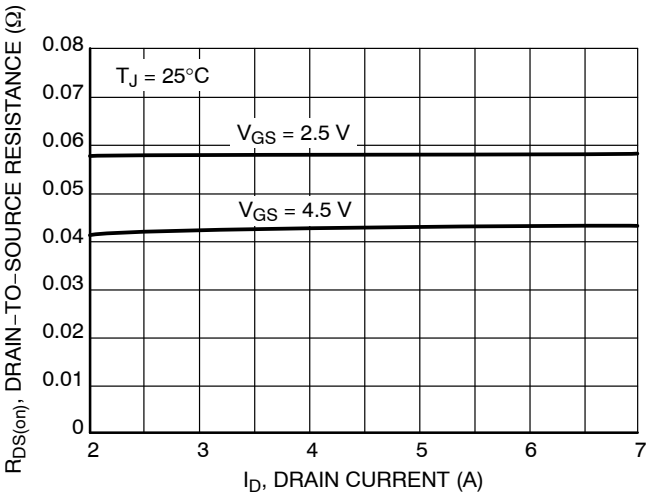


Figure 4. On–Resistance vs. Drain Current and Gate Voltage

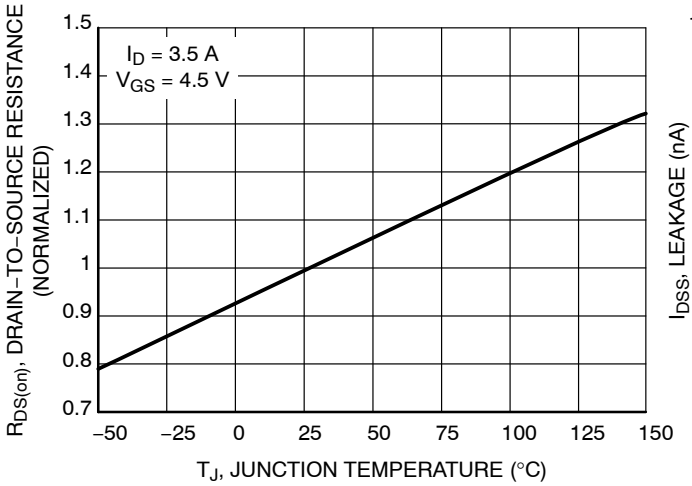


Figure 5. On–Resistance Variation vs. Temperature

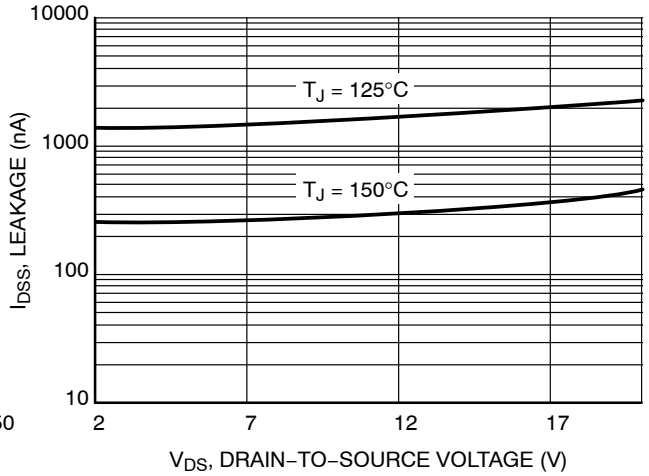


Figure 6. Drain–to–Source Leakage Current vs. Voltage

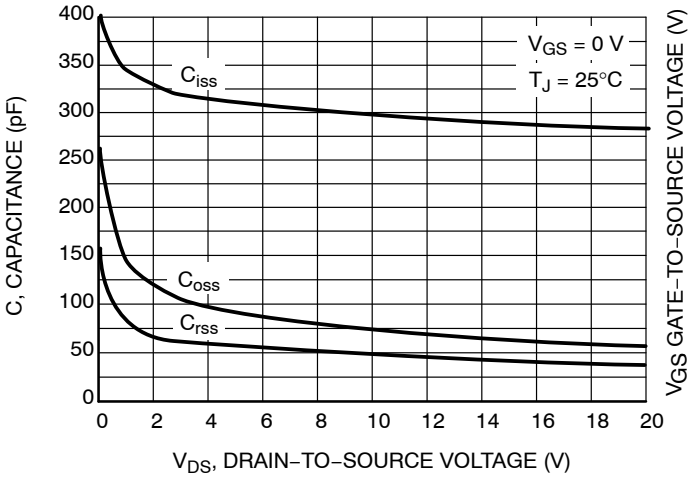


Figure 7. Capacitance Variation

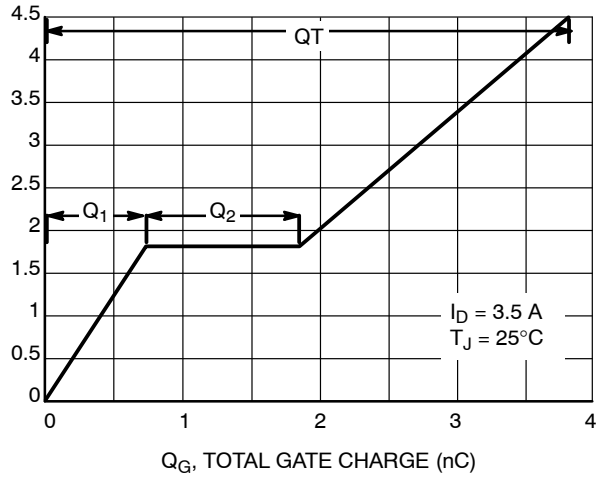


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

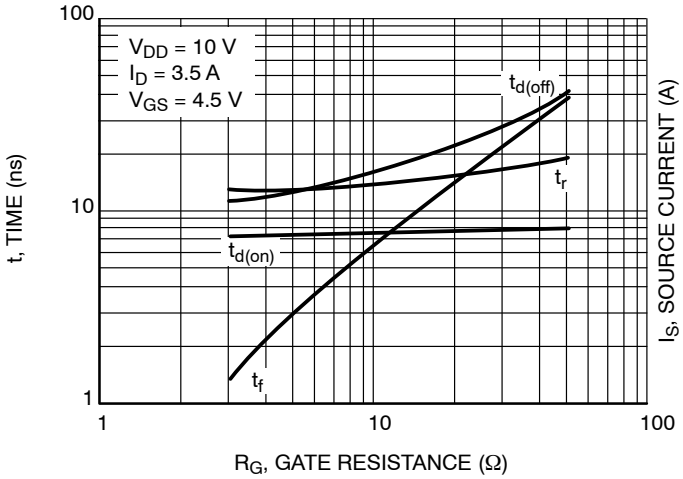


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

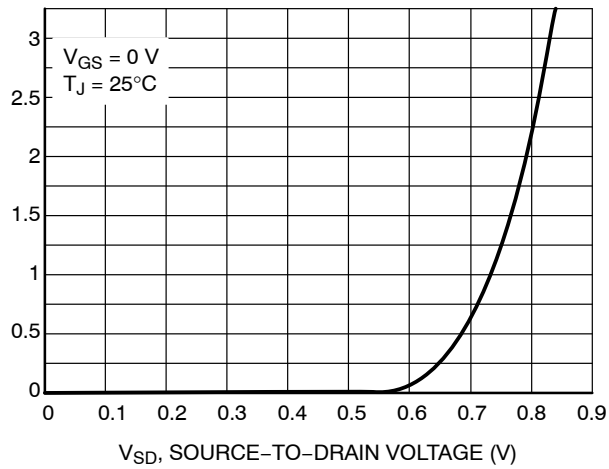


Figure 10. Diode Forward Voltage vs. Current

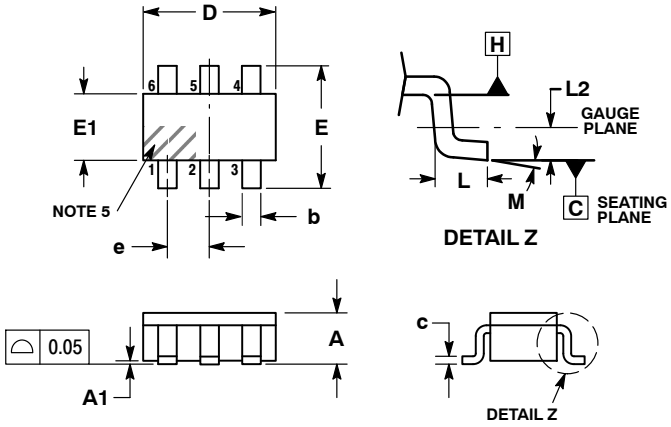
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2		0.25 BSC	
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

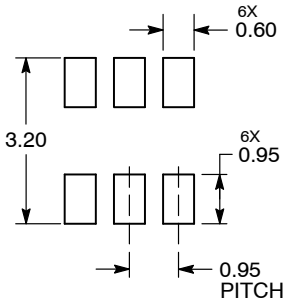
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

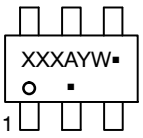
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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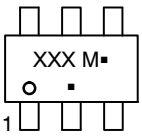

STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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DESCRIPTION:	**TSOP−6**	**PAGE 1 OF 1**

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