

FDS7760A

N-Channel Logic Level PowerTrench[®] MOSFET

General Description

This N-Channel Logic Level MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

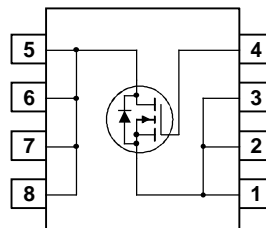
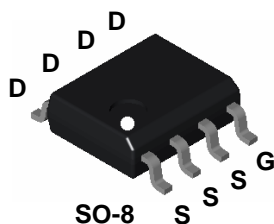
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Applications

- DC/DC converter
- Load switch
- Motor drives

Features

- 15 A, 30 V. $R_{DS(ON)} = 5.5 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 8 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$.
- Low gate charge (37nC typical)
- Fast switching speed.
- High performance trench technology for extremely low $R_{DS(ON)}$.
- High power and current handling capability.



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	Drain-Source Voltage	30	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current – Continuous (Note 1a)	15	A
	– Pulsed	60	
P _D	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1c)	50 (10 sec)	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	30	°C/W

Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS7760A	FDS7760A	13"	12mm	2500 units

DMOS Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Drain-Source Avalanche Ratings (Note 2)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 15\text{ V}$, $I_D = 15\text{ A}$			360	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				15	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		24		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	1	1.6	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-5		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 15\text{ A}$, $T_J = 125^\circ\text{C}$ $V_{GS} = 4.5\text{ V}$, $I_D = 13\text{ A}$		4.5 7 6	5.5 8 8	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 5\text{ V}$	50			A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 15\text{ A}$		65		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		3514		pF
C_{oss}	Output Capacitance			1123		pF
C_{rss}	Reverse Transfer Capacitance			307		pF

Switching Characteristics (Note 2)

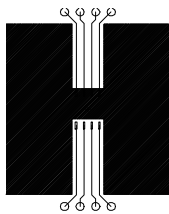
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$		13	20	ns
t_r	Turn-On Rise Time			12	19	ns
$t_{d(off)}$	Turn-Off Delay Time			78	125	ns
t_f	Turn-Off Fall Time			32	51	ns
Q_g	Total Gate Charge	$V_{DS} = 15\text{ V}$, $I_D = 15\text{ A}$, $V_{GS} = 5\text{ V}$		37	55	nC
Q_{gs}	Gate-Source Charge			10		nC
Q_{gd}	Gate-Drain Charge			12		nC

Drain-Source Diode Characteristics and Maximum Ratings

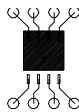
I_S	Maximum Continuous Drain-Source Diode Forward Current			2.1		A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V

Notes:

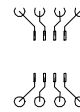
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°/W when mounted on a 1in² pad of 2 oz copper



b) 105°/W when mounted on a .04 in² pad of 2 oz copper



c) 125°/W when mounted on a minimum pad.

2. Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

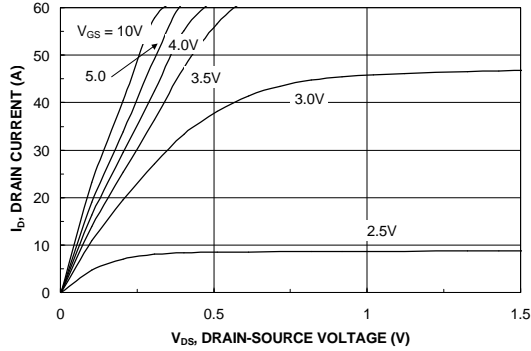


Figure 1. On-Region Characteristics.

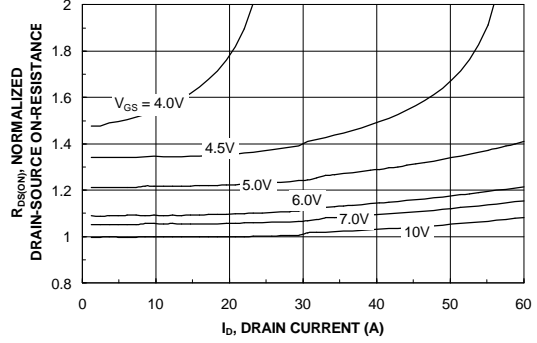


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

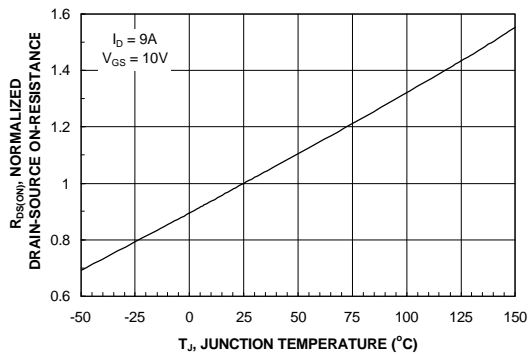


Figure 3. On-Resistance Variation with Temperature.

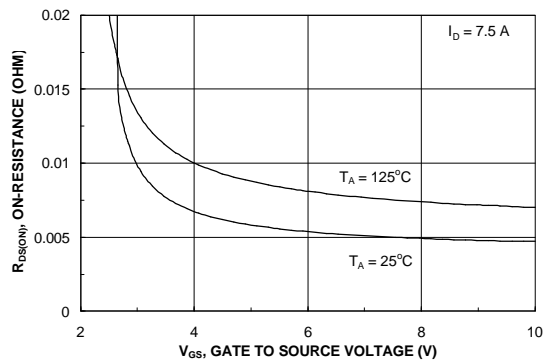


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

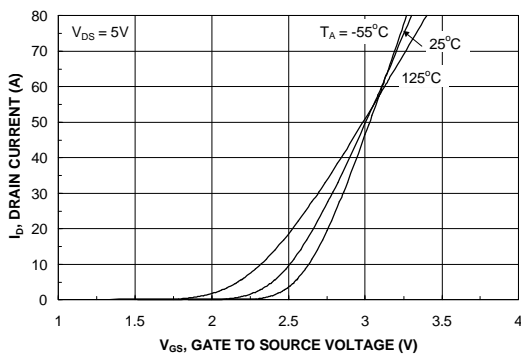


Figure 5. Transfer Characteristics.

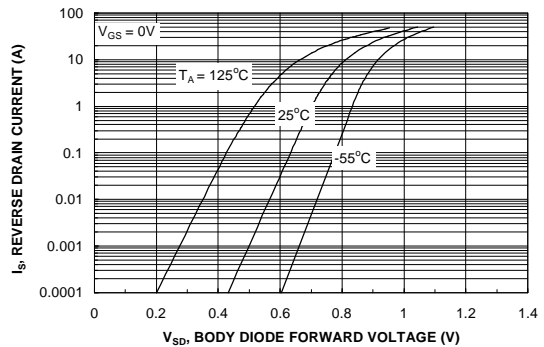


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

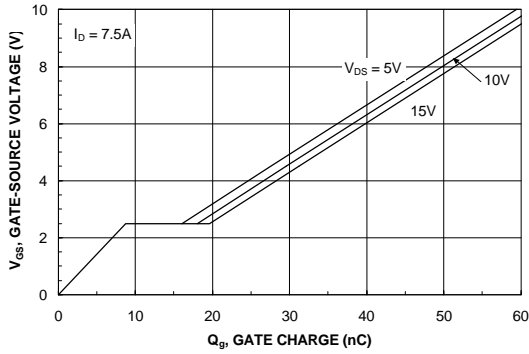


Figure 7. Gate Charge Characteristics.

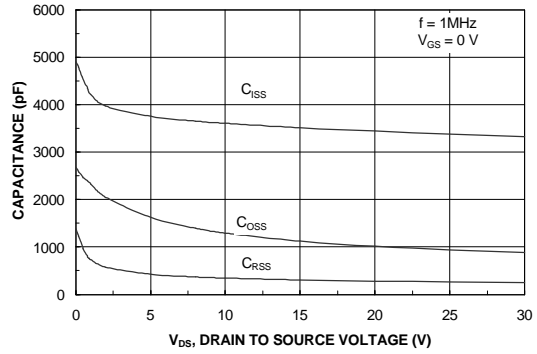


Figure 8. Capacitance Characteristics.

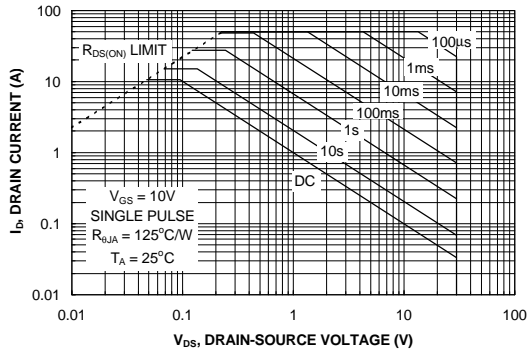


Figure 9. Maximum Safe Operating Area.

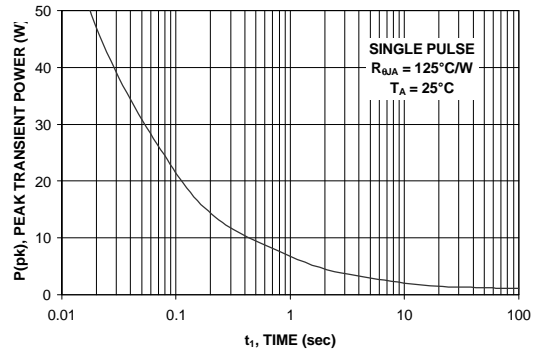


Figure 10. Single Pulse Maximum Power Dissipation.

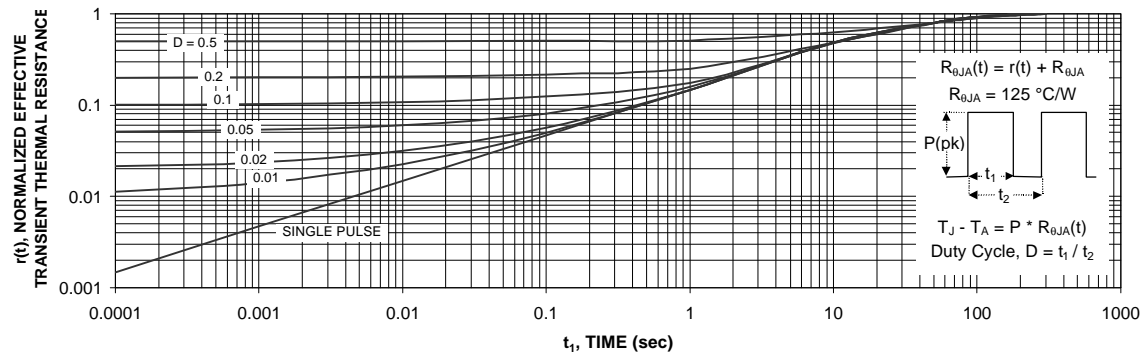


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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