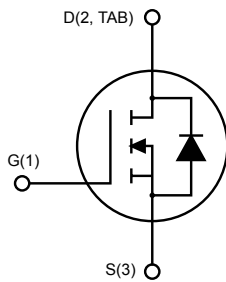
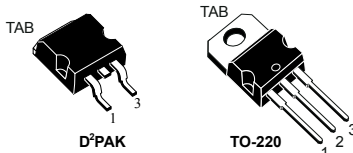


## Automotive-grade N-channel 55 V, 6.2 mΩ typ., 80 A, STripFET™ II Power MOSFETs in D<sup>2</sup>PAK and TO-220 packages




AM01475v1\_noZen



### Features

Type	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STB85NF55T4	55 V	8.0 mΩ	80 A
STP85NF55			

- AEC-Q101 qualified 
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

### Applications

- Switching applications

### Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

#### Product status link

[STB85NF55T4](#)
[STP85NF55](#)

#### Product summary

Order code	STB85NF55T4
Marking	B85NF55
Package	D <sup>2</sup> PAK
Packing	Tape and reel
Order code	STP85NF55
Marking	P85NF55
Package	TO-220
Packing	Tube

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	55	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	80	A
	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	80	A
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2.0	W/ $^\circ\text{C}$
$E_{AS}^{(3)}$	Single-pulse avalanche energy	980	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	10	V/ns
$T_{stg}$	Storage temperature range	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

1. Current limited by package.
2. Pulse width limited by safe operating area.
3. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $I_D = 40\text{ A}$ ,  $V_{DD} = 37.5\text{ V}$
4.  $I_{SD} \leq 80\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq T_{JMAX}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	$^\circ\text{C}/\text{W}$

## 2 Electrical characteristics

$T_{CASE} = 25\text{ °C}$  unless otherwise specified

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	55			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 55\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}, V_{DS} = 55\text{ V}$ $T_C = 125\text{ °C}$ <sup>(1)</sup>			10	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		6.2	8.0	m $\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}$ <sup>(1)</sup>	Forward transconductance	$V_{DS} = 15\text{ V}, I_D = 40\text{ A}$		120		S
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0\text{ V}$	-	3700		pF
$C_{oss}$	Output capacitance		-	900		pF
$C_{riss}$	Reverse transfer capacitance		-	310		pF
$Q_g$	Total gate charge	$V_{DD} = 30\text{ V}, I_D = 80\text{ A},$ $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior)	-	120	150	nC
$Q_{gs}$	Gate-source charge		-	30		nC
$Q_{gd}$	Gate-drain charge		-	45		nC

1. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

**Table 5. Switching times**

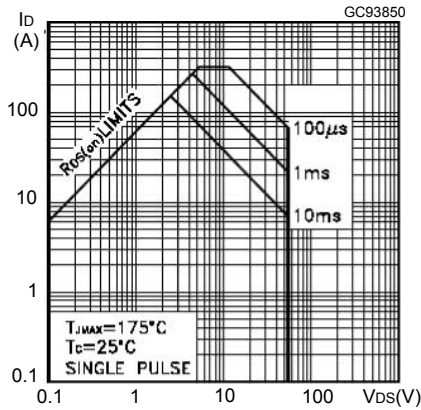
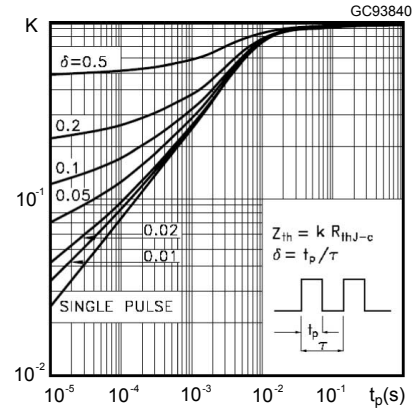
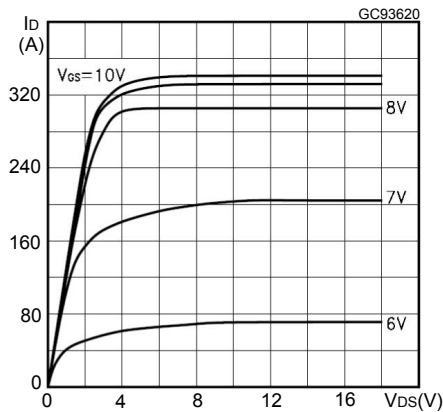
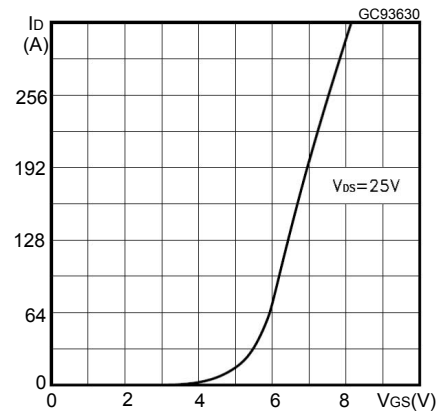
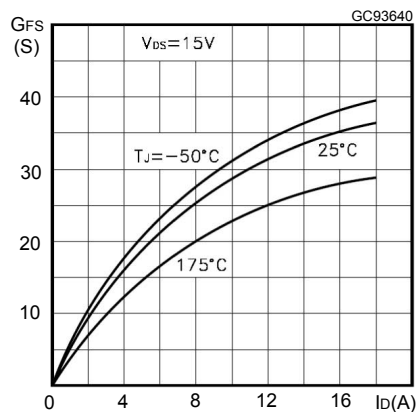
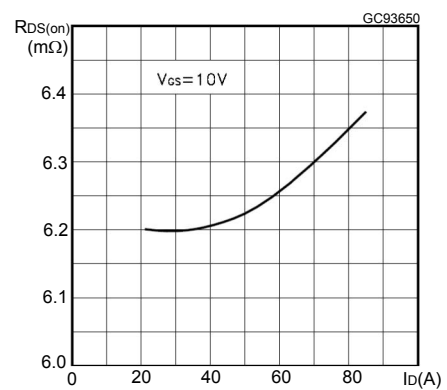
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}, I_D = 40\text{ A},$ $R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$	-	25	-	ns
$t_r$	Rise time		-	100	-	ns
$t_{d(off)}$	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform)	-	70	-	ns
$t_f$	Fall time		-	35	-	ns

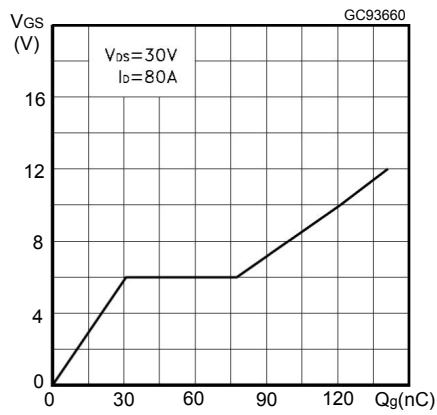
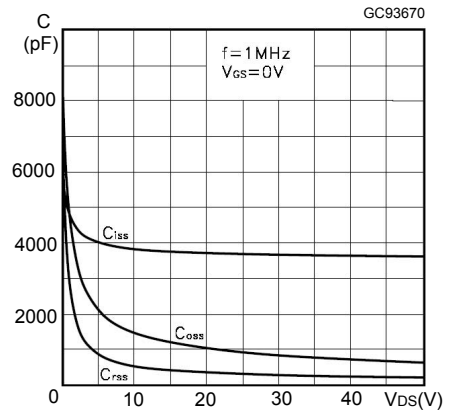
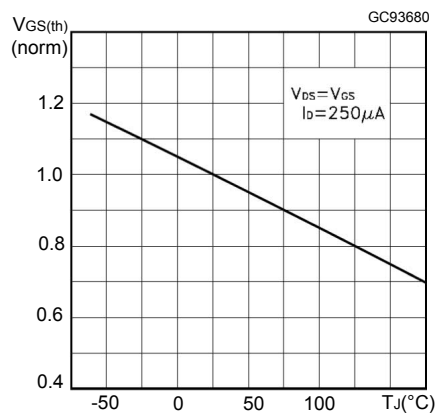
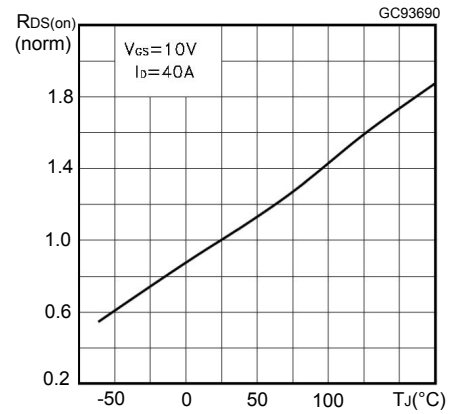
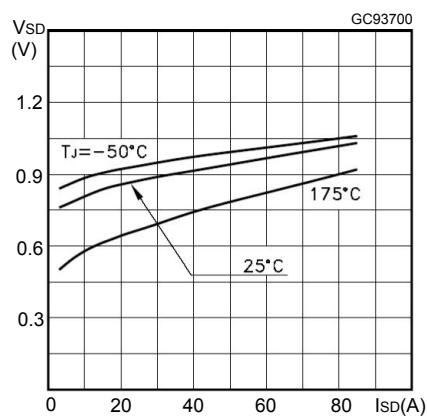
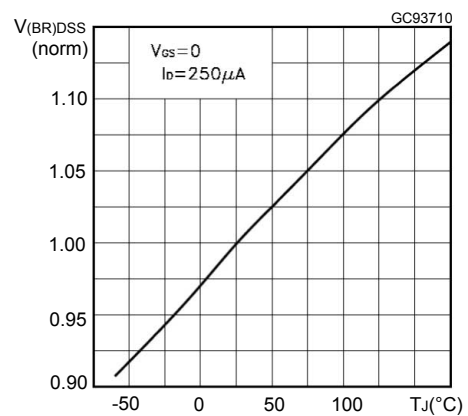
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 80 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 25 \text{ V}$ , $T_J = 150 \text{ }^\circ\text{C}$ (see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	75		ns
$Q_{rr}$	Reverse recovery charge		-	210		nC
$I_{RRM}$	Reverse recovery current		-	5.5		A

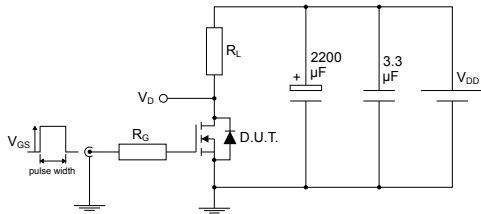
1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

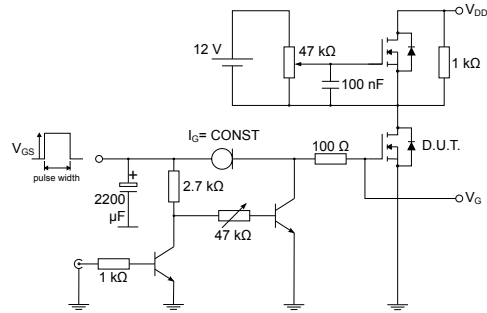
**Figure 1. Safe operating area**

**Figure 2. Thermal impedance**

**Figure 3. Output characteristics**

**Figure 4. Transfer characteristics**

**Figure 5. Transconductance**

**Figure 6. Static drain-source on-resistance**


**Figure 7. Gate charge vs gate-source voltage**

**Figure 8. Capacitance variations**

**Figure 9. Normalized gate threshold voltage vs temperature**

**Figure 10. Normalized on-resistance vs temperature**

**Figure 11. Source-drain diode forward characteristics**

**Figure 12. Normalized  $V_{(BR)DSS}$  vs temperature**


### 3 Test circuits

**Figure 13. Test circuit for resistive load switching times**


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**Figure 14. Test circuit for gate charge behavior**


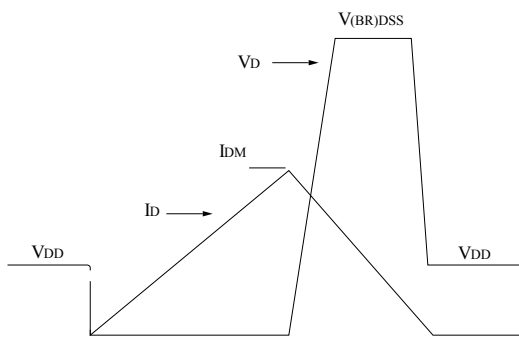
AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**

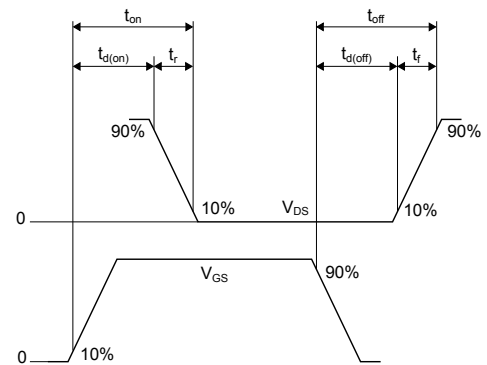

AM01470v1

**Figure 16. Unclamped inductive load test circuit**


AM01471v1

**Figure 17. Unclamped inductive waveform**


AM01472v1

**Figure 18. Switching time waveform**


AM01473v1

## 4 Package information

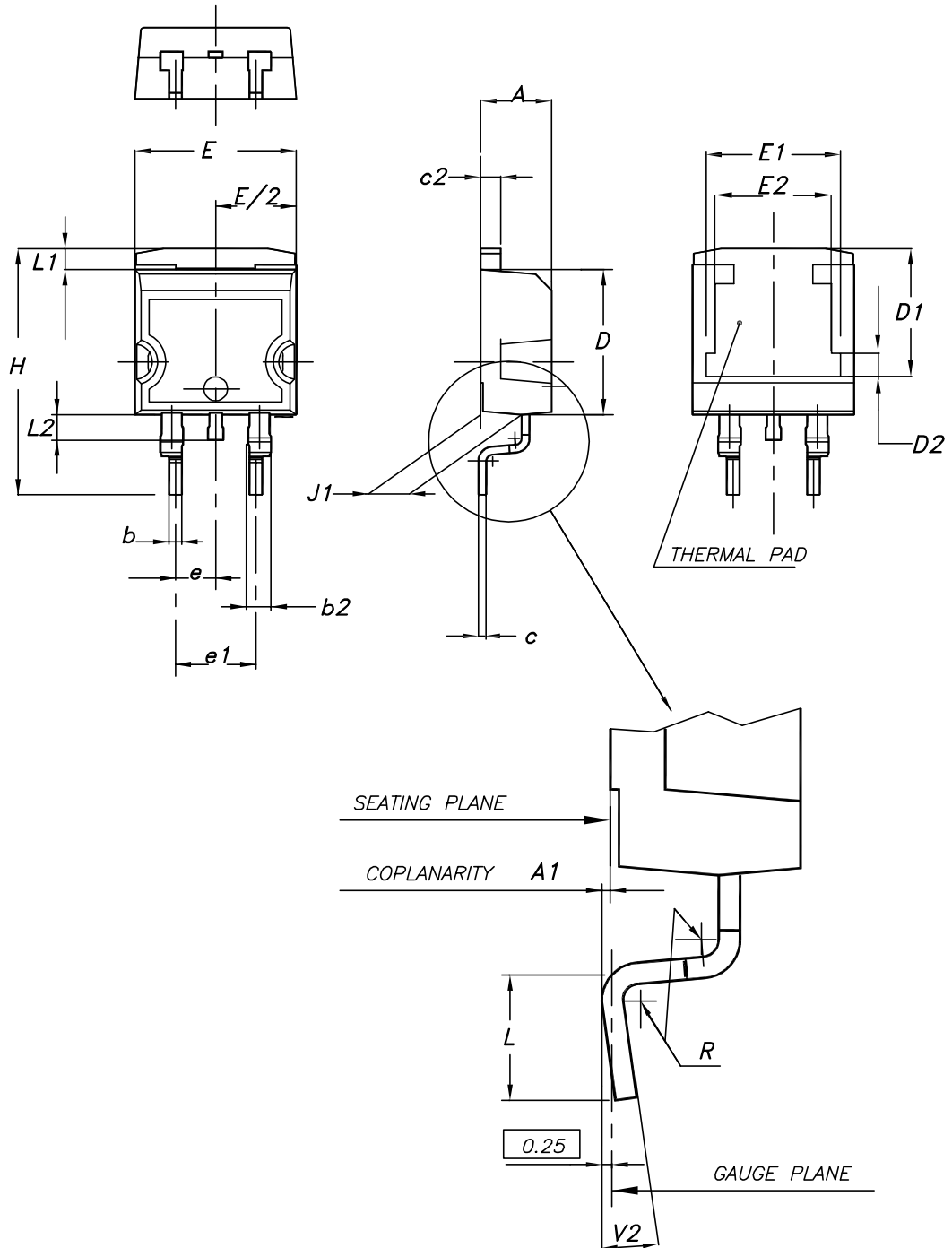
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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.



#### 4.1 D<sup>2</sup>PAK (TO-263) type A package information

Figure 19. D<sup>2</sup>PAK (TO-263) type A package outline

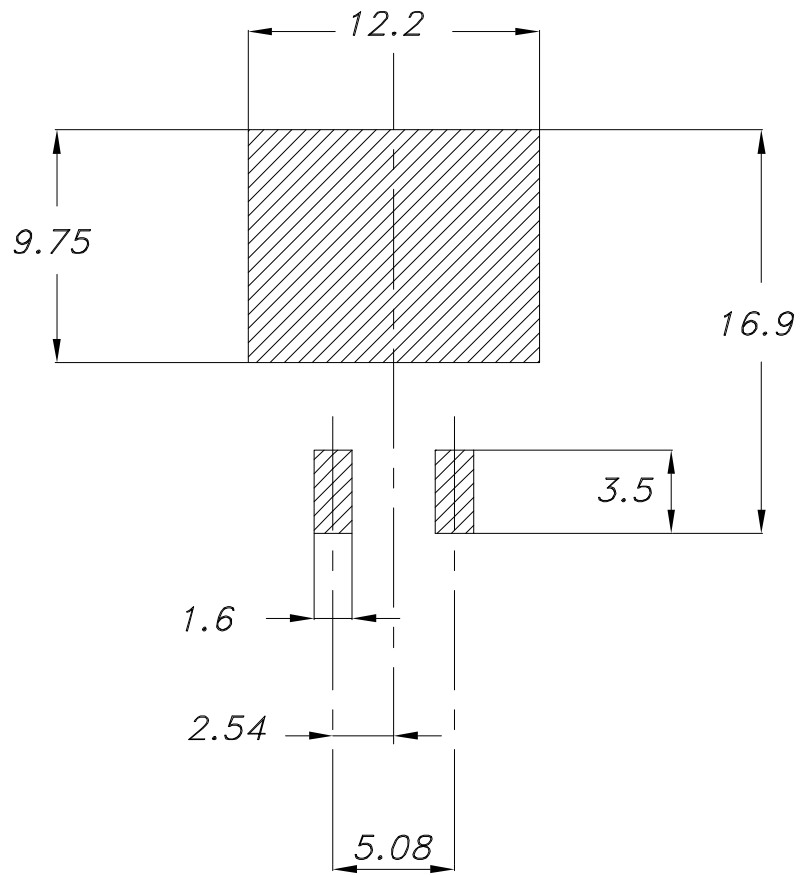


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**Table 7. D<sup>2</sup>PAK (TO-263) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

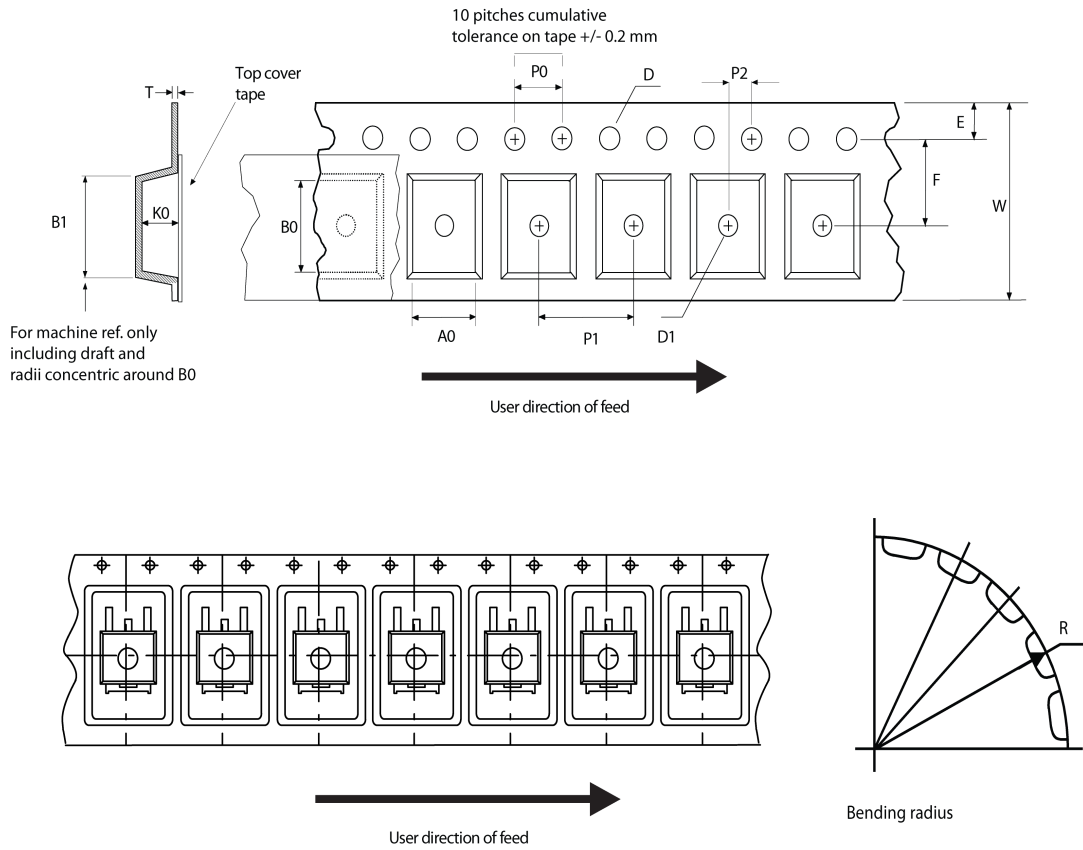
**Figure 20. D<sup>2</sup>PAK (TO-263) recommended footprint (dimensions are in mm)**



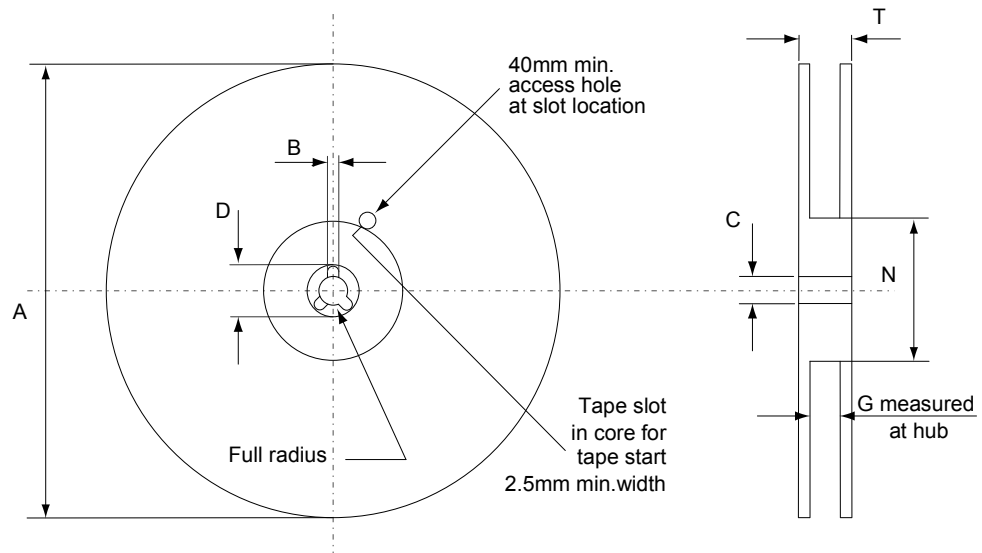
Footprint

## 4.2 D<sup>2</sup>PAK packing information

**Figure 21. D<sup>2</sup>PAK tape outline**



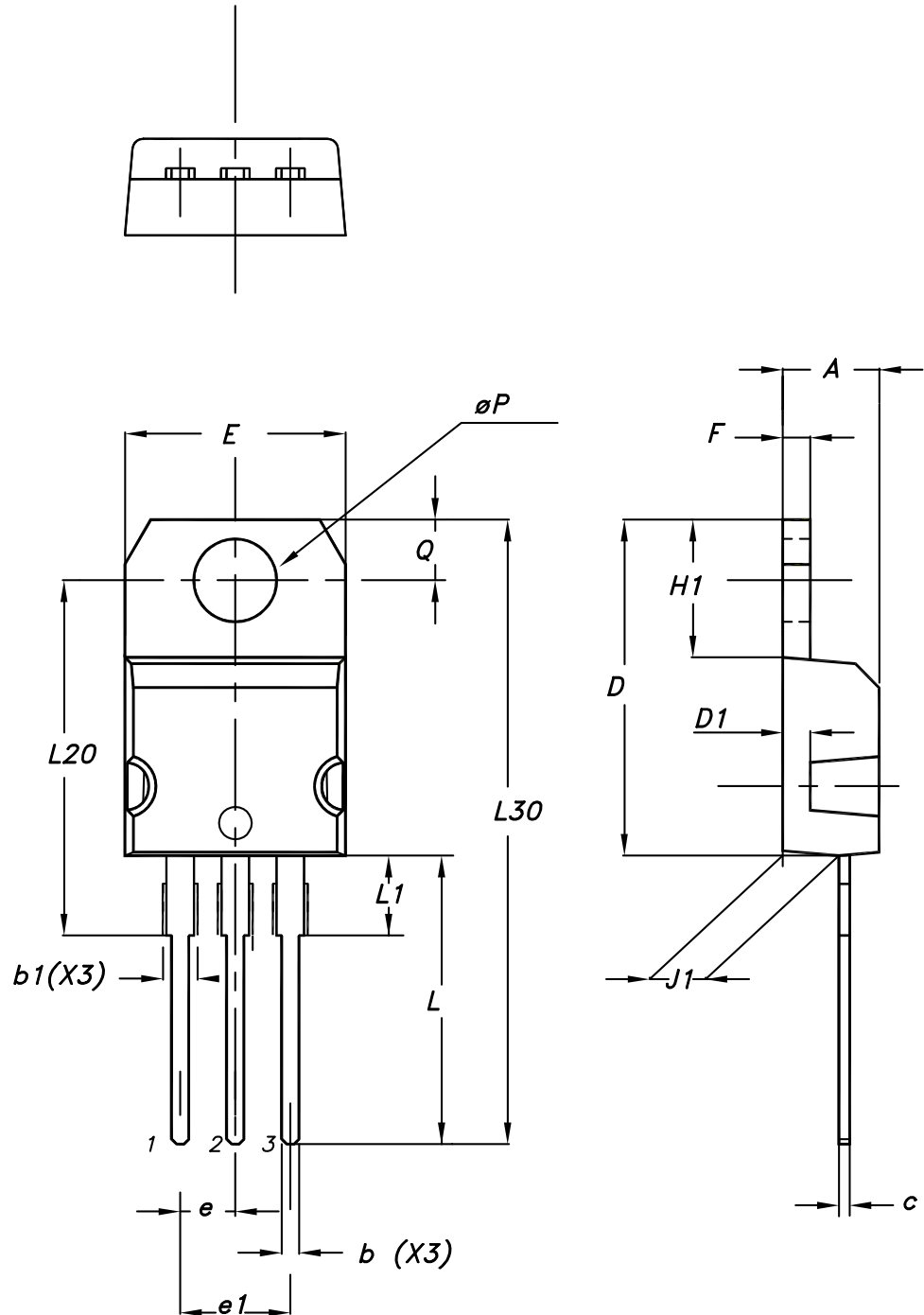
AM08852v1

**Figure 22. D<sup>2</sup>PAK reel outline**


AM06038v1

**Table 8. D<sup>2</sup>PAK tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1	Base quantity		
P1	11.9	12.1			
P2	1.9	2.1	Bulk quantity		
R	50				
T	0.25	0.35			
W	23.7	24.3			

**4.3 TO-220 type A package information**
**Figure 23. TO-220 type A package outline**


0015988\_typeA\_Rev\_22

**Table 9. TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

## Revision history

**Table 10. Document revision history**

Date	Version	Changes
21-Jun-2004	8	Updated SOA and application.
01-Oct-2009	9	Added new device in I <sup>2</sup> PAK
10-Jul-2013	10	– Minor text changes – Updated: <i>Section 4: Package mechanical data</i> and <i>Section 5: Packaging mechanical data</i>
17-Jul-2013	11	– Minor text changes – Modified: order code for D2PAK
16-Jan-2019	12	Modified <a href="#">Table 6. Source-drain diode</a> . Updated <a href="#">Section 4.1 D<sup>2</sup>PAK (TO-263) type A package information</a> and <a href="#">Section 4.3 TO-220 type A package information</a> . Minor text changes.



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