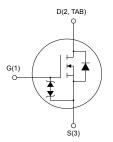


# N-channel 650 V, 1.4 Ω typ., 3.5 A MDmesh™ M6 Power MOSFET in a DPAK package

# TAB O 1 2 3





# Product status link STD3N65M6

Product summary			
Order code	STD3N65M6		
Marking	3N65M6		
Package	DPAK		
Packing	Tube		

#### **Features**

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD3N65M6	650 V	1.5 Ω	3.5 A

- · Reduced switching losses
- Lower R<sub>DS(on)</sub> per area vs previous generation
- · Low gate input resistance
- 100% avalanche tested
- · Zener-protected

#### **Applications**

· Switching applications

#### **Description**

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs.

STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent  $R_{DS(on)}$  per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.



# 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>GS</sub>	Gate-source voltage	±25	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	3.5	Α
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	2.2	Α
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	14	Α
P <sub>TOT</sub>	Total power dissipation at T <sub>C</sub> = 25 °C	45	W
dv/dt (2)	Peak diode recovery voltage slope	5	V/ns
dv/dt (3)	MOSFET dv/dt ruggedness	100	V/115
T <sub>J</sub>	Operating junction temperature range	-55 to 150	°C
T <sub>stg</sub>	Storage temperature range	-33 to 130	

- 1. Pulse width limited by safe operating area
- 2.  $I_{SD} \le 3.5 \, A$ ,  $di/dt=400 \, A/\mu s$ ;  $V_{DS \, peak} < V_{(BR)DSS}$ ,  $V_{DD} = 400 \, V$
- 3.  $V_{DS} \le 520 \text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	2.78	°C/W
R <sub>thj-pcb</sub> (1)	Thermal resistance junction-pcb	50	C/VV

1. When mounted on FR-4 board of inch², 2oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	1	Α
E <sub>AS</sub>	Single pulse avalanche energy (starting $T_j$ =25°C, $I_D$ = $I_{AR}$ , $V_{DD}$ =50 V)	78	mJ

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#### 2 Electrical characteristics

 $T_C$  = 25 °C unless otherwise specified

Table 4. On/off-state

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	$V_{GS}$ = 0 V, $I_D$ = 1 mA	650			V
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 650 V			1	μA
I <sub>DSS</sub>	Zero gate voltage drain current	$V_{GS}$ = 0 V, $V_{DS}$ = 650 V, $T_{C}$ = 125 °C <sup>(1)</sup>			100	μΑ
I <sub>GSS</sub>	Gate body leakage current	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 25 \text{ V}$			±5	μA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	2.25	3	3.75	V
R <sub>DS(on)</sub>	Static drain-source on-resistance	$V_{GS}$ = 10 V, $I_{D}$ = 1.75 A		1.4	1.5	Ω

<sup>1.</sup> Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		-	150	-	pF
C <sub>oss</sub>	Output capacitance	V <sub>DS</sub> = 100 V, f = 1 MHz, V <sub>GS</sub> = 0 V	-	13	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	0.7	-	pF
Coss eq. (1)	Equivalent output capacitance	V <sub>DS</sub> = 0 to 520 V, V <sub>GS</sub> = 0 V	-	31	-	pF
R <sub>G</sub>	Intrinsic gate resistance	f = 1 MHz, I <sub>D</sub> =0 A	-	5.2	-	Ω
Qg	Total gate charge	V <sub>DD</sub> = 520 V, I <sub>D</sub> = 3.5 A,	-	6	-	nC
Q <sub>gs</sub>	Gate-source charge	V <sub>GS</sub> = 0 to10 V, (see Figure 14. Test circuit for gate charge behavior)	-	1	-	nC
Q <sub>gd</sub>	Gate-drain charge		-	3.2	-	nC

C<sub>oss eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oss</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	$V_{DD}$ = 325 V, $I_{D}$ = 1.75 A,	-	5.2	-	ns
t <sub>r</sub>	Rise time	$R_G = 4.7 \Omega$ , $V_{GS} = 10 V$ (see Figure 13. Test circuit	-	5.4	-	ns
t <sub>d(off)</sub>	Turn-off delay time	for resistive load switching times and	-	14.1	-	ns
t <sub>f</sub>	Fall time	Figure 18. Switching time waveform )	-	17.1	-	ns

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Table 7. Source-drain diode

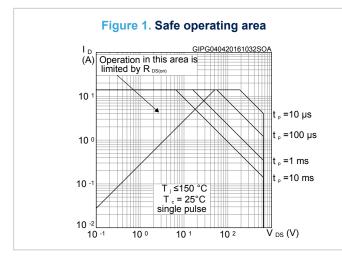
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		-		3.5	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		14	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	$I_{SD} = 3.5 \text{ A}, V_{GS} = 0 \text{ V}$	-		1.6	V
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 3.5 \text{ A}, \text{ di/dt} = 100$	-	159		ns
Q <sub>rr</sub>	Reverse recovery charge	A/μs, V <sub>DD</sub> = 60 V, (see ) Figure 15. Test circuit for	-	0.7		μC
I <sub>RRM</sub>	Reverse recovery current	inductive load switching and diode recovery times	-	8.9		Α
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 3.5 \text{ A}, \text{ di/dt} = 100$	-	190		ns
Q <sub>rr</sub>	Reverse recovery charge	A/ $\mu$ s, V <sub>DD</sub> = 60 V, T <sub>j</sub> = 150 °C (see ) Figure 15. Test	-	0.8		μC
I <sub>RRM</sub>	Reverse recovery current	circuit for inductive load switching and diode recovery times	_	8.5		Α

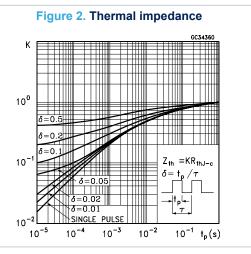
<sup>1.</sup> Pulse width limited by safe operating area

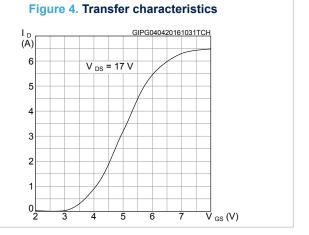
<sup>2.</sup> Pulsed: pulse duration = 300 µs, duty cycle 1.5%

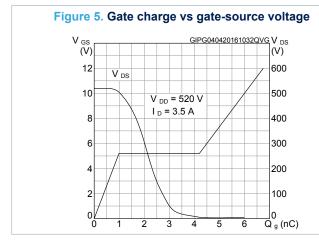


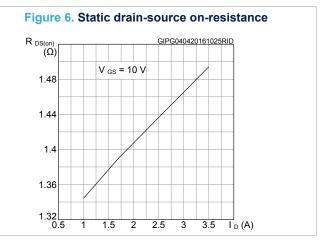
#### 2.1 Electrical characteristics (curves)











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Figure 7. Capacitance variations

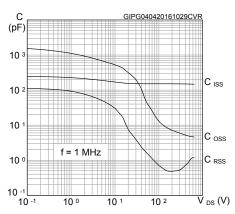


Figure 8. Normalized gate threshold voltage vs temperature

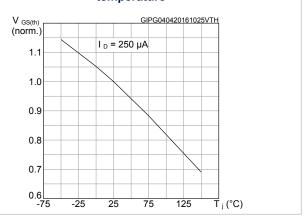


Figure 9. Normalized on-resistance vs temperature

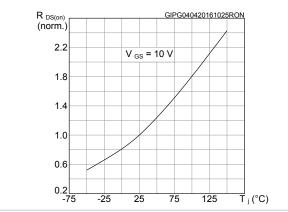


Figure 10. Normalized  $V_{(BR)DSS}$  vs temperature

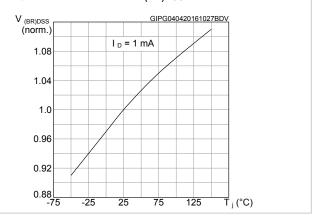


Figure 11. Output capacitance stored energy

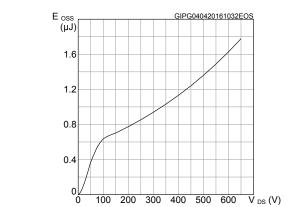
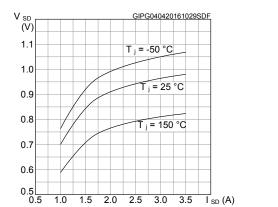


Figure 12. Source-drain diode forward characteristics



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#### 3 Test circuits

Figure 13. Test circuit for resistive load switching times

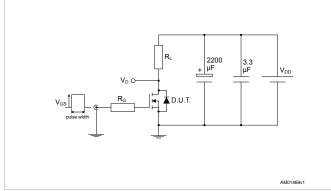


Figure 14. Test circuit for gate charge behavior

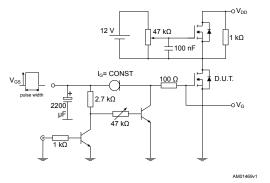


Figure 15. Test circuit for inductive load switching and diode recovery times

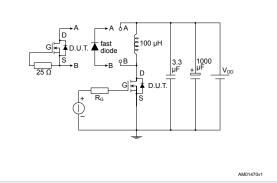


Figure 16. Unclamped inductive load test circuit

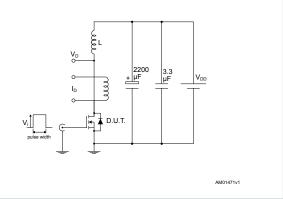


Figure 17. Unclamped inductive waveform

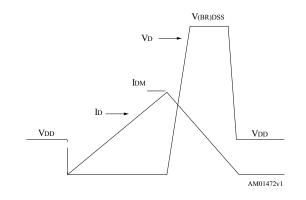
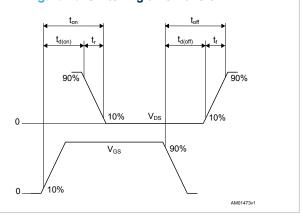


Figure 18. Switching time waveform



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## 4 Package information

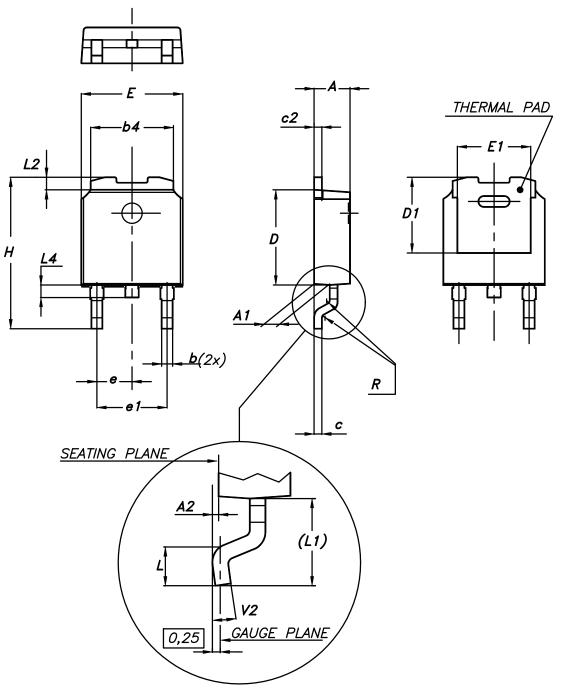
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

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## 4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



0068772\_A\_26



Table 8. DPAK (TO-252) type A mechanical data

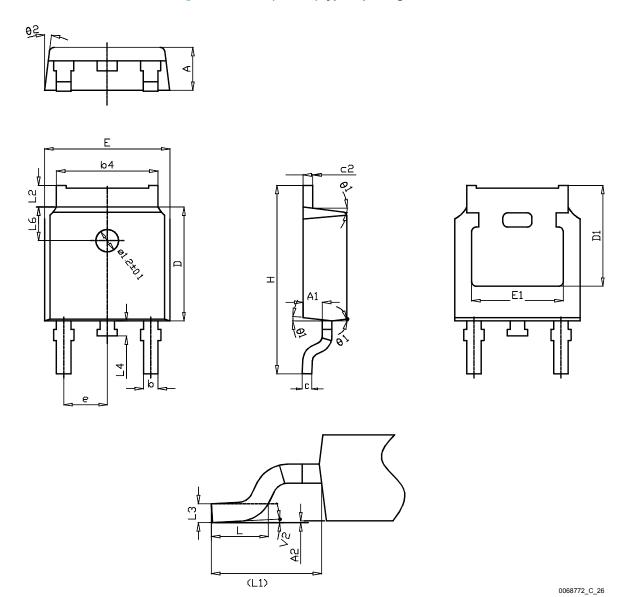
Dim.		mm	
Dim.	Min.	Тур.	Max.
А	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
е	2.159	2.286	2.413
e1	4.445	4.572	4.699
Н	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

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# 4.2 DPAK (TO-252) type C package information

Figure 20. DPAK (TO-252) type C package outline



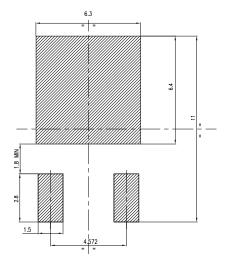
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Table 9. DPAK (TO-252) type C mechanical data

Dim.		mm		
DIM.	Min.	Тур.	Max.	
Α	2.20	2.30	2.38	
A1	0.90	1.01	1.10	
A2	0.00		0.10	
b	0.72		0.85	
b4	5.13	5.33	5.46	
С	0.47		0.60	
c2	0.47		0.60	
D	6.00	6.10	6.20	
D1	5.25			
Е	6.50	6.60	6.70	
E1	4.70			
е	2.186	2.286	2.386	
Н	9.80	10.10	10.40	
L	1.40	1.50	1.70	
L1		2.90 REF		
L2	0.90		1.25	
L3		0.51 BSC		
L4	0.60	0.80	1.00	
L6	1.80 BSC			
θ1	5°	7°	9°	
θ2	5°	7°	9°	
V2	0°		8°	

Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)

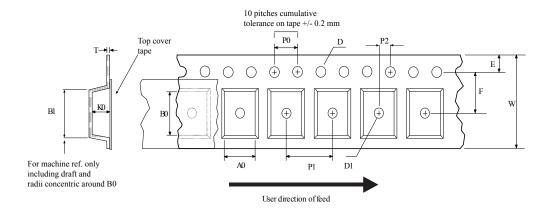


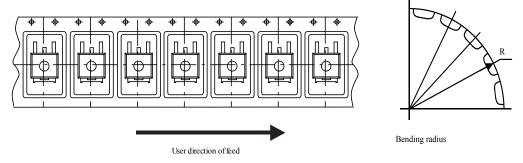
FP\_0068772\_26\_C



#### 4.3 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



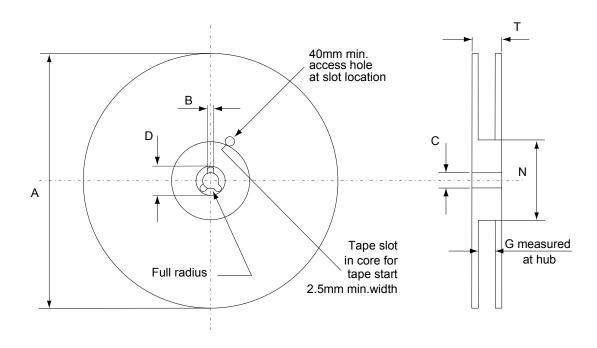


AM08852v1

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Figure 23. DPAK (TO-252) reel outline



AM06038v1

Table 10. DPAK (TO-252) tape and reel mechanical data

Таре			Reel		
Dim.	mm		Dim.		mm
Dim.	Min.	Max.	Biiii.	Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Bas	e qty.	2500
P1	7.9	8.1	Bull	k qty.	2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

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## **Revision history**

**Table 11. Document revision history** 

Date	Revision	Changes
02-May-2016	1	Initial release.
22-Nov-2018	2	Added Section 4.2 DPAK (TO-252) type C package information.
22-NOV-2016		Minor text changes to improve readability.

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