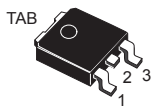
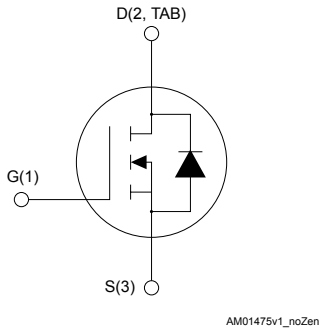
Datasheet

Automotive-grade N-channel 60 V, 0.07 Ω typ., 12 A STripFET II Power MOSFET in a DPAK package



DPAK



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD12NF06LAG	60 V	0.09 Ω	12 A

- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link
STD12NF06LAG

Product summary	
Order code	STD12NF06LAG
Marking	D12NF06L
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±16	V
I_D	Drain current (continuous) at T_{case} = 25 °C	12	A
	Drain current (continuous) at T_{case} = 100 °C	8.5	
I_{DM}(1)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	30	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
E_{AS}(3)	Single pulse avalanche energy	100	mJ
T_{stg}	Storage temperature range	-55 to 175	°C
T_J	Operating junction temperature range		

1. *Pulse width is limited by safe operating area.*
2. *I_{SD} ≤ 12 A, di/dt ≤ 200 A/µs, V_{DS} ≤ 40 V, T_J ≤ T_{JMAX}*
3. *Starting T_j = 25 °C, I_D = 6 A, V_{DD} = 30 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	5	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50	

1. *When mounted on a 1-inch² FR-4, 2 Oz copper board.*

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
		V_{GS} = 0 V, V_{DS} = 60 V, T_{case} = 125 °C(1)			10	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 6 A		70	90	mΩ
		V_{GS} = 5 V, I_D = 6 A		80	100	

1. *Defined by design, not subject to production test.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	350		pF
C_{oss}	Output capacitance		-	75		
C_{rss}	Reverse transfer capacitance		-	30		
Q_g	Total gate charge	V_{DD} = 48 V, I_D = 12 A, V_{GS} = 0 to 5 V (see Figure 13. Test circuit for gate charge behavior)	-	7.5	10	nC
Q_{gs}	Gate-source charge		-	2.5		
Q_{gd}	Gate-drain charge		-	3.0		

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 6 A, R_G = 4.7 Ω, V_{GS} = 4.5 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	10	-	ns
t_r	Rise time		-	35	-	
$t_{d(off)}$	Turn-off delay time		-	20	-	
t_f	Fall time		-	13	-	

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}(1)	Source-drain current (pulsed)		-		48	A
V_{SD}(2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 12 A	-		1.5	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	I_{SD} = 12 A, di/dt = 100 A/µs,	-	50		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 16 V, T_J = 150 °C	-	65		nC
I_{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	2.5		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

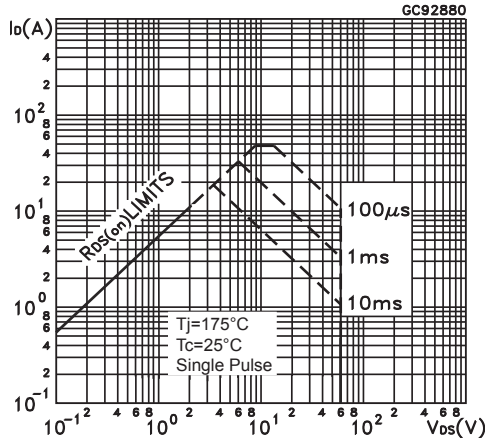


Figure 2. Thermal impedance

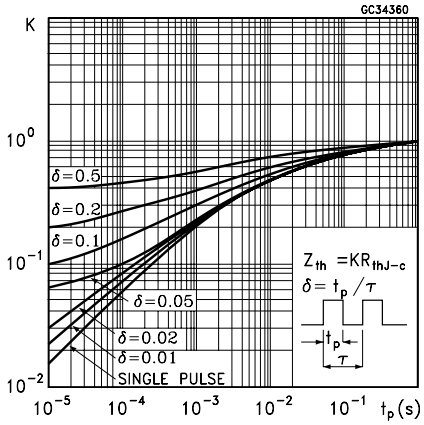


Figure 3. Output characteristics

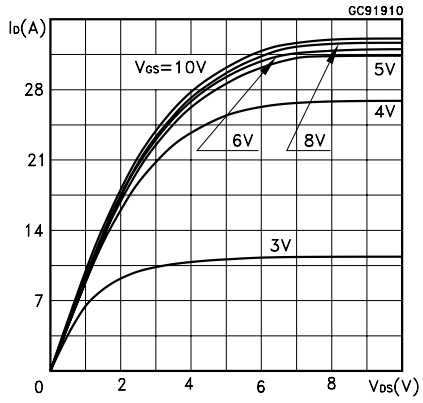


Figure 4. Transfer characteristics

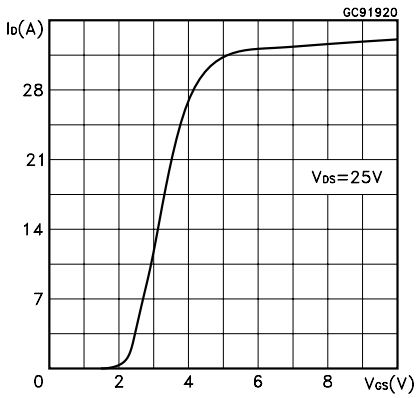


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

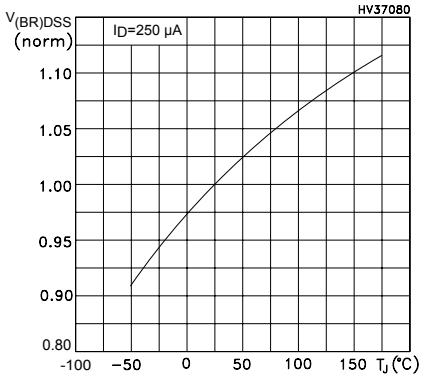


Figure 6. Static drain-source on-resistance

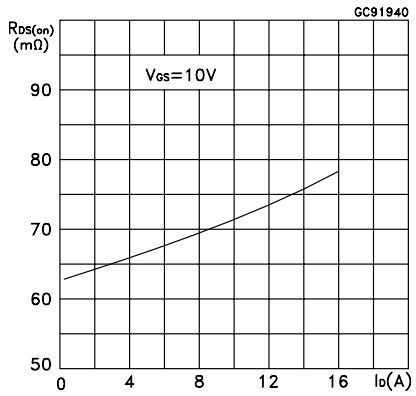


Figure 7. Gate charge vs gate-source voltage

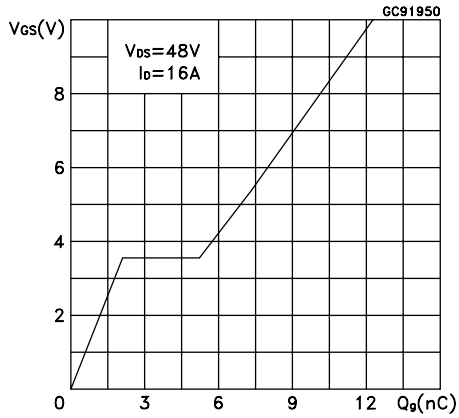


Figure 8. Capacitance variations

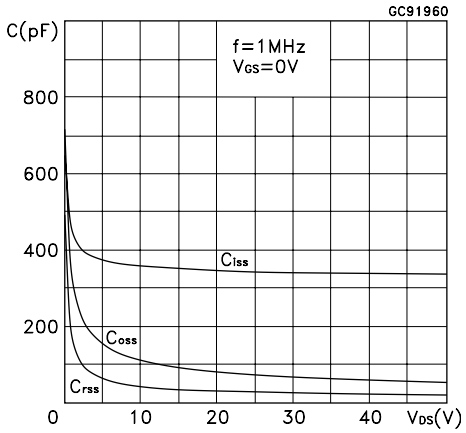


Figure 9. Normalized gate threshold vs temperature

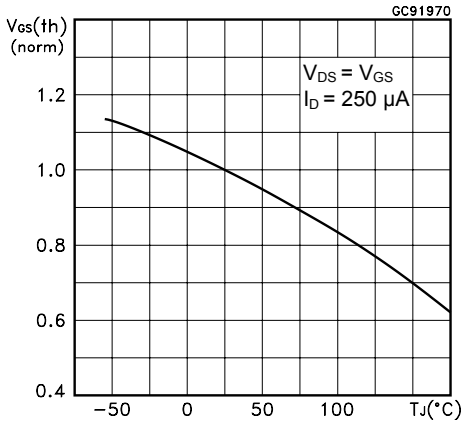


Figure 10. Normalized on-resistance vs temperature

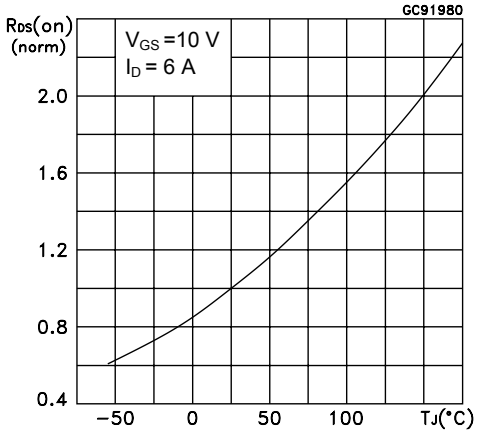
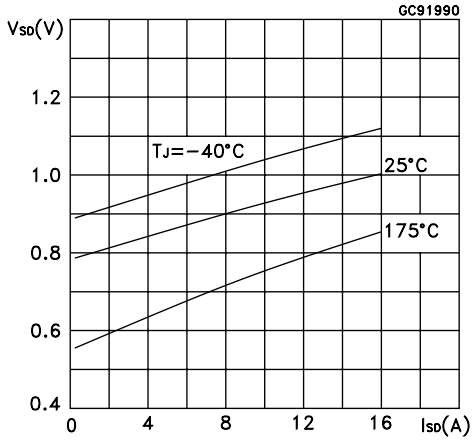


Figure 11. Source-drain diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

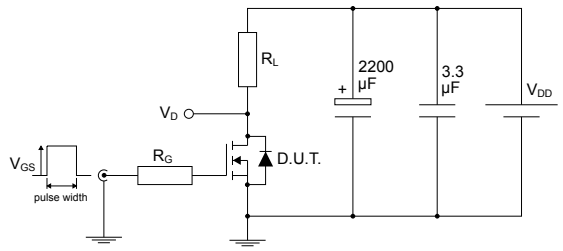


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Figure 13. Test circuit for gate charge behavior

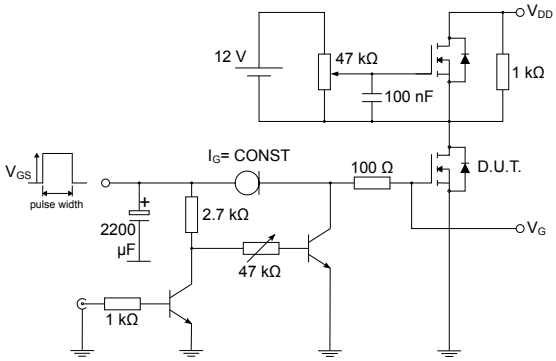

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Figure 14. Test circuit for inductive load switching and diode recovery times

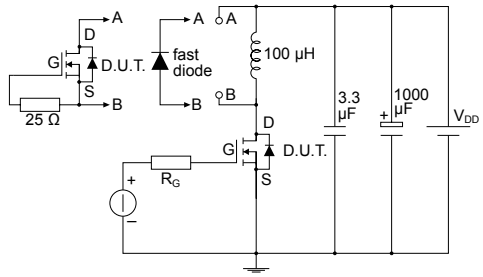

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Figure 15. Unclamped inductive load test circuit

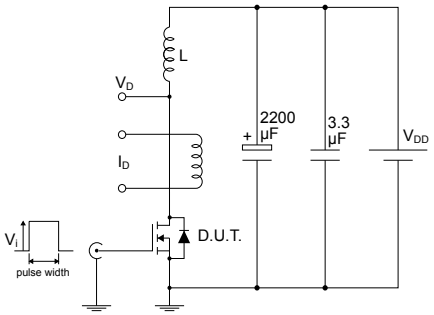

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Figure 16. Unclamped inductive waveform

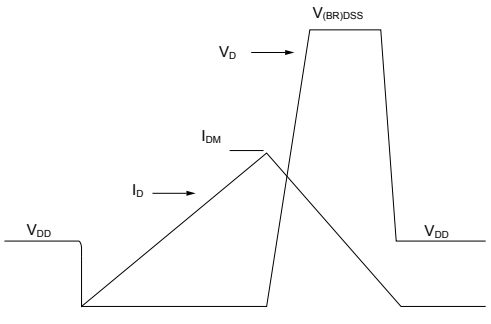

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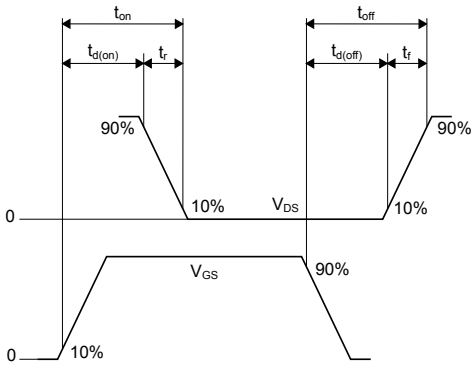
Figure 17. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) package information

Figure 18. **DPAK (TO-252) type A package outline**

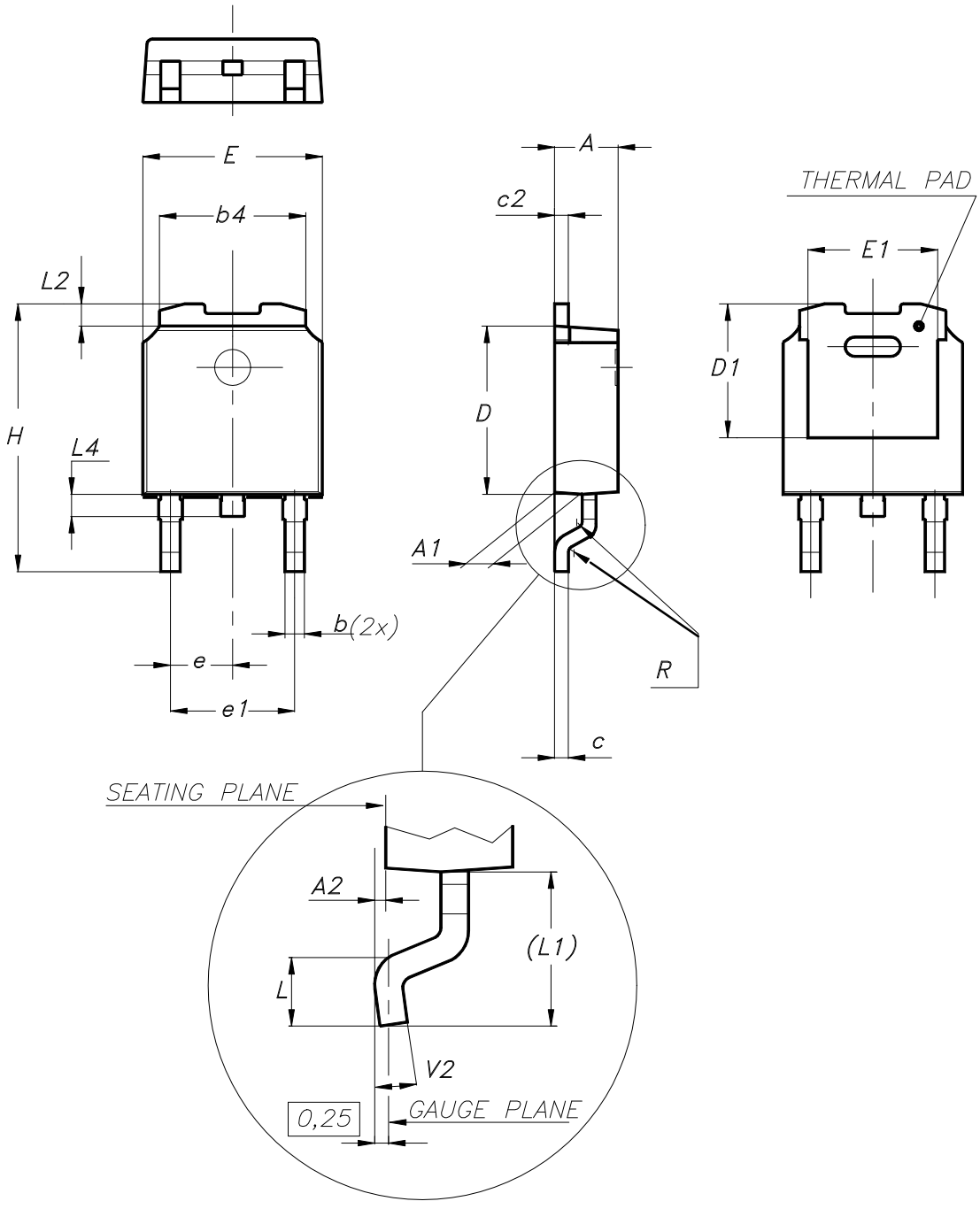

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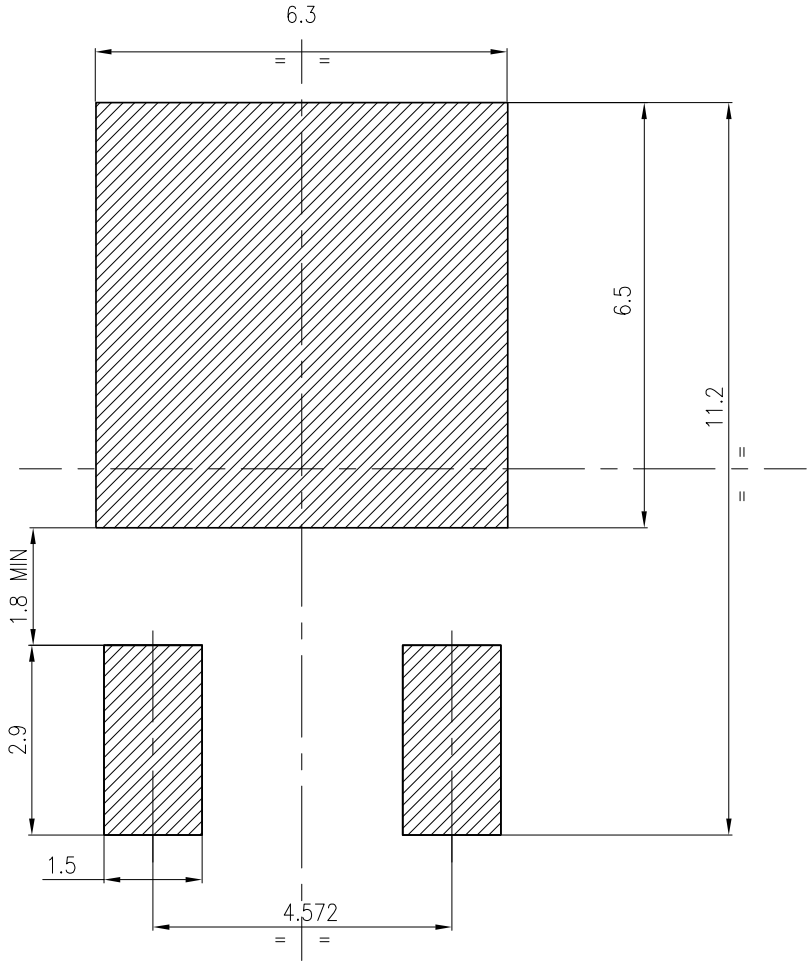
Table 7. **DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 19. **DPAK (TO-252) recommended footprint (dimensions are in mm)**



4.2 DPAK (TO-252) packing information

Figure 20. **DPAK (TO-252) tape outline**

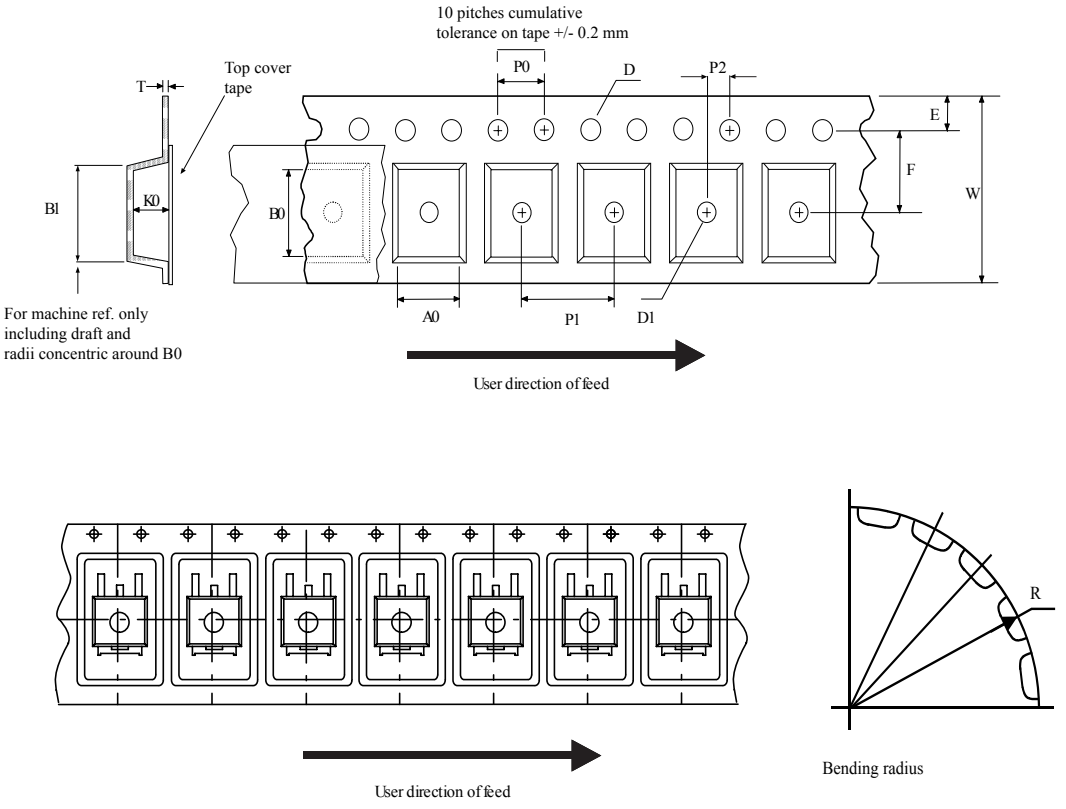


Figure 21. **DPAK (TO-252) reel outline**

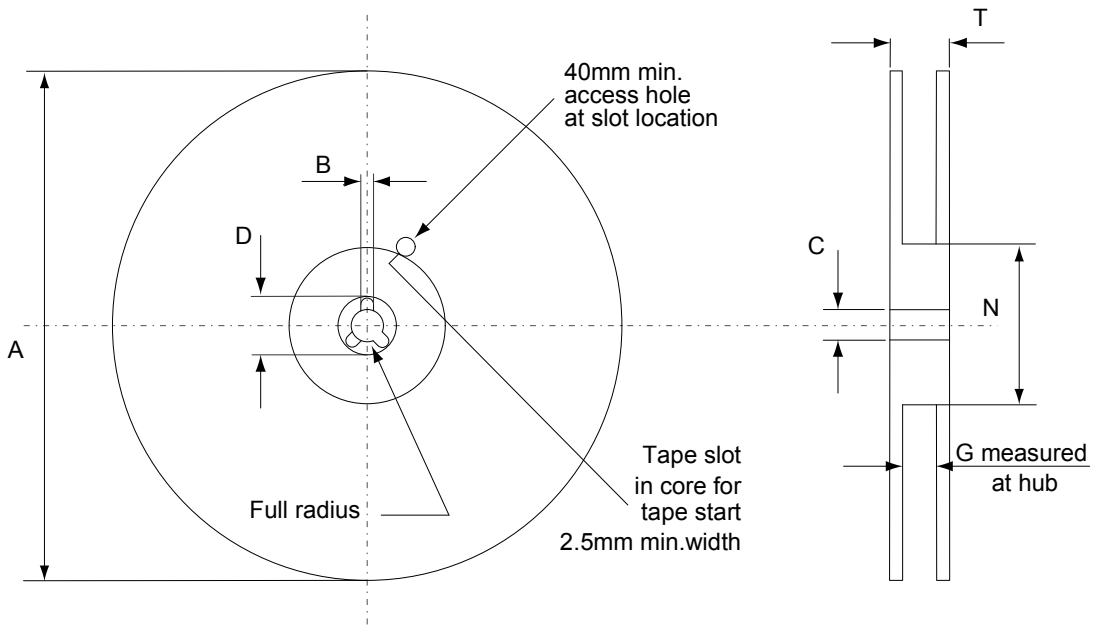


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Table 8. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 9. **Document revision history**

Date	Revision	Changes
15-Feb-2017	1	First release
10-Jun-2019	2	New template. Minor changes.
19-Nov-2021	3	Updated features table in cover page.

Contents