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ON Semiconductor®

FDS6673BZ-F085

P-Channel PowerTrench® MOSFET -30V, -14.5A, 7.8m Ω

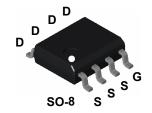
General Description

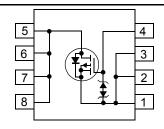
This P-Channel MOSFET is produced using ON Semiconductor's advanced Power Trench process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Features

- $\text{Max r}_{\text{DS(on)}} = 7.8 \text{m}\Omega, V_{\text{GS}} = -10 \text{V}, I_{\text{D}} = -14.5 \text{A}$
- Max $r_{DS(on)} = 12m\Omega$, $V_{GS} = -4.5V$, $I_D = -12A$
- Extended V_{GS} range (-25V) for battery applications
- HBM ESD protection level of 6.5kV typical (note 3)
- High performance trench technology for extremely low rDS(on)
- High power and current handling capability
- RoHS compliant
- Qualified to AEC Q101





MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	±25	V
	Drain Current -Continuous (Note1	a) -14.5	Α
ID	-Pulsed	-75	Α
	Power Dissipation for Single Operation (Note	la) 2.5	
P_{D}	(Note	lb) 1.2	W
	(Note	1c) 1.0	
T _J , T _{STG}	Operating and Storage Temperature	-55 to 150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance , Junction to Ambient (Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance , Junction to Case (Note 1)	25	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
FDS6673BZ	FDS6673BZ-F085	13"	12mm	2500 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Parameter

Off Characteristics								
B _{VDSS}	Drain to Source Breakdown Voltage	$I_D = -250 \mu A, V_{GS} = 0 V$	-30			V		
$\frac{\Delta B_{VDSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu A$, referenced to 25°C		-20		mV/°C		
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$			-1	μΑ		
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25V, V_{DS} = 0V$			±10	μΑ		

Test Conditions

Min

Тур

Max

Units

On Characteristics (Note 2)

Symbol

V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250 \mu A$	-1	-1.9	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250μA, referenced to 25°C		8.1		mV/°C
	Drain to Source On Resistance	$V_{GS} = -10V$, $I_D = -14.5A$		6.5	7.8	
rno()		$V_{GS} = -4.5V, I_D = -12A$		9.6	12	mΩ
r _{DS(on)}		$V_{GS} = -10V, I_D = -14.5A$ $T_J = 125$ °C		9.7	12	- 11152
9 _{FS}	Forward Transconductance	$V_{DS} = -5V, I_{D} = -14.5A$		60		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 45V V 0V	3500	4700	pF
C _{oss}	Output Capacitance	V _{DS} = -15V, V _{GS} = 0V, f = 1.0MHz	600	800	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1.0111112	600	900	pF

Switching Characteristics (Note 2)

t _{d(on)}	Turn-On Delay Time		14	26	ns
t _r	Rise Time	$V_{DD} = -15V, I_{D} = -1A$ $V_{GS} = -10V, R_{GS} = 6\Omega$	16	29	ns
t _{d(off)}	Turn-Off Delay Time	V _{GS} = -10V, n _{GS} = 612	225	306	ns
t _f	Fall Time		105	167	ns
Qg	Total Gate Charge	$V_{DS} = -15V, V_{GS} = -10V,$ $I_{D} = -14.5A$	88	124	nC
Q_g	Total Gate Charge	V 45V V 5V	46	65	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DS} = -15V, V_{GS} = -5V,$ $I_{D} = -14.5A$	8		nC
Q_{gd}	Gate to Drain Charge	ID = -14.5A	23.5		nC

Drain-Source Diode Characteristics

V	SD	Source to Drain Diode Forward Voltage	$V_{GS} = 0V, I_S = -2.1A$	-0.7	-1.2	V
t _{rr}	r	Reverse Recovery Time	$I_F = 14.5A$, $di/dt = 100A/\mu s$		45	ns
Q	rr	Reverse Recovery Charge	$I_F = 14.5A$, $di/dt = 100A/\mu s$		34	nC

1: R_{0JA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0JC} is guaranteed by design while R_{0CA} is determined by the user's board design.



a) 50 °C/W (10 sec) when mounted on a 1 in² pad of 2 oz copper



b) 105 °C/W when mounted on a .04 in² pad of 2 oz copper



Scale 1: 1 on letter size paper

- 2: Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%.
- 3: The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25°C unless otherwise noted

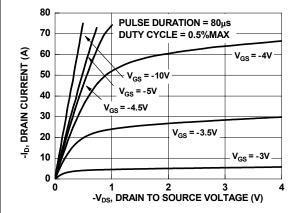


Figure 1. On Region Characteristics

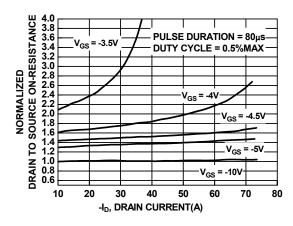


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

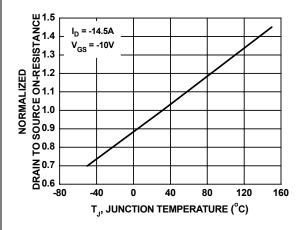


Figure 3. Normalized On Resistance vs Junction Temperature

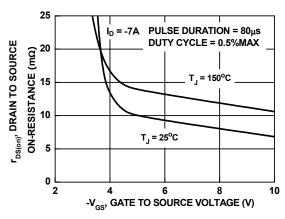


Figure 4. On-Resistance vs Gate to Source Voltage

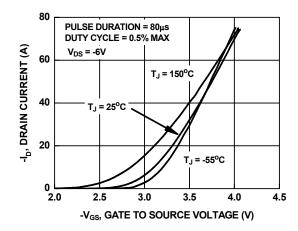


Figure 5. Transfer Characteristics

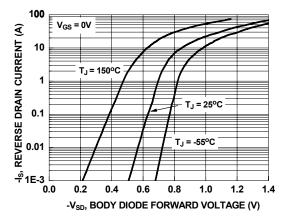
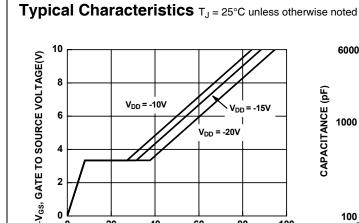


Figure 6. Source to Drain Diode Forward Voltage vs Source Current



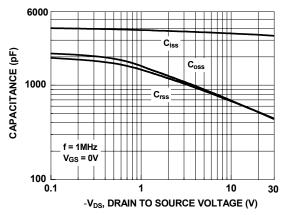


Figure 7. Gate Charge Characteristics

Qg, GATE CHARGE(nC)

60

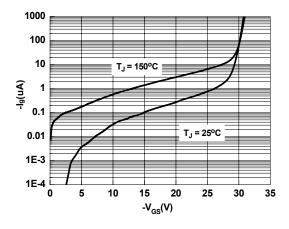
80

100

0

20

Figure 8. Capacitance vs Drain to Source Voltage



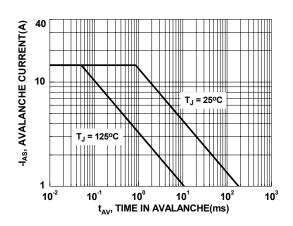
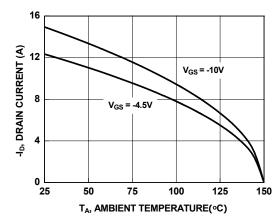


Figure 9. $I_g vs V_{GS}$

Figure 10. Unclamped Inductive Switching Capability



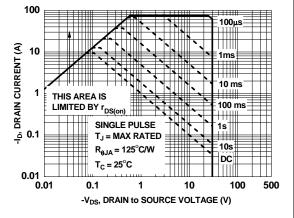


Figure 11. Maximum Continuous Drain Current vs **Ambient Temperature**

Figure 12. Forward Bias Safe Operating Area

Typical Characteristics T_J = 25 °C unless otherwise noted

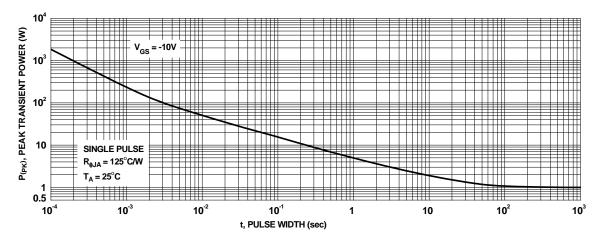


Figure 13. Junction-to-Case Transient Thermal Response Curve

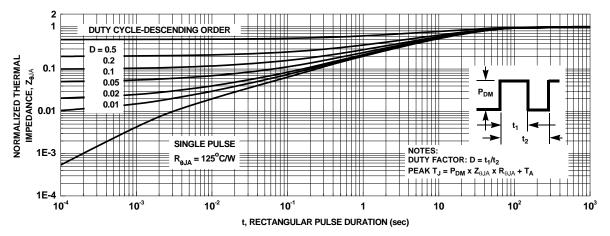


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

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