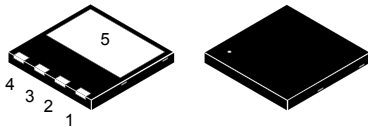
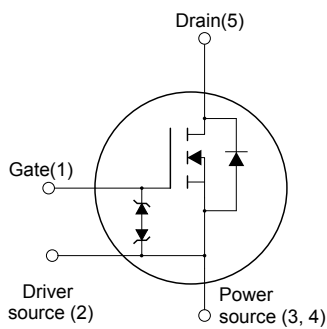


## N-channel 600 V, 0.115 $\Omega$ typ., 21 A MDmesh™ M6 Power MOSFET in a PowerFLAT™ 8x8 HV package



PowerFLAT™ 8x8 HV



NG1DS2PS34D5Z

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL33N60M6	600 V	137 m $\Omega$	21 A

- Reduced switching losses
- Lower R<sub>DS(on)</sub> per area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications
- LLC converters
- Boost PFC converters

### Description

The new MDmesh™ M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent R<sub>DS(on)</sub> per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.

#### Product status link

[STL33N60M6](#)

#### Product summary

<b>Order code</b>	STL33N60M6
<b>Marking</b>	33N60M6
<b>Package</b>	PowerFLAT™ 8x8 HV
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±25	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	21	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	13	
$I_{DM}^{(1)}$	Drain current (pulsed)	78	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ °C}$	150	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET $dv/dt$ ruggedness	50	
$T_{stg}$	Storage temperature range	-55 to 150	°C
$T_j$	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2.  $I_{SD} \leq 21\text{ A}$ ,  $di/dt = 400\text{ A}/\mu\text{s}$ ,  $V_{DS} < V_{(BR)DSS}$ ,  $V_{DD} = 400\text{ V}$
3.  $V_{DS} \leq 480\text{ V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.83	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	45	°C/W

1. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or non-repetitive (pulse width limited by $T_{Jmax}$ )	4	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	500	mJ

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified).

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 1\text{ mA}$	600			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 600\text{ V}$ , $T_{\text{case}} = 125\text{ }^{\circ}\text{C}^{(1)}$			100	
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 25\text{ V}$			$\pm 5$	$\mu\text{A}$
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	3.25	4	4.75	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 10.5\text{ A}$		0.115	0.137	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{ISS}}$	Input capacitance	$V_{\text{DS}} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	1515	-	$\mu\text{F}$
$C_{\text{OSS}}$	Output capacitance		-	128	-	
$C_{\text{RSS}}$	Reverse transfer capacitance		-	4.2	-	
$C_{\text{OSS eq.}}^{(1)}$	Equivalent output capacitance	$V_{\text{DS}} = 0\text{ to }480\text{ V}$ , $V_{\text{GS}} = 0\text{ V}$	-	269	-	$\mu\text{F}$
$R_{\text{G}}$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_{\text{D}} = 0\text{ A}$	-	1.5	-	$\Omega$
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 480\text{ V}$ , $I_{\text{D}} = 25\text{ A}$ ,	-	33.4	-	nC
$Q_{\text{gs}}$	Gate-source charge	$V_{\text{GS}} = 0\text{ to }10\text{ V}$	-	7.2	-	
$Q_{\text{gd}}$	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	16.3	-	

1.  $C_{\text{OSS eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{OSS}}$  when  $V_{\text{DS}}$  increases from 0 to 80%  $V_{\text{DSS}}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{DD}} = 300\text{ V}$ , $I_{\text{D}} = 12.5\text{ A}$ , $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$	-	19.5	-	ns
$t_{\text{r}}$	Rise time		-	33	-	
$t_{\text{d}(\text{off})}$	Turn-off delay time	(see Figure 13. Switching times test circuit for resistive load and Figure 18. Switching time waveform)	-	38.5	-	
$t_{\text{f}}$	Fall time		-	7.5	-	

**Table 7. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		21	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		78	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 21\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	265		ns
$Q_{rr}$	Reverse recovery charge		-	3.07		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	23.2		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 15. Test circuit for inductive load switching and diode recovery times</a> )	-	374		ns
$Q_{rr}$	Reverse recovery charge		-	5.78		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	30.9		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

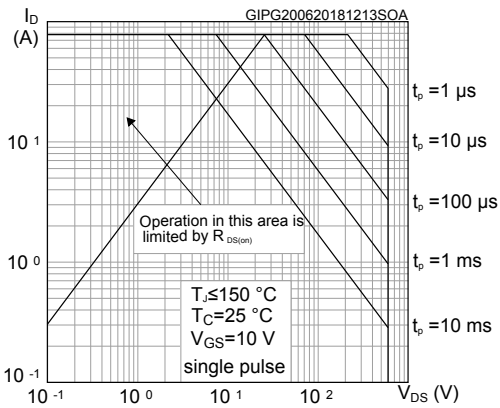


Figure 2. Thermal impedance

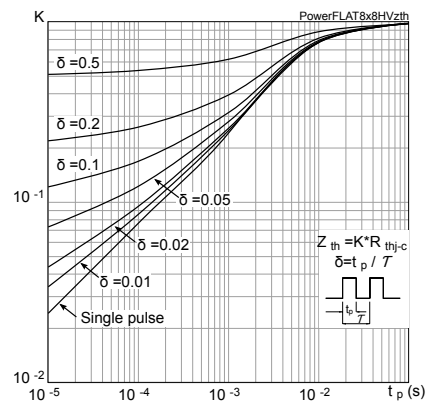


Figure 3. Output characteristics

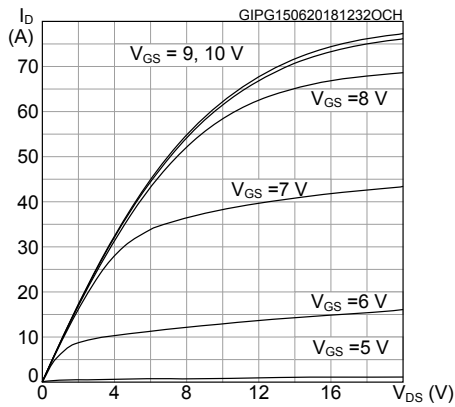


Figure 4. Transfer characteristics

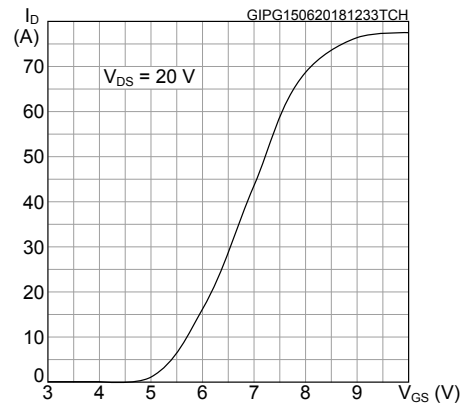


Figure 5. Gate charge vs gate-source voltage

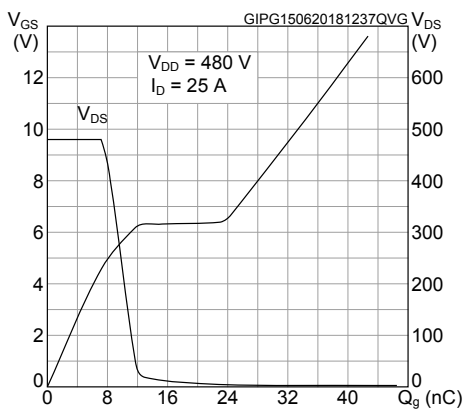
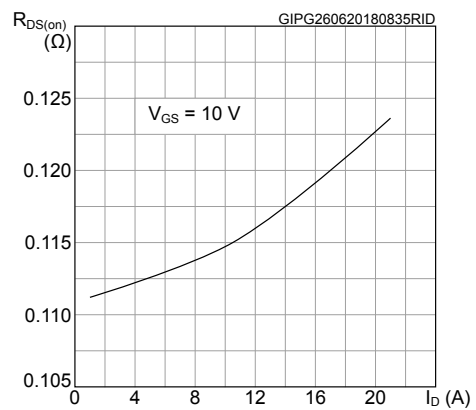
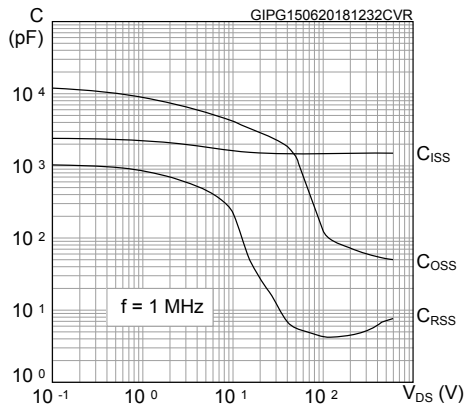
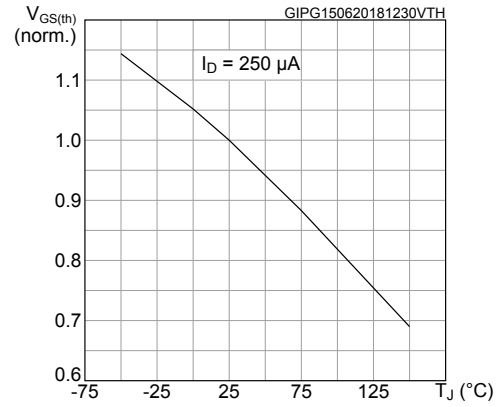
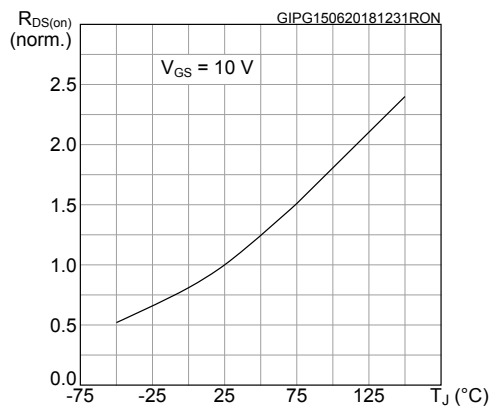
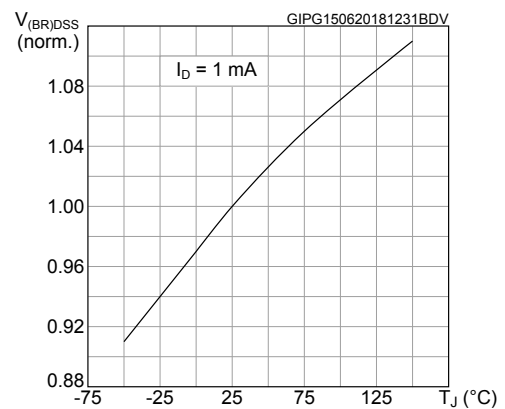
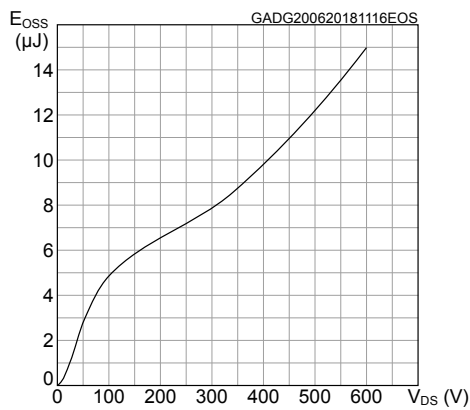
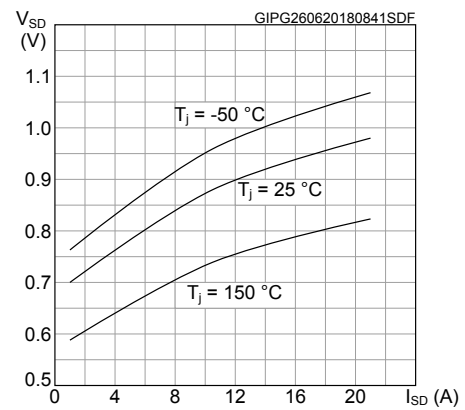
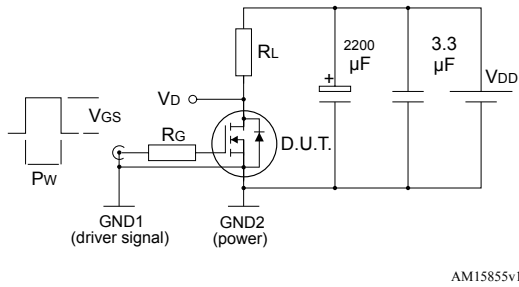
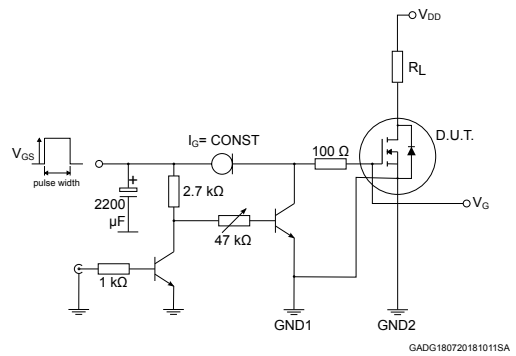
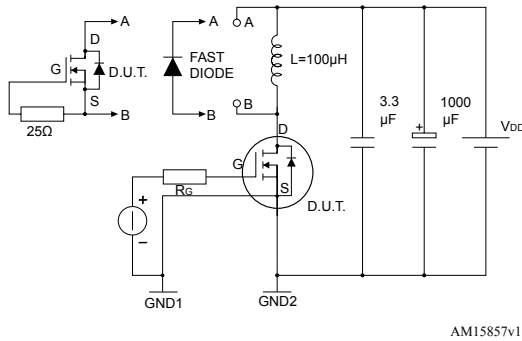
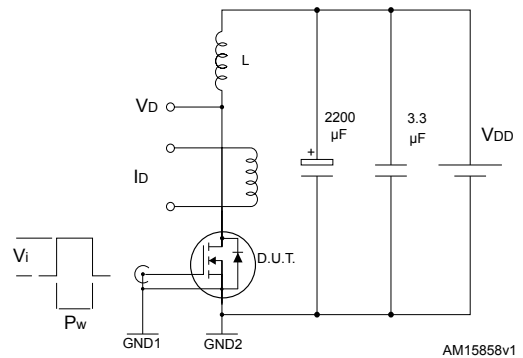
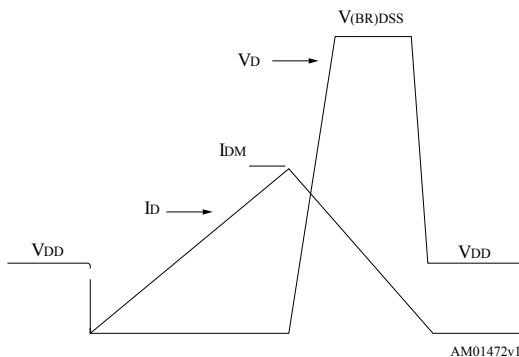
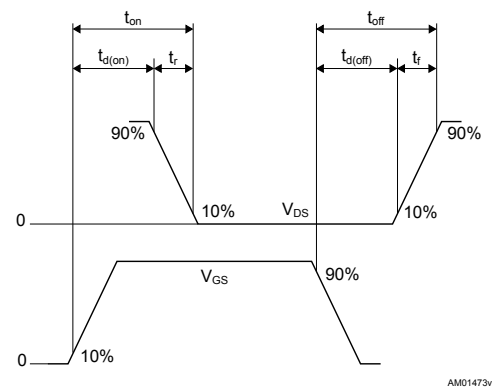


Figure 6. Static drain-source on-resistance



**Figure 7. Capacitance variations**

**Figure 8. Normalized gate threshold voltage vs temperature**

**Figure 9. Normalized on-resistance vs temperature**

**Figure 10. Normalized V\_(BR)DSS vs temperature**

**Figure 11. Output capacitance stored energy**

**Figure 12. Source-drain diode forward characteristics**


### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**

**Figure 14. Test circuit for gate charge behavior**

**Figure 15. Test circuit for inductive load switching and diode recovery times**

**Figure 16. Unclamped inductive load test circuit**

**Figure 17. Unclamped inductive waveform**

**Figure 18. Switching time waveform**


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## 4 Package information

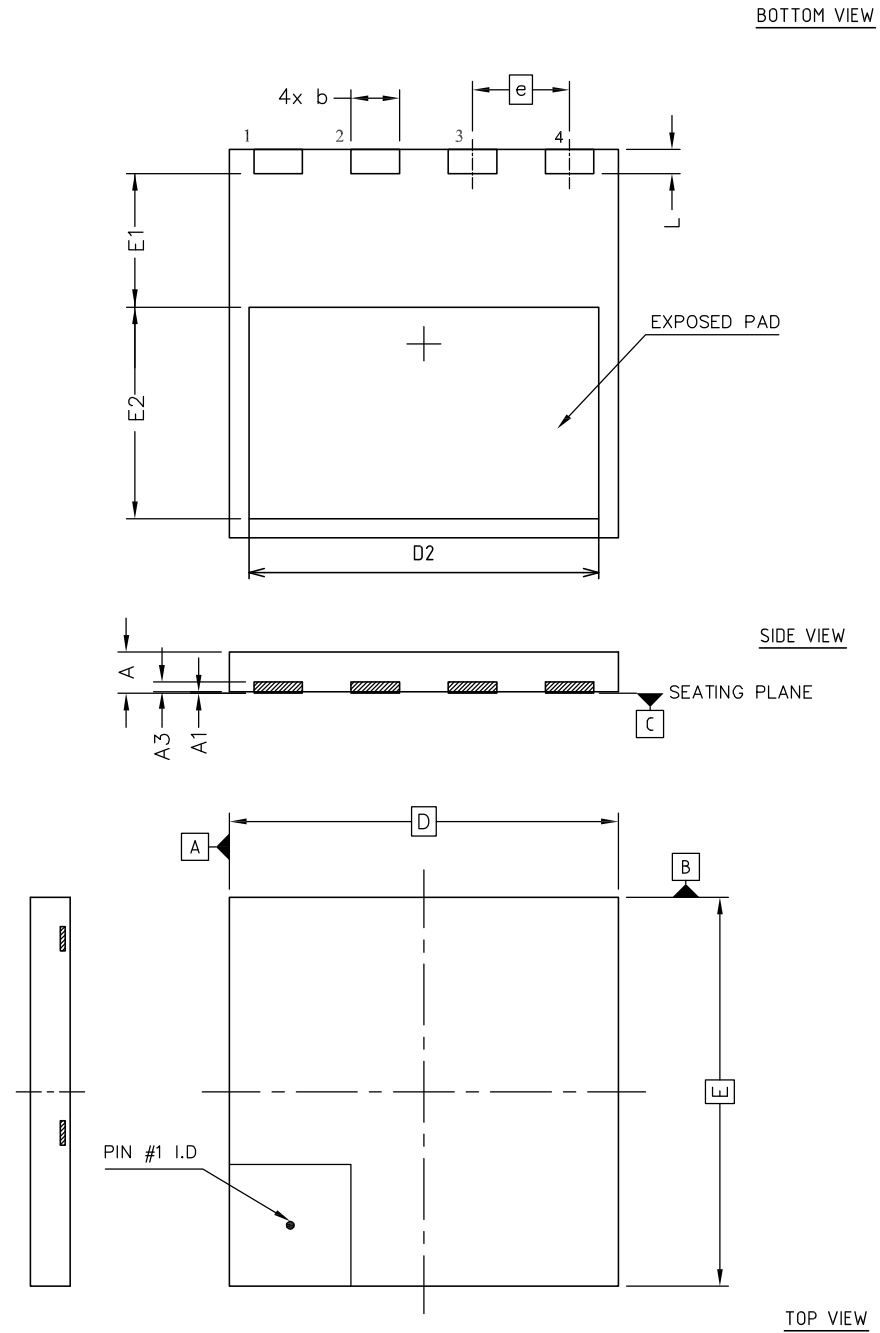
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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.



## 4.1 PowerFLAT™ 8x8 HV package information

Figure 19. PowerFLAT™ 8x8 HV package outline

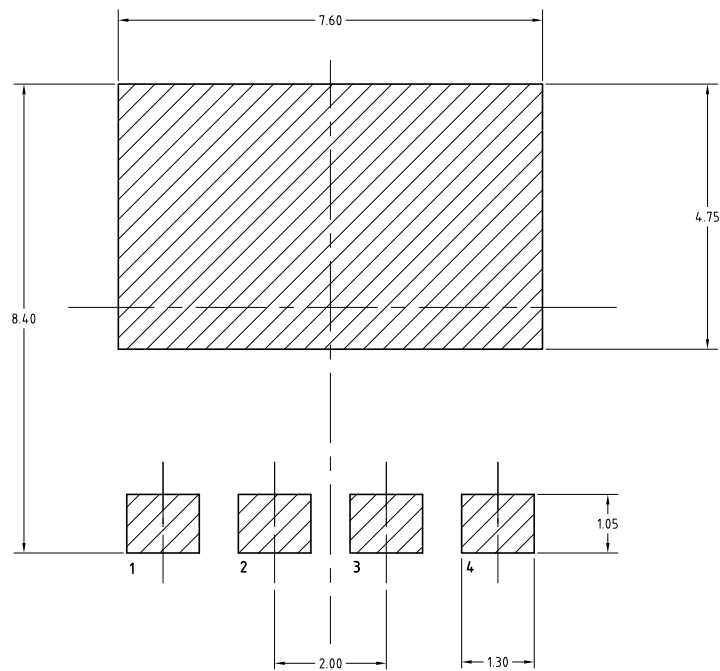


8222871\_Rev\_4

**Table 8. PowerFLAT™ 8x8 HV mechanical data**

Ref.	Dimensions (in mm)		
	Min.	Typ.	Max.
A	0.75	0.85	0.95
A1	0.00		0.05
A3	0.10	0.20	0.30
b	0.90	1.00	1.10
D	7.90	8.00	8.10
E	7.90	8.00	8.10
D2	7.10	7.20	7.30
E1	2.65	2.75	2.85
E2	4.25	4.35	4.45
e	2.00 BSC		
L	0.40	0.50	0.60

**Figure 20. PowerFLAT™ 8x8 HV footprint**

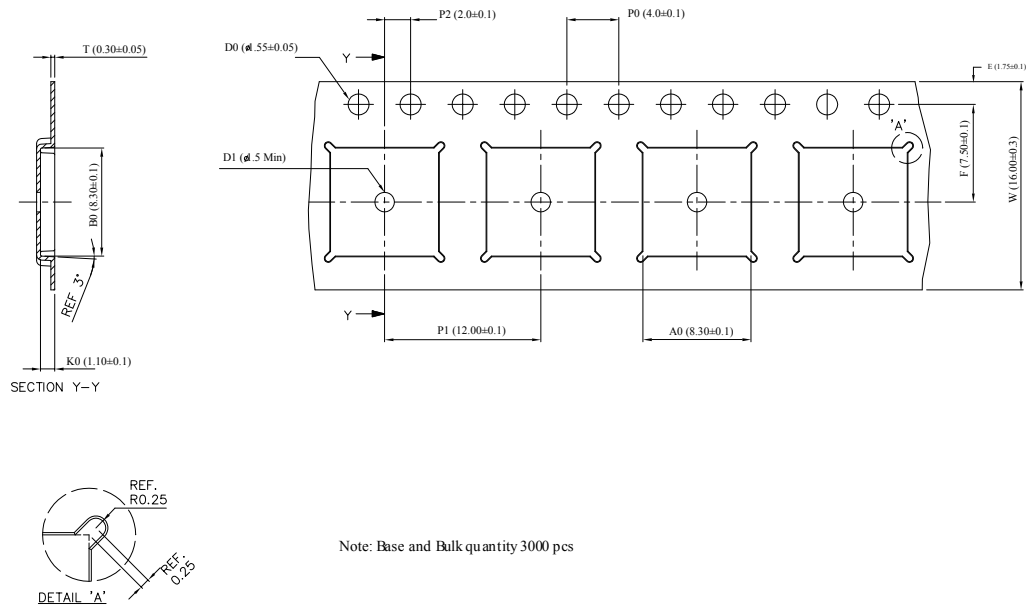


8222871\_REV\_4\_footprint

*Note: All dimensions are in millimeters.*

## 4.2 PowerFLAT™ 8x8 HV packing information

Figure 21. PowerFLAT™ 8x8 HV tape



8229819\_Tape\_revA

Note: All dimensions are in millimeters.

Figure 22. PowerFLAT™ 8x8 HV package orientation in carrier tape

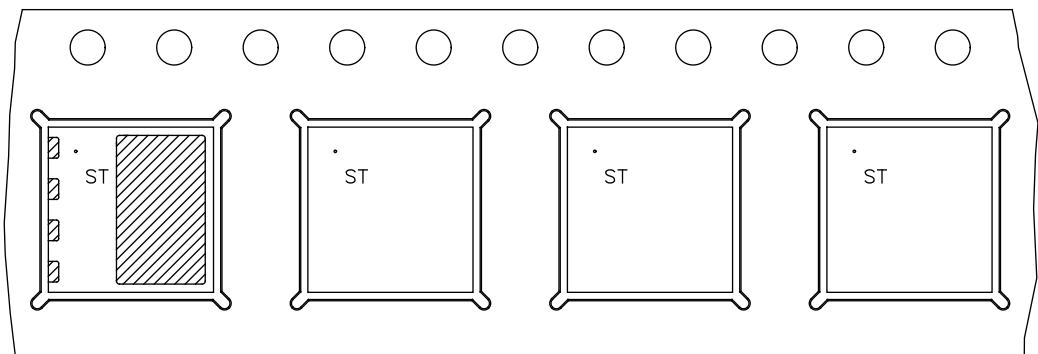
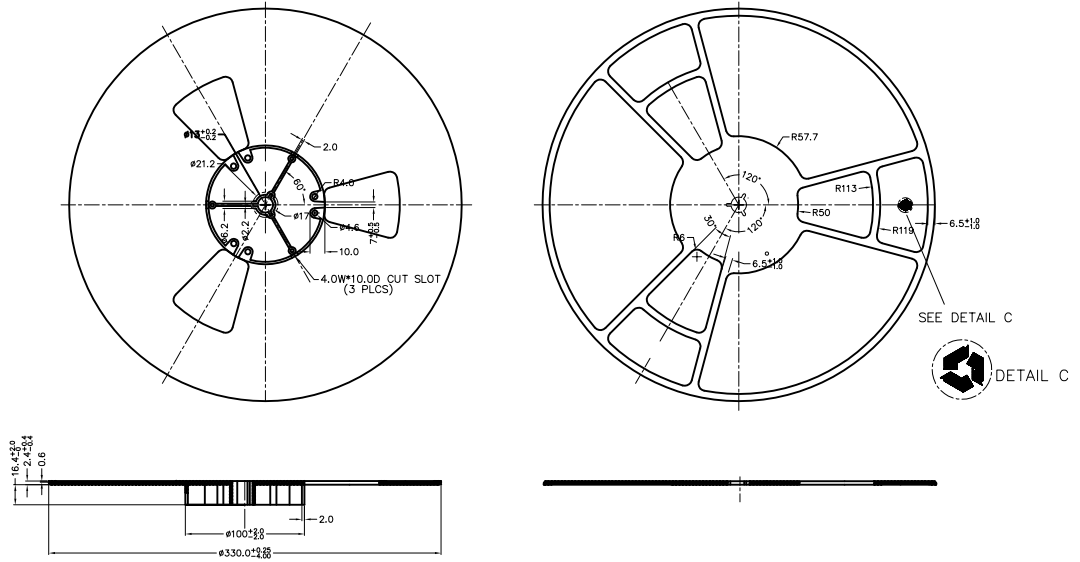


Figure 23. PowerFLAT™ 8x8 HV reel



8229819\_Reel\_revA

Note: All dimensions are in millimeters.

## Revision history

**Table 9. Document revision history**

Date	Version	Changes
02-Jul-2018	1	Initial release.
18-Jul-2018	2	Modified <a href="#">Section 3 Test circuits</a> . Minor text changes.
02-Aug-2018	3	Updated features in cover page.

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