![FAIRCHILD SEMICONDUCTOR®]

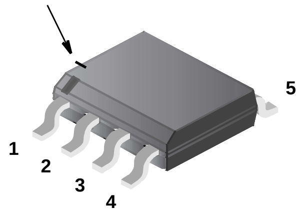
HUF75631SK8

Data Sheet **December 2001**

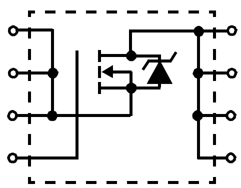
5.5A, 100V, 0.039 Ohm, N-Channel, UltraFET® Power MOSFET

Packaging

JEDEC MS-012AA



Symbol



Features

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.039\Omega$, $V_{GS} = 10V$
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75631SK8	MS-012AA	75631SK8

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF75631SK8T.

Absolute Maximum Ratings $T_A = 25^oC$, Unless Otherwise Specified

	HUF75631SK8	UNITS
Drain to Source Voltage (Note 1) . . . . . V_{DSS}	100	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1) . . . . . V_{DGR}	100	V
Gate to Source Voltage . . . . . V_{GS}	±20	V
Drain Current		
Continuous ($T_A = 25^oC$, $V_{GS} = 10V$) (Figure 2) . . . . . I_D	5.5	A
Continuous ($T_A = 100^oC$, $V_{GS} = 10V$) (Figure 2) . . . . . I_D	3.5	A
Pulsed Drain Current . . . . . I_{DM}	Figure 4	
Pulsed Avalanche Rating . . . . . UIS	Figures 6, 14, 15	
Power Dissipation . . . . . P_D	2.5	W
Derate Above 25^oC	20	$mW/^oC$
Operating and Storage Temperature . . . . . T_J, T_{STG}	-55 to 150	^oC
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . . T_L	300	^oC
Package Body for 10s, See Techbrief TB334 . . . . . T_{pkg}	260	^oC

NOTES:

1. $T_J = 25^oC$ to 150^oC.
2. $50^oC/W$ measured using FR-4 board with 0.76 in^2 (490.3 mm^2) copper pad at 10 second.
3. $152^oC/W$ measured using FR-4 board with 0.054 in^2 (34.8 mm^2) copper pad at 1000 seconds
4. $189^oC/W$ measured using FR-4 board with 0.0115 in^2 (7.42 mm^2) copper pad at 1000 seconds

CAUTION: *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html
For severe environments, see our Automotive HUFA series.
All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

Electrical Specifications $T_A = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$ (Figure 11)		100	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 95V$, $V_{GS} = 0V$		-	-	1	µA
		$V_{DS} = 90V$, $V_{GS} = 0V$, $T_A = 150^oC$		-	-	250	µA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$ (Figure 10)		2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 5.5A$, $V_{GS} = 10V$ (Figure 9)		-	0.033	0.039	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = 0.76 in^2 (490.3 mm^2) (Note 2) (Figures 20, 21)		-	-	50	$^oC/W$
		Pad Area = 0.054 in^2 (34.8 mm^2) (Note 3) (Figures 20, 21)		-	-	152	$^oC/W$
		Pad Area = 0.0115 in^2 (7.42 mm^2)(Note 4) (Figures 20, 21)		-	-	189	$^oC/W$
SWITCHING SPECIFICATIONS							
Turn-On Time	t_{ON}	$V_{DD} = 50V$, $I_D = 5.5A$ $V_{GS} = 10V$, $R_{GS} = 6.8\Omega$ (Figures 18, 19)		-	-	50	ns
Turn-On Delay Time	$t_{d(ON)}$			-	11	-	ns
Rise Time	t_r			-	23	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	39	-	ns
Fall Time	t_f			-	31	-	ns
Turn-Off Time	t_{OFF}			-	-	105	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to 20V	$V_{DD} = 50V$, $I_D = 5.5A$, $I_{g(REF)} = 1.0mA$ (Figures 13, 16, 17)	-	66	79	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0V$ to 10V		-	35	43	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to 2V		-	2.4	2.9	nC
Gate to Source Gate Charge	Q_{gs}			-	4.75	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	12	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz (Figure 12)		-	1225	-	pF
Output Capacitance	C_{OSS}			-	330	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	105	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 5.5$ A	-	-	1.25	V
		$I_{SD} = 2.5$ A	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 5.5$ A, $dI_{SD}/dt = 100A/\mu s$	-	-	96	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 5.5$ A, $dI_{SD}/dt = 100A/\mu s$	-	-	310	nC

Typical Performance Curves

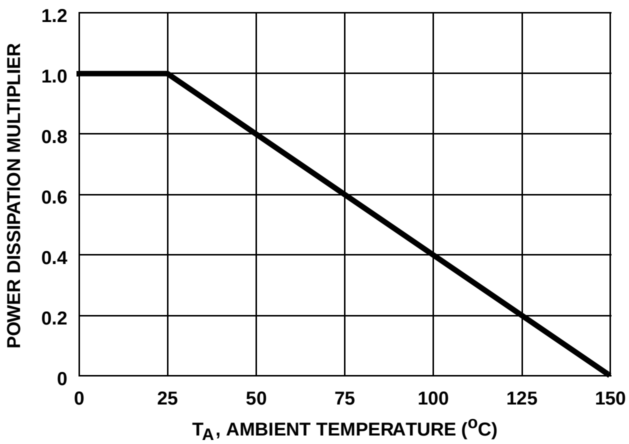


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

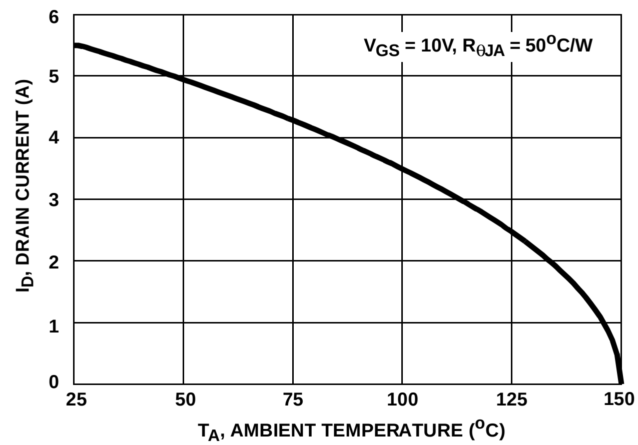


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

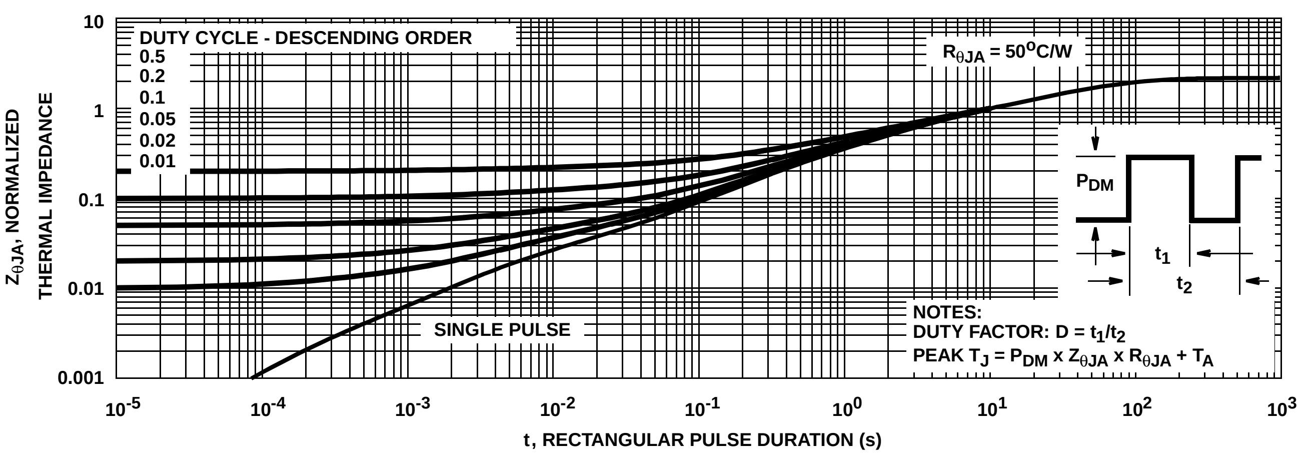


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

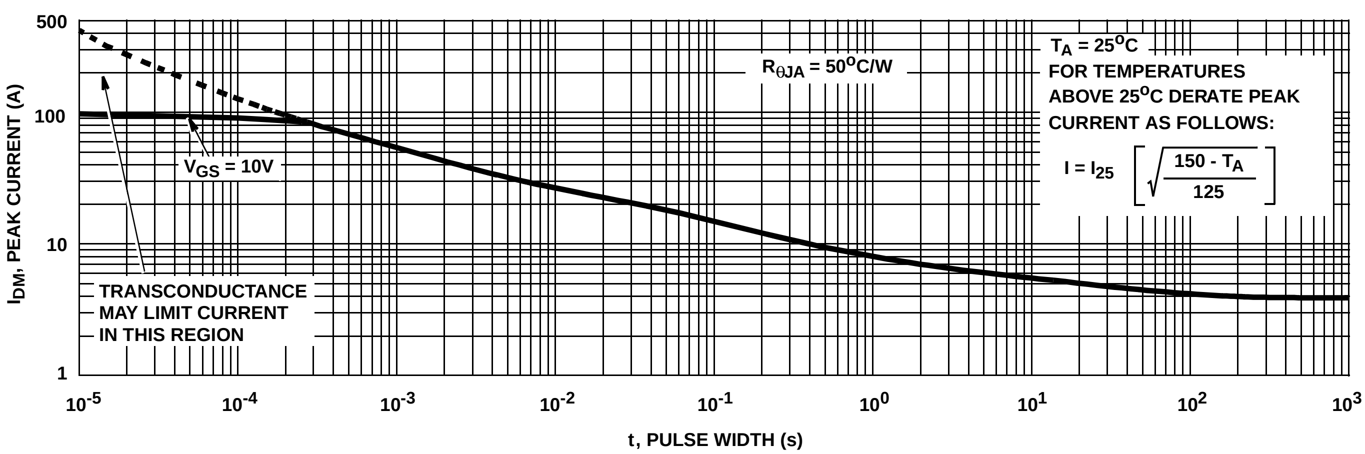


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

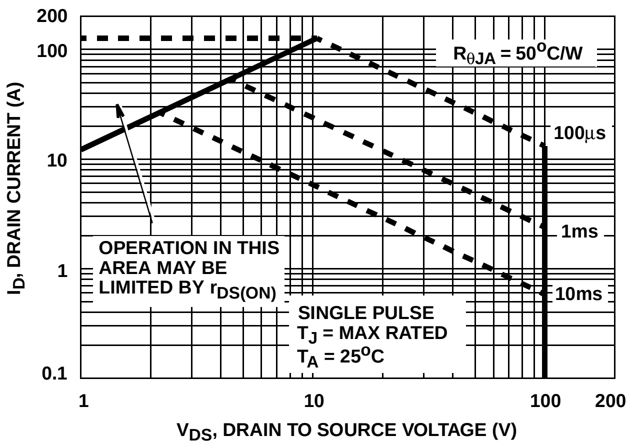
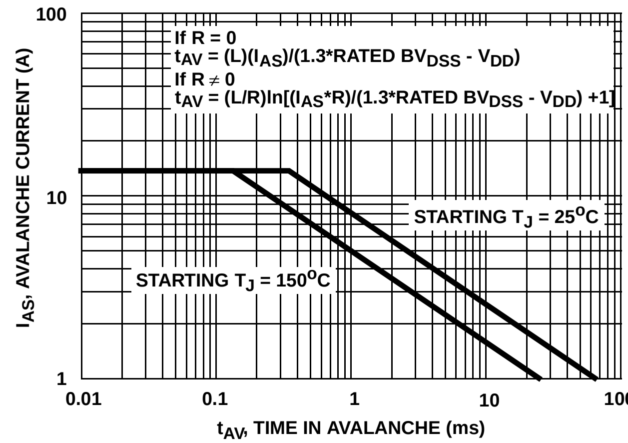


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

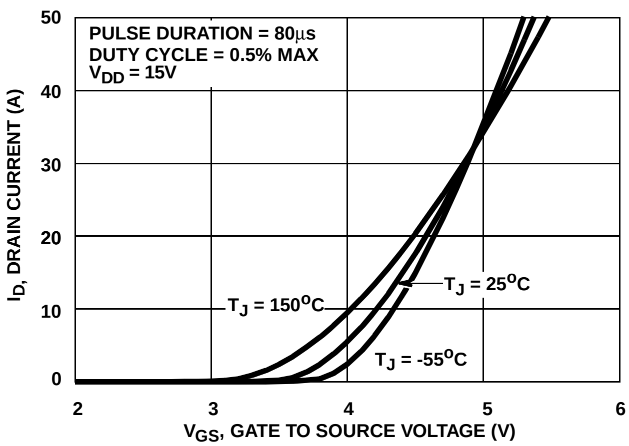


FIGURE 7. TRANSFER CHARACTERISTICS

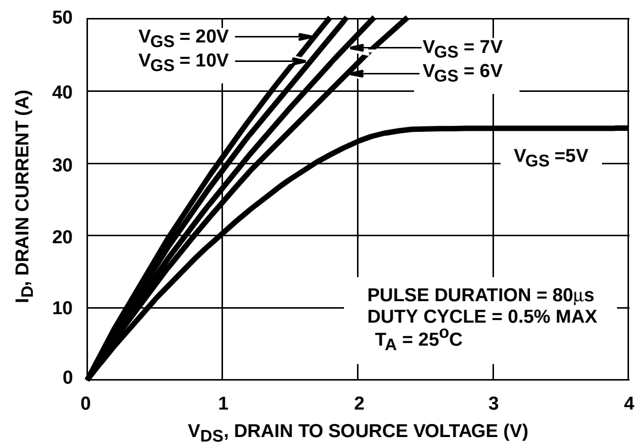


FIGURE 8. SATURATION CHARACTERISTICS

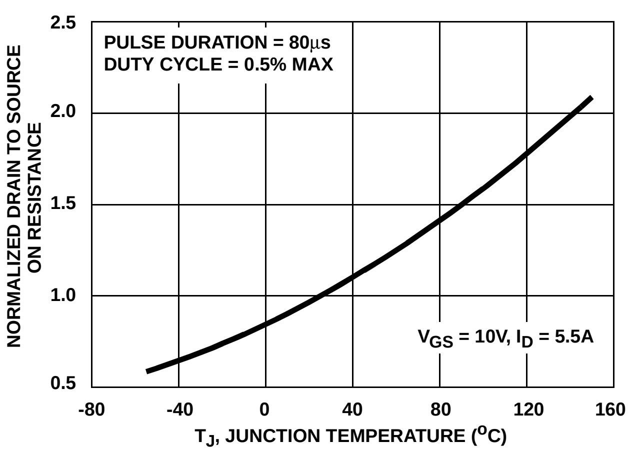


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

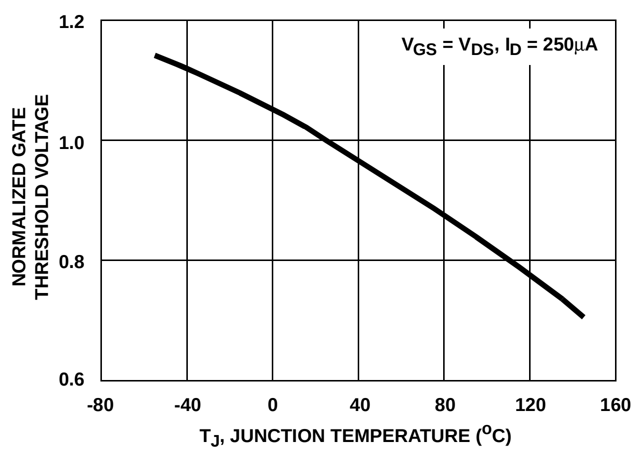


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

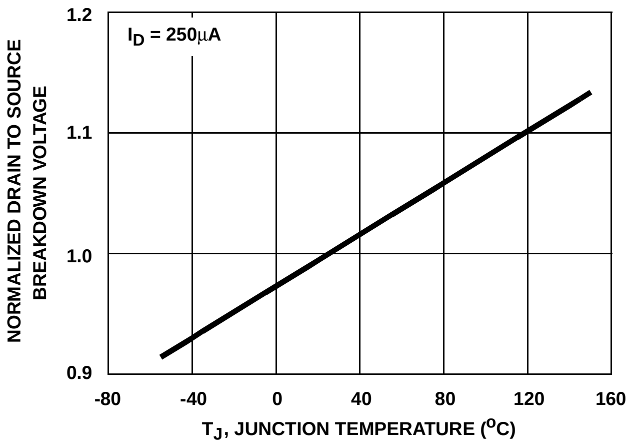


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

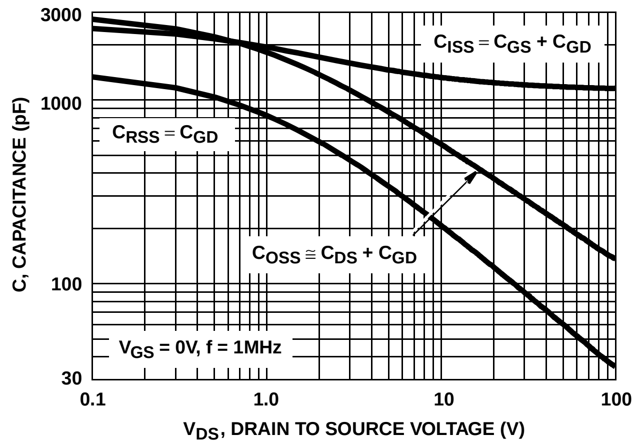
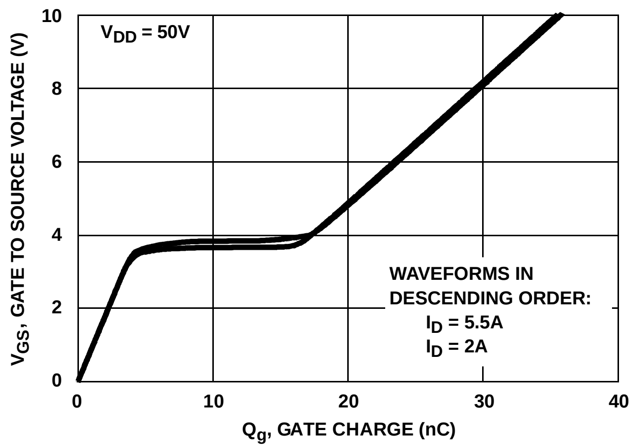


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

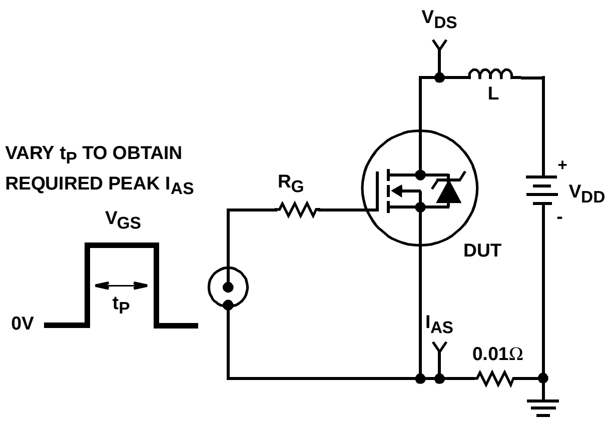


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

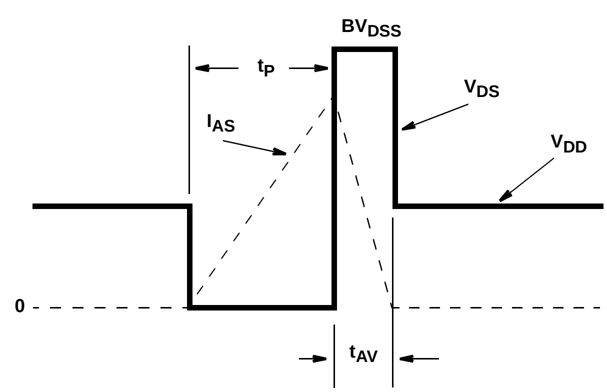


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

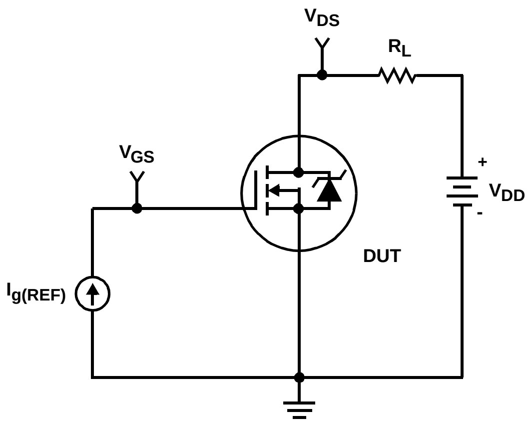


FIGURE 16. GATE CHARGE TEST CIRCUIT

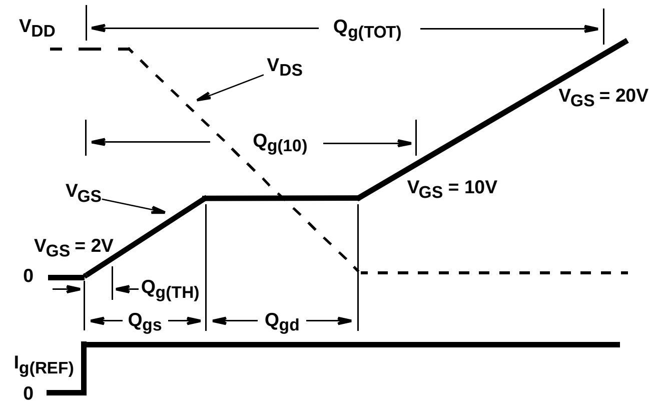


FIGURE 17. GATE CHARGE WAVEFORMS

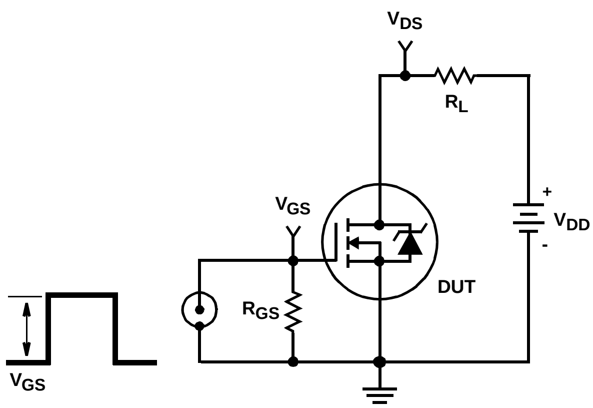


FIGURE 18. SWITCHING TIME TEST CIRCUIT

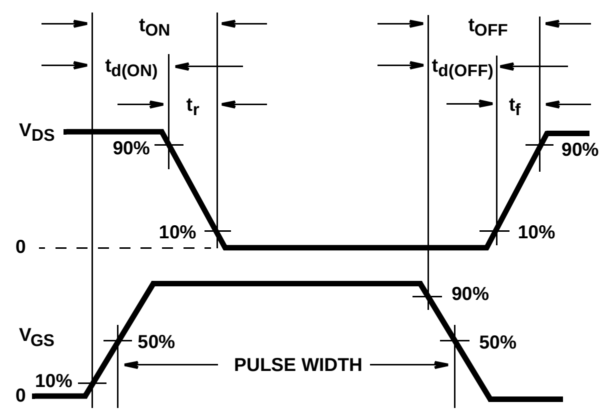


FIGURE 19. SWITCHING TIME WAVEFORM

Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature, T_{JM}, and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation, P_{DM}, in an application. Therefore the application's ambient temperature, T_A (^oC), and thermal resistance $R_{\theta JA}$ ($^oC/W$) must be reviewed to ensure that T_{JM} is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{Z_{\theta JA}} \qquad \text{(EQ. 1)}$$

In using surface mount devices such as the SOP-8 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of P_{DM} is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 20 defines the $R_{\theta JA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Displayed on the curve are $R_{\theta JA}$ values listed in the Electrical Specifications table. The points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation, P_{DM}.

Thermal resistances corresponding to other copper areas can be obtained from Figure 23 or by calculation using Equation 2. $R_{\theta JA}$ is defined as the natural log of the area times a coefficient added to a constant. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 83.2 - 23.6 \times \ln(\text{Area}) \qquad \text{(EQ. 2)}$$

The transient thermal impedance ($Z_{\theta JA}$) is also effected by varied top copper board area. Figure 21 shows the effect of copper pad area on single pulse transient thermal impedance. Each trace represents a copper pad area in square inches corresponding to the descending list in the graph. Spice and SABER thermal models are provided for each of the listed pad areas.

Copper pad area has no perceivable effect on transient thermal impedance for pulse widths less than 100ms. For pulse widths less than 100ms the transient thermal impedance is determined by the die and package. Therefore, CTHERM1 through CTHERM5 and RTHERM1 through RTHERM5 remain constant for each of the thermal models. A listing of the model component values is available in Table 1.

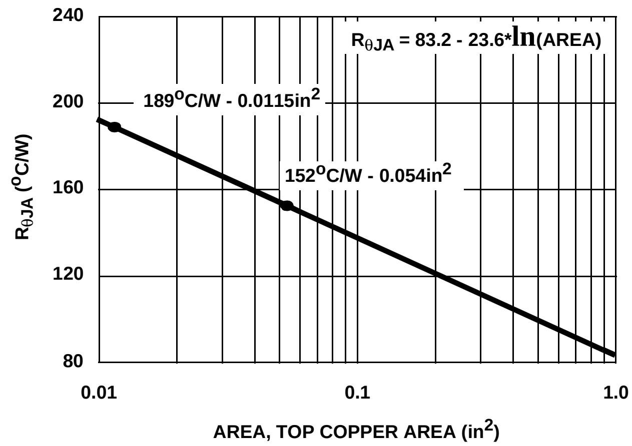


FIGURE 20. THERMAL RESISTANCE vs MOUNTING PAD AREA

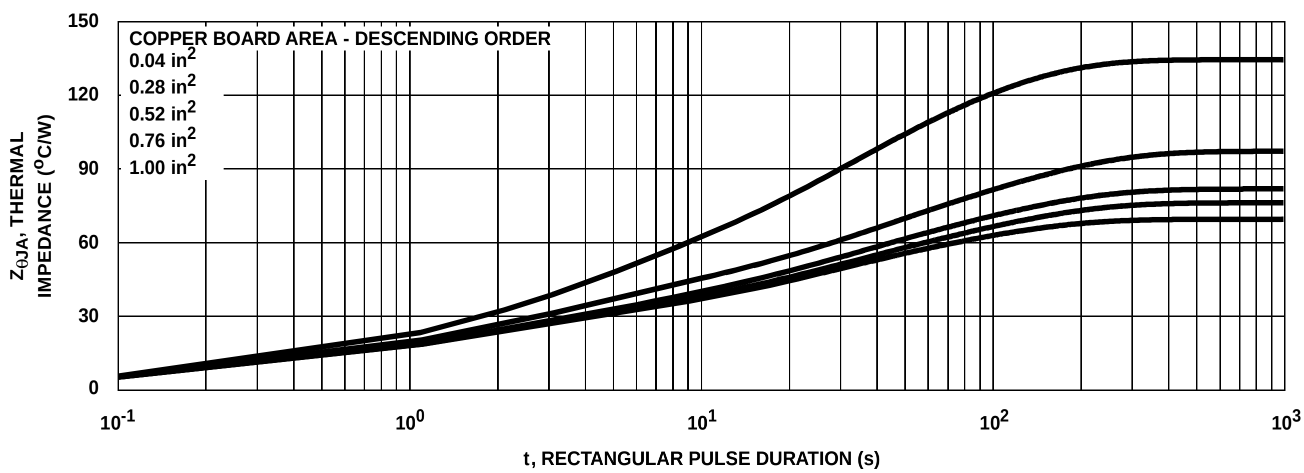
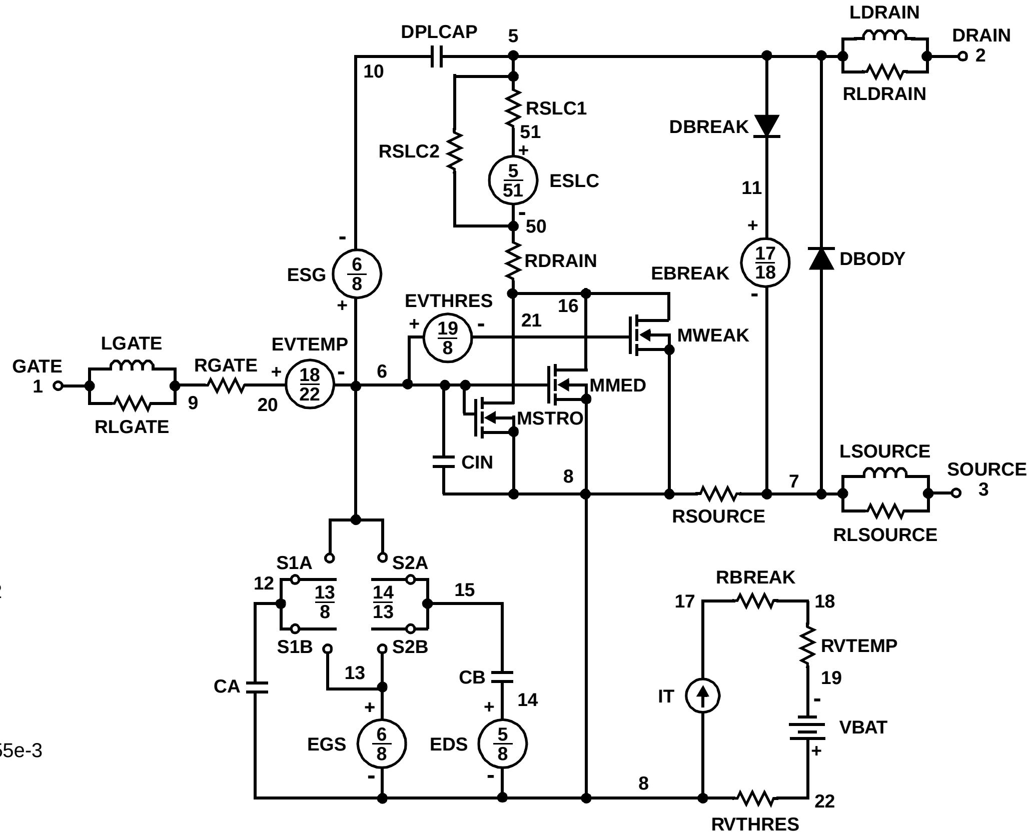


FIGURE 21. THERMAL IMPEDANCE vs MOUNTING PAD AREA

PSPICE Electrical Model

.SUBCKT HUF75631SK8 2 1 3 ;   rev 29 July 1999

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CA  12  8 1.88e-9
CB  15  14 1.88e-9
CIN  6  8 1.12e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11  DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17  18 114.8
EDS  14  8  5  8 1
EGS  13  8  6  8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8  1
EVTEMP 20 6 18 22 1

IT  8  17  1

LDRAIN 2 5 1.0e-9
LGATE 1  9 1.12e-9
LSOURCE  3  7 1.29e-10

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK  17  18  RBREAKMOD  1
RDRAIN 50 16 RDRAINMOD 1.86e-2
RGATE  9  20 1.88
RLDRAIN 2 5 10
RLGATE 1 9 11.2
RLSOURCE 3 7 1.29
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE  8  7  RSOURCEMOD 7.55e-3
RVTHRES 22 8 RVTHRESMOD  1
RVTEMP 18 19 RVTEMPMOD 1

S1A  6  12  13  8  S1AMOD
S1B  13  12  13  8  S1BMOD
S2A  6  15  14  13  S2AMOD
S2B  13  15  14  13  S2BMOD

VBAT 22 19  DC  1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*76),2))}

.MODEL DBODYMOD D (IS = 1.02e-12 RS = 5.39e-3  TRS1 = 1.01e-3  TRS2 = 9.97e-7  CJO = 1.49e-9  TT = 9.98e-8 M = 0.58)
.MODEL DBREAKMOD D (RS = 3.03e-  1TRS1 = 2.37e-  3TRS2 = 0)
.MODEL DPLCAPMOD D (CJO = 1.44e-  9IS = 1e-3  0M = 0.80)
.MODEL MMEDMOD NMOS (VTO = 3.04 KP = 1.75 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.88)
.MODEL MSTROMOD NMOS (VTO = 3.47 KP = 40 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.71 KP = 0.08 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 18.8 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.09e-  3TC2 = 0)
.MODEL RDRAINMOD RES (TC1 = 9.09e-3  TC2 = 2.74e-5)
.MODEL RSLCMOD RES (TC1 = 5.00e-3 TC2 = 0)
.MODEL RSOURCEMOD RES (TC1 = 1.00e-3 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.66e-3 TC2 = -1.01e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.38e-  3TC2 = 1.39e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -5.5  VOFF= -4.0)
.MODEL S1BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -4.0  VOFF= -5.5)
.MODEL S2AMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = -1.0  VOFF= 0.0)
.MODEL S2BMOD VSWITCH (RON = 1e-5  ROFF = 0.1  VON = 0.0  VOFF= -1.0)

.ENDS
```

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 29 July 1999

```
template huf75631sk8 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod =  (is = 1.02e-12, cjo = 1.49e-9, tt = 9.98e-8, m = 0.58)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 1.44e-9, is = 1e-30, m = 0.80 )
m..model mmedmod = (type=_n, vto = 3.04, kp = 1.75, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.47, kp = 40, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 2.71, kp = 0.08, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -5.5, voff = -4)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -4, voff = -5.5)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -1, voff = 0)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0, voff = -1)

c.ca n12 n8 = 1.88e-9
c.cb n15 n14 = 1.88e-9
c.cin n6 n8 = 1.12e-9

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 1.12e-9
l.lsource n3 n7 = 1.29e-10

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

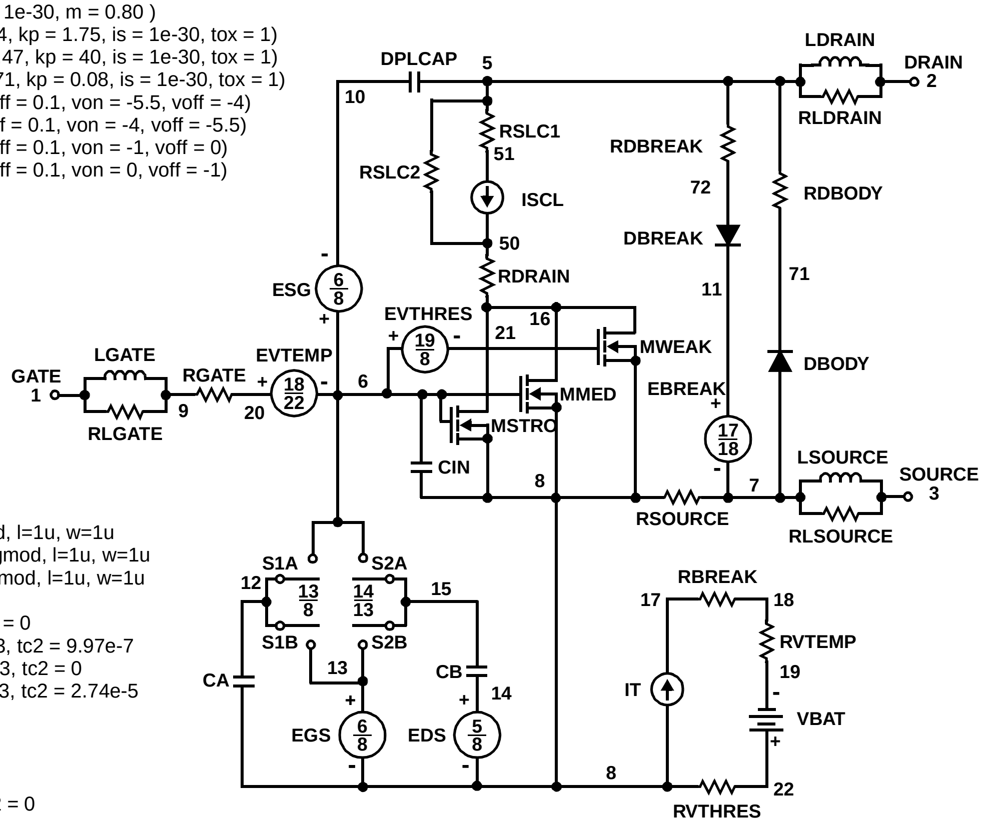
res.rbreak n17 n18  = 1, tc1 = 1.09e-3, tc2 = 0
res.rdbody n71 n5 = 5.39e-3, tc1 = 1.01e-3, tc2 = 9.97e-7
res.rdbreak n72 n5 = 3.03e-1, tc1 = 2.37e-3, tc2 = 0
res.rdrain n50 n16  = 1.86e-2, tc1 = 9.09e-3, tc2 = 2.74e-5
res.rgate n9 n20 = 1.88
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 11.2
res.rlsource n3 n7 = 1.29
res.rslc1 n5 n51  = 1e-6, tc1 = 5.00e-3, tc2 = 0
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 7.55e-3, tc1 = 1.00e-3, tc2 = 0
res.rvtemp n18 n19  = 1, tc1 = -2.38e-3, tc2 = 1.39e-6
res.rvthres n22 n8  = 1, tc1 = -2.66e-3, tc2 = -1.01e-5

spe.ebreak n11 n7 n17 n18 = 114.8
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/76))** 2))
}
}
```



SPICE Thermal Model

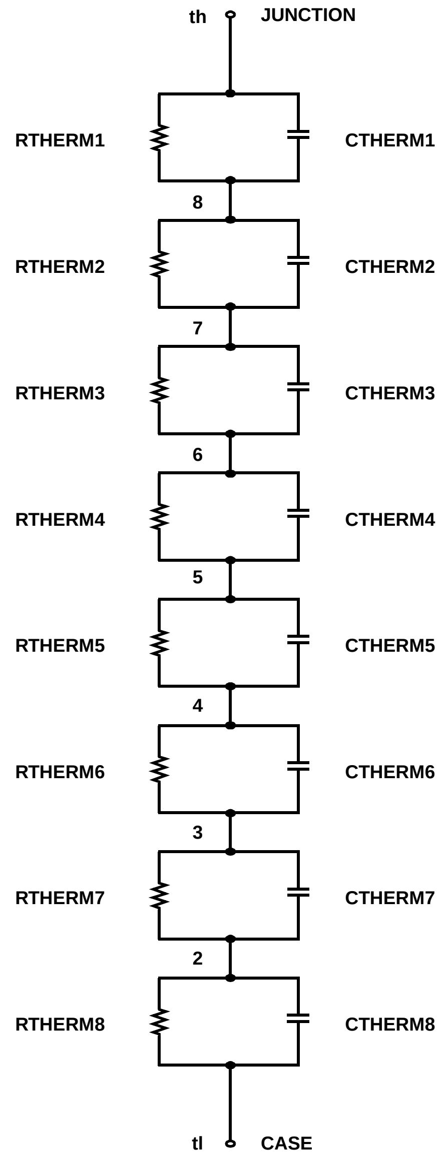
REV 28 July 1999
HUF75631SK8
Copper Area = 0.04 in^2
CTHERM1 th 8 2.0e-3
CTHERM2 8 7 5.0e-3
CTHERM3 7 6 1.0e-2
CTHERM4 6 5 4.0e-2
CTHERM5 5 4 9.0e-2
CTHERM6 4 3 1.2e-1
CTHERM7 3 2 0.5
CTHERM8 2 tl 1.3

RTHERM1 th 8 0.1
RTHERM2 8 7 0.5
RTHERM3 7 6 1.0
RTHERM4 6 5 5.0
RTHERM5 5 4 8.0
RTHERM6 4 3 26
RTHERM7 3 2 39
RTHERM8 2 tl 55

SABER Thermal Model

Copper Area = 0.04 in^2
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 8 = 2.0e-3
ctherm.ctherm2 8 7 = 5.0e-3
ctherm.ctherm3 7 6 = 1.0e-2
ctherm.ctherm4 6 5 = 4.0e-2
ctherm.ctherm5 5 4 = 9.0e-2
ctherm.ctherm6 4 3 = 1.2e-1
ctherm.ctherm7 3 2 = 0.5
ctherm.ctherm8 2 tl = 1.3

rtherm.rtherm1 th 8 = 0.1
rtherm.rtherm2 8 7 = 0.5
rtherm.rtherm3 7 6 = 1.0
rtherm.rtherm4 6 5 = 5.0
rtherm.rtherm5 5 4 = 8.0
rtherm.rtherm6 4 3 = 26
rtherm.rtherm7 3 2 = 39



rtherm.rtherm8 2 tl = 55

TABLE 1. THERMAL MODELS

COMPONENT	0.04 in^2	0.28 in^2	0.52 in^2	0.76 in^2	1.0 in^2
CTHERM6	1.2e-1	1.5e-1	2.0e-1	2.0e-1	2.0e-1
CTHERM7	0.5	1.0	1.0	1.0	1.0
CTHERM8	1.3	2.8	3.0	3.0	3.0
RTHERM6	26	20	15	13	12
RTHERM7	39	24	21	19	18
RTHERM8	55	38.7	31.3	29.7	25

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CROSSVOLT™	GlobalOptoisolator™	POP™	SuperSOT™-3	
DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOME™	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPLANAR™	QFET™	SyncFET™	
E^2CMOS™	LittleFET™	QS™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

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Rev. H4