STI270N4F3

Automotive-grade N-channel 40 V, 2.1 mΩ typ., 120 A STripFET™ F3 Power MOSFET in an I²PAK package

Datasheet - production data

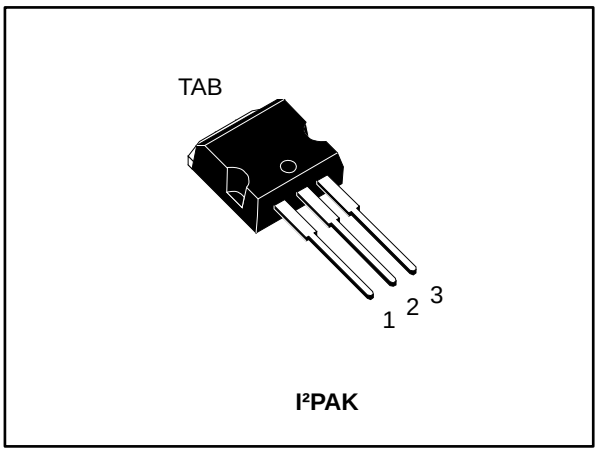
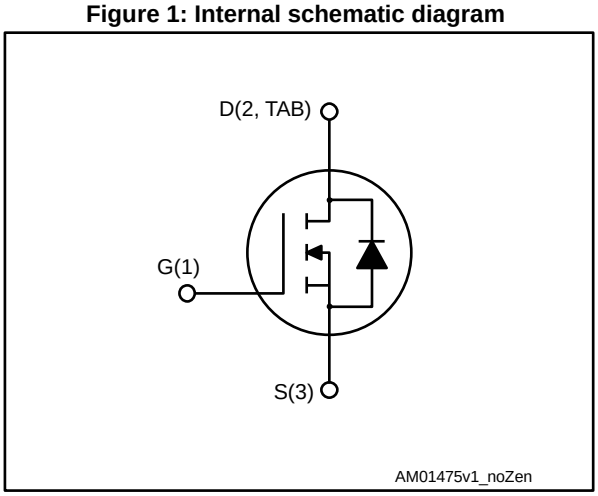


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STI270N4F3	40 V	2.6 mΩ	120 A	330 W

- AEC-Q101 qualified
- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using STripFET™ F3 technology. It is designed to minimize on-resistance and gate charge to provide superior switching performance.

Table 1: Device summary

Order code	Marking	Package	Packing
STI270N4F3	270N4F3	I²PAK	Tube

This is information on a product in full production.

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	120	A
I_D (1)	Drain current (continuous) at T_c = 100 °C	120	A
I_{DM} (2)	Drain current (pulsed)	480	A
P_{TOT}	Total dissipation at T_C = 25 °C	330	W
dv/dt (3)	Peak diode recovery voltage slope	3.5	V/ns
E_{AS} (4)	Single pulse avalanche energy	1	J
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

(1) Current limited by package.

(2) Pulse width limited by safe operating area.

(3) I_{SD} ≤ 120 A, di/dt ≤ 200 A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}

(4) Starting T_J= 25 °C, I_D= 80 A, V_{DD}= 32 V.

Table 3: Thermal resitance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	0.45	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On/Off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 40 V,			10	µA
		V_{DS} = 40 V, T_j = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±200	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 80 A		2.1	2.6	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15 V, I_D = 80 A	-	200	-	S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	7400	-	pF
C_{oss}	Output capacitance		-	1800	-	
C_{rss}	Reverse transfer capacitance		-	47	-	
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 160 A, V_{GS} = 0 to 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	110	150	nC
Q_{gs}	Gate-source charge		-	27	-	
Q_{gd}	Gate-drain charge		-	25	-	

Notes:

(1)Pulsed: pulse duration=300µs, duty cycle 1.5%.

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 80 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	22	-	ns
t_r	Rise time		-	180	-	
$t_{d(off)}$	Turn-off delay time		-	110	-	
t_f	Fall time		-	45	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		120	A
I_{SDM}(1)	Source-drain current (pulsed)		-		480	A
V_{SD}(2)	Forward on voltage	I_{DS} = 80 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 160 A, di/dt = 100 A/µs	-	70		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 32 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	225		nC
I_{RRM}	Reverse recovery current		-	3.2		A

Notes:

(1)Pulse width limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

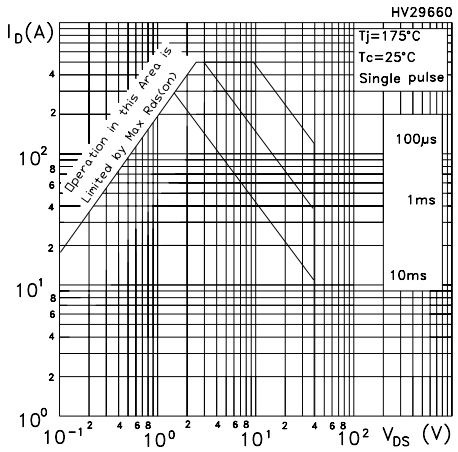


Figure 3: Thermal impedance

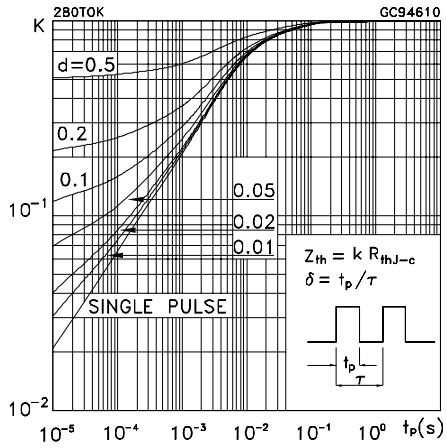


Figure 4: Output characteristics

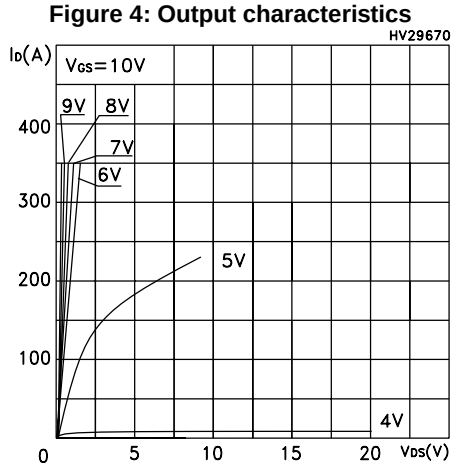


Figure 5: Transfer characteristics

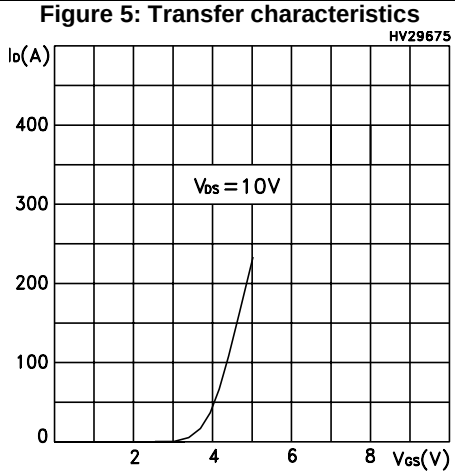


Figure 6: Normalized $V_{(BR)DSS}$ vs temperature

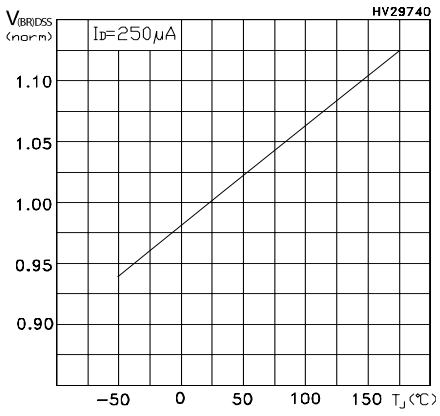


Figure 7: Static drain-source on-resistance

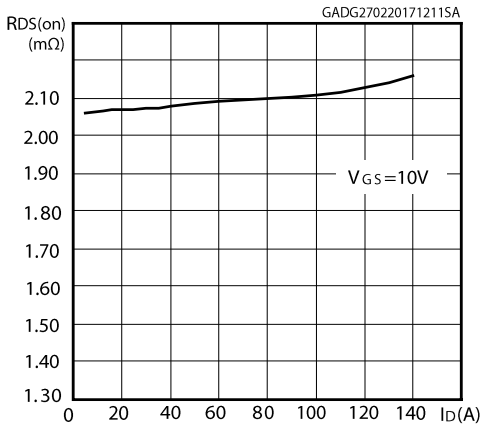


Figure 8: Gate charge vs gate-source voltage

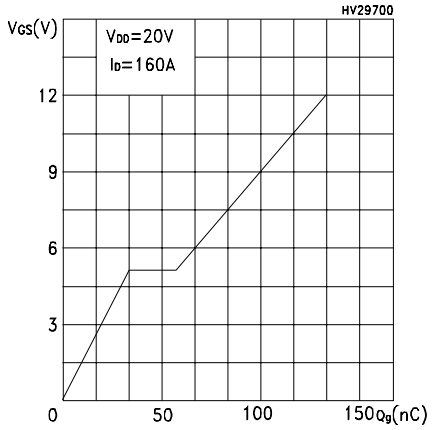


Figure 9: Capacitance variation

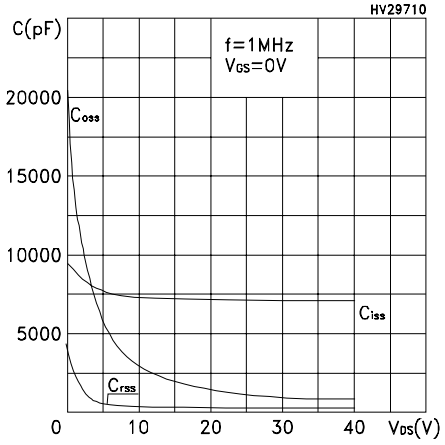


Figure 10: Normalized gate threshold voltage vs temperature

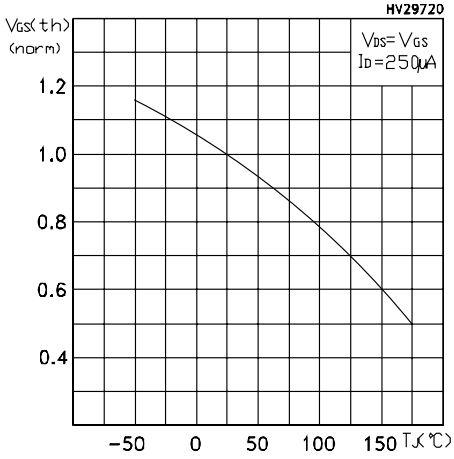


Figure 11: Normalized on-resistance vs temperature

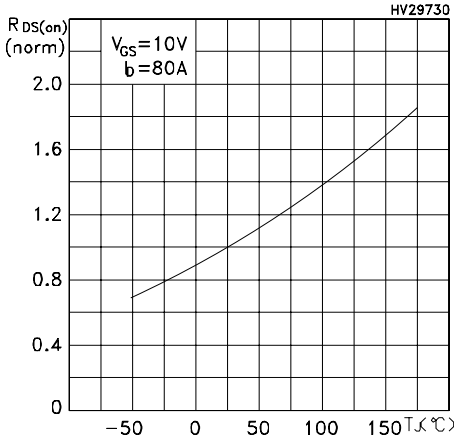
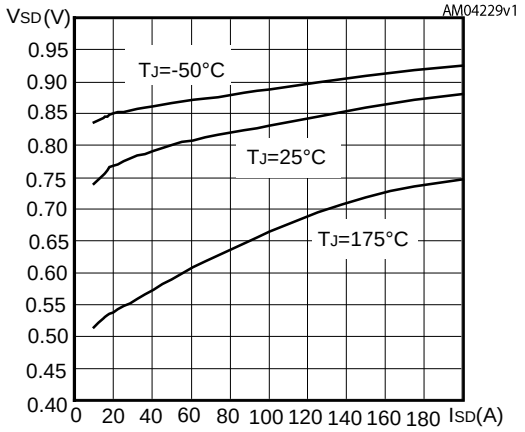


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

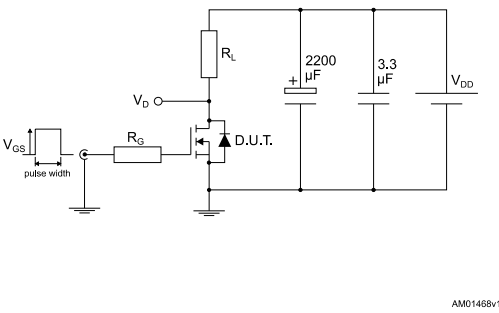


Figure 14: Test circuit for gate charge behavior

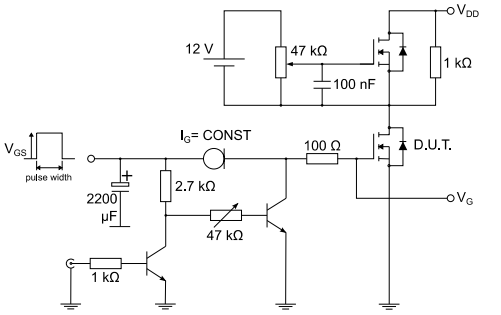


Figure 15: Test circuit for inductive load switching and diode recovery times

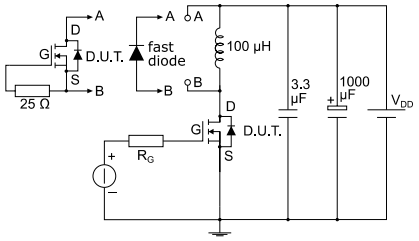


Figure 16: Unclamped inductive load test circuit

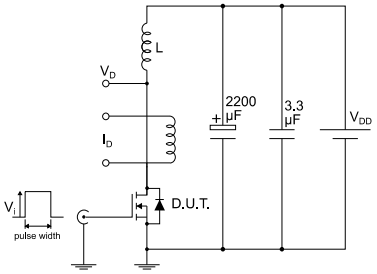


Figure 17: Unclamped inductive waveform

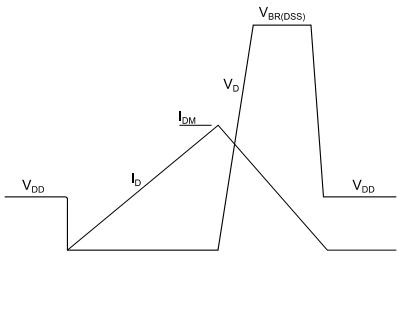
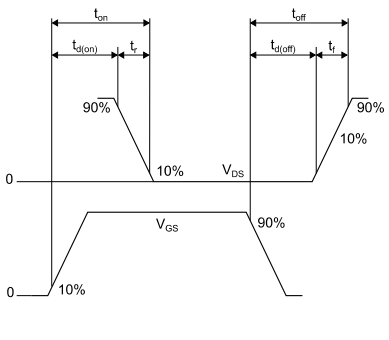


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 I²PAK package information

Figure 19: I²PAK package outline

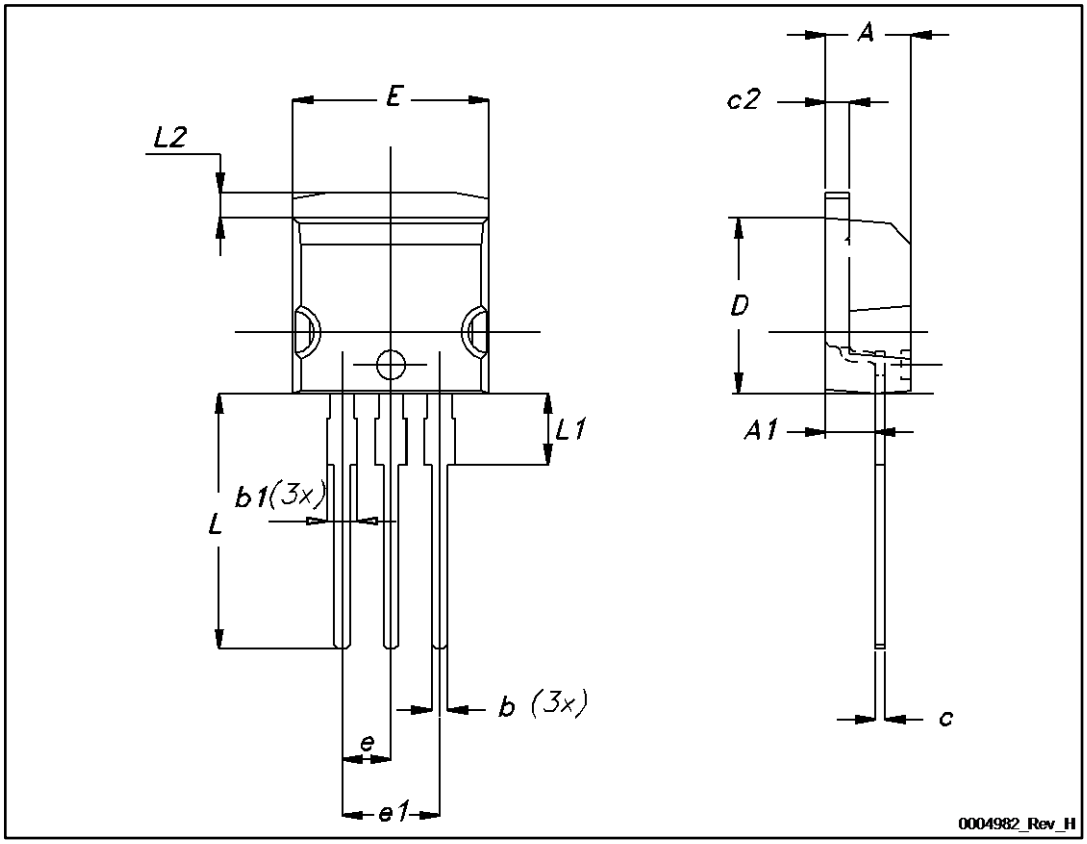


Table 8: I²PAK package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40	-	4.60
A1	2.40	-	2.72
b	0.61	-	0.88
b1	1.14	-	1.70
c	0.49	-	0.70
c2	1.23	-	1.32
D	8.95	-	9.35
e	2.40	-	2.70
e1	4.95	-	5.15
E	10	-	10.40
L	13	-	14
L1	3.50	-	3.93
L2	1.27	-	1.40

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
01-Mar-2017	1	First release.

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