# STFW45N65M5, STW45N65M5, STWA45N65M5

## N-channel 650 V, 35 A, 0.067 Ω typ., MDmesh™ V Power MOSFETs in TO-3PF, TO-247 and TO-247 long leads packages

**Datasheet - production data**

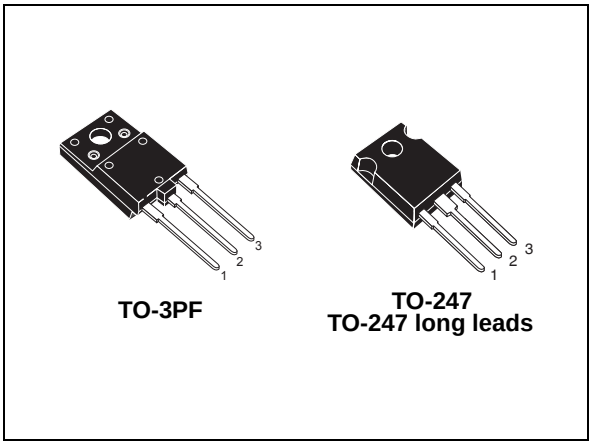
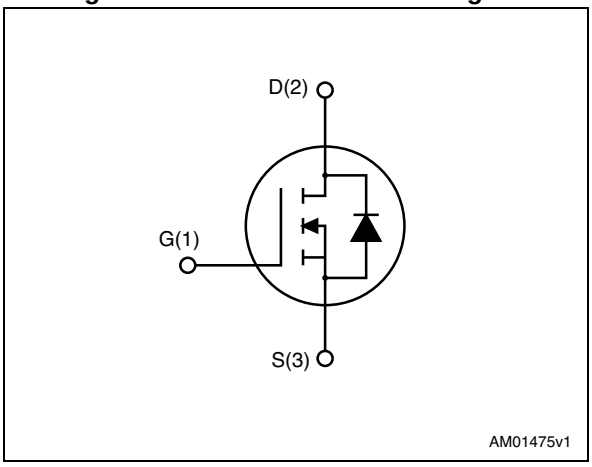



**Figure 1. Internal schematic diagram**




## Features

| Order codes | $V_{DS}$ @ $T_{Jmax}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STFW45N65M5 | 710 V | 0.078 Ω | 35 A |
| STW45N65M5 | | | |
| STWA45N65M5 | | | |

- Worldwide best $R_{DS(on)}$ * area
- Higher $V_{DSS}$ rating and high dv/dt capability
- Excellent switching performance
- 100% avalanche tested

## Applications

- Switching applications

## Description

These devices are N-channel MDmesh™ V Power MOSFETs based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Table 1. Device summary**

| Order codes | Marking | Package | Packaging |
|---|---|---|---|
| STFW45N65M5 | 45N65M5 | TO-3PF | Tube |
| STW45N65M5 | | TO-247 | |
| STWA45N65M5 | | TO-247 long leads | |

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | TO-3PF | TO-247, TO-247 long leads | |
| $V_{GS}$ | Gate-source voltage | ± 25 | | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 35 | | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100 °C | 22 | | A |
| $I_{DM}$ (1) | Drain current (pulsed) | 140 | | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 57 | 210 | W |
| dv/dt (2) | Peak diode recovery voltage slope | 15 | | V/ns |
| dv/dt (3) | MOSFET dv/dt ruggedness | 50 | | V/ns |
| $V_{ISO}$ | Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; Tc=25°C) | 3500 | | V |
| $T_{stg}$ | Storage temperature | - 55 to 150 | | °C |
| $T_j$ | Max. operating junction temperature | 150 | | °C |

1. Limited by maximum junction temperature
2. $I_{SD} \leq 35$ A, di/dt $\leq$ 400 A/µs, $V_{DS(Peak)} < V_{(BR)DSS}$, $V_{DD}$ = 400 V
3. $V_{DS} < 520$ V

**Table 3. Thermal data**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | TO-3PF | TO-247, TO-247 long leads | |
| $R_{thj\text{-}case}$ | Thermal resistance junction-case max | 2.2 | 0.6 | °C/W |
| $R_{thj\text{-}amb}$ | Thermal resistance junction-ambient max | 50 | 50 | °C/W |

**Table 4. Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$) | 9 | A |
| $E_{AS}$ | Single pulse avalanche energy (starting $t_j$=25°C, $I_d$= $I_{AR}$; $V_{dd}$=50) | 810 | mJ |

# 2 Electrical characteristics

($T_C$ = 25 °C unless otherwise specified)

**Table 5. On /off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 1 mA, $V_{GS}$ = 0 | 650 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = 650 V | | | 1 | µA |
| | | $V_{DS}$ = 650 V, $T_C$=125 °C | | | 100 | µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ± 25 V | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 17.5 A | | 0.067 | 0.078 | Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 100 V, f = 1 MHz, $V_{GS}$ = 0 | - | 3470 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 82 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 7 | - | pF |
| $C_{o(tr)}$(1) | Equivalent capacitance time related | $V_{DS}$ = 0 to 520 V, $V_{GS}$ = 0 | - | 280 | - | pF |
| $C_{o(er)}$(2) | Equivalent capacitance energy related | | - | 79 | - | pF |
| $R_G$ | Intrinsic gate resistance | f = 1 MHz open drain | - | 2 | - | Ω |
| $Q_g$ | Total gate charge | $V_{DD}$ = 520 V, $I_D$ = 17.5 A, $V_{GS}$ = 10 V (see *Figure 18*) | - | 82 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 18.5 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 35 | - | nC |

1. Time related is defined as a constant equivalent capacitance giving the same charging time as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$
2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as $C_{oss}$ when $V_{DS}$ increases from 0 to 80% $V_{DSS}$

**Table 7. Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $t_d$ (v) | Voltage delay time | $V_{DD}$ = 400 V, $I_D$ = 23 A, $R_G$ = 4.7 Ω, $V_{GS}$ = 10 V (see *Figure 19* and *Figure 22*) | - | 79.5 | - | ns |
| $t_r$ (v) | Voltage rise time | | - | 11 | - | ns |
| $t_f$ (i) | Current fall time | | - | 9.3 | - | ns |
| $t_c$(off) | Crossing time | | - | 16 | - | ns |

**Table 8. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 35 | A |
| $I_{SDM}$ (1) | Source-drain current (pulsed) | | - | | 140 | A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 35 A, $V_{GS}$ = 0 | - | | 1.5 | V |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 35 A, di/dt = 100 A/µs $V_{DD}$ = 100 V (see *Figure 19*) | - | 392 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 7.4 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 38 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 35 A, di/dt = 100 A/µs $V_{DD}$ = 100 V, $T_j$ = 150 °C (see *Figure 19*) | - | 468 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 9.7 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 42 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 2. Safe operating area for TO-3PF**

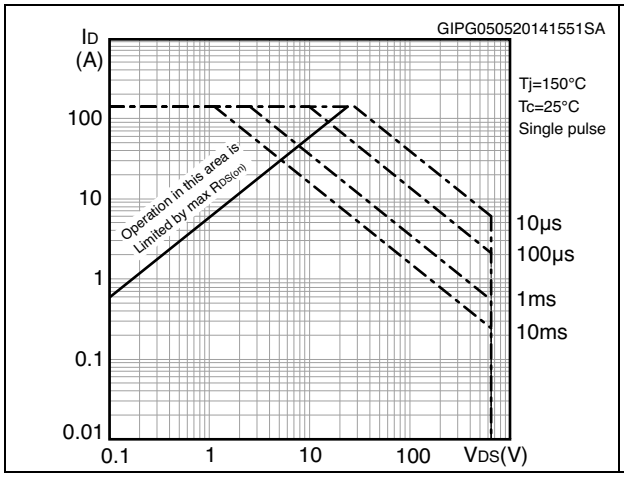



**Figure 3. Thermal impedance for TO-3PF**

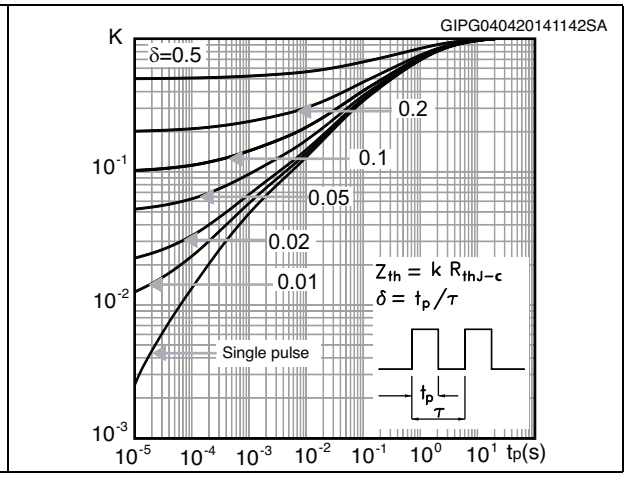



**Figure 4. Safe operating area for TO-247 and TO-247LL**

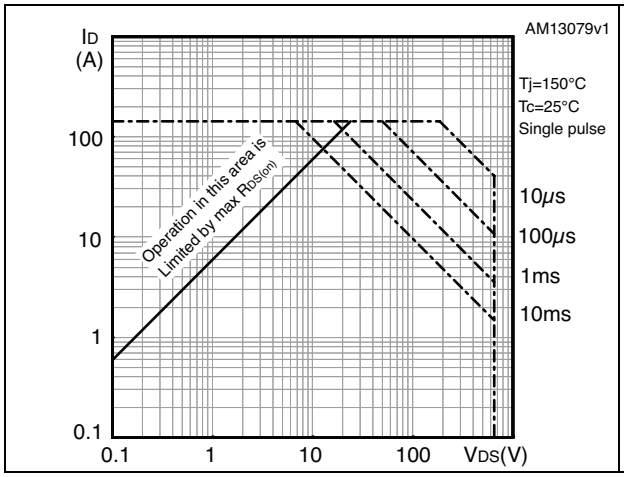



**Figure 5. Thermal impedance for TO-247 and TO-247LL**

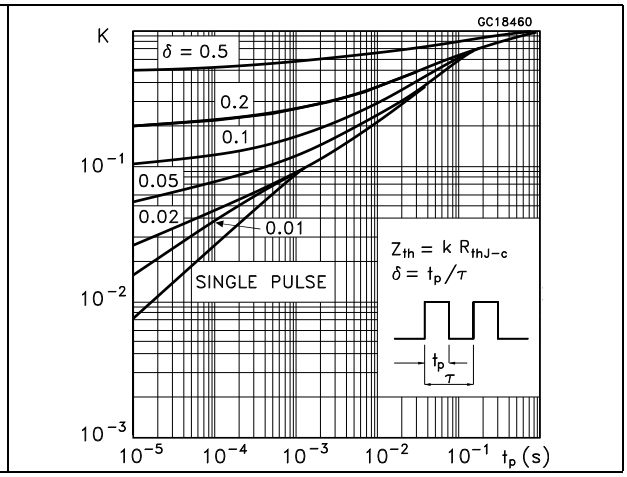



**Figure 6. Output characteristics**

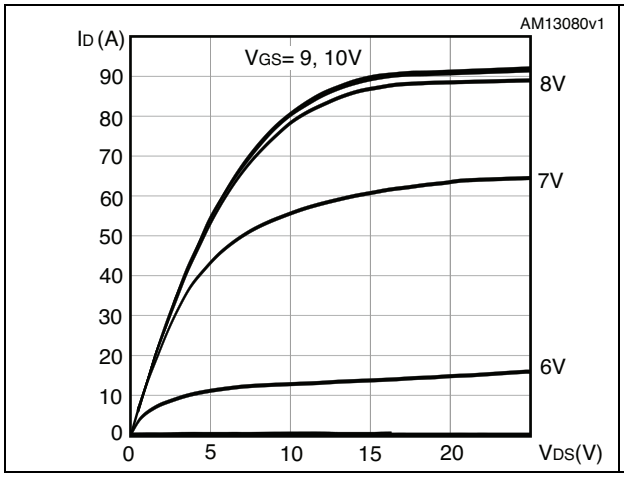



**Figure 7. Transfer characteristics**

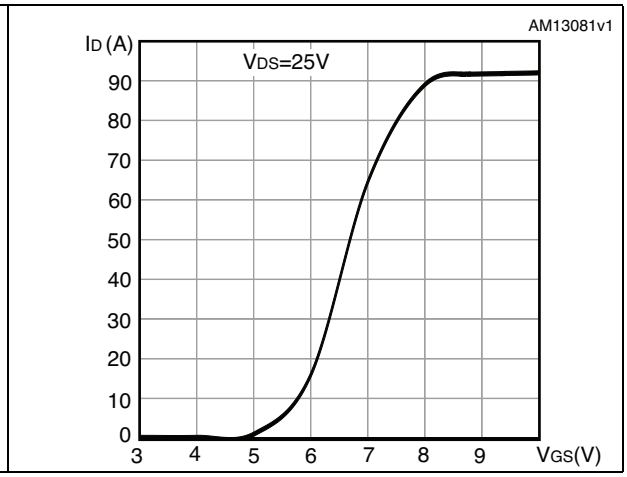


**Figure 8. Gate charge vs gate-source voltage**

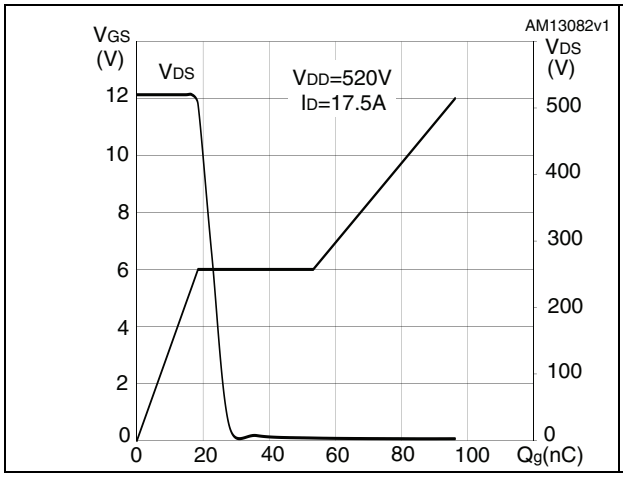



**Figure 9. Static drain-source on-resistance**

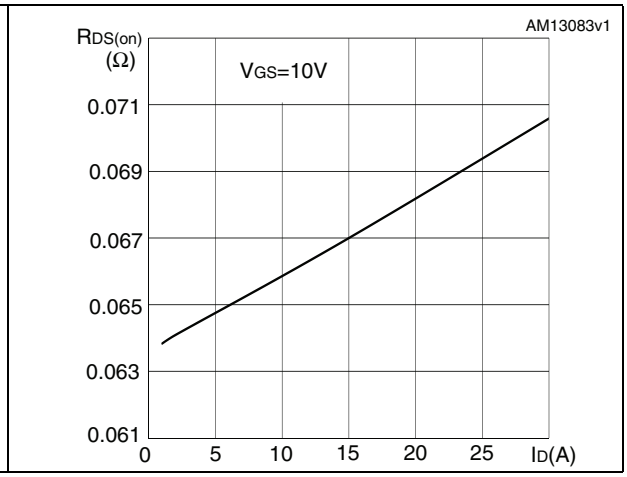



**Figure 10. Capacitance variations**

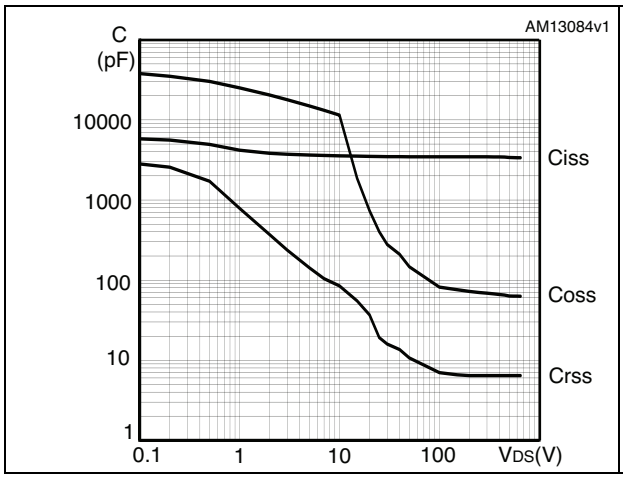



**Figure 11. Output capacitance stored energy**

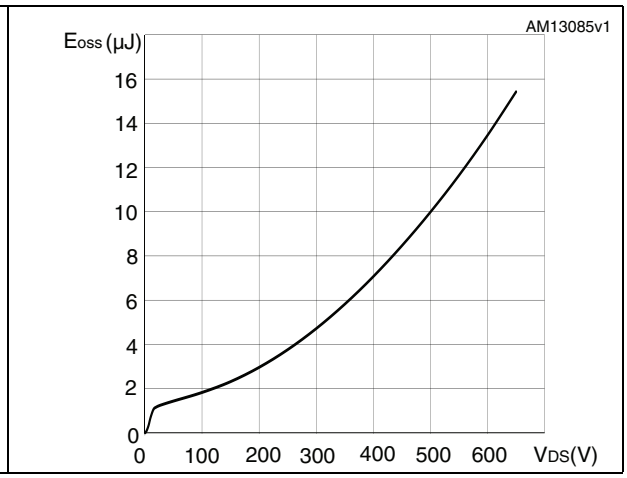



**Figure 12. Normalized gate threshold voltage vs. temperature**

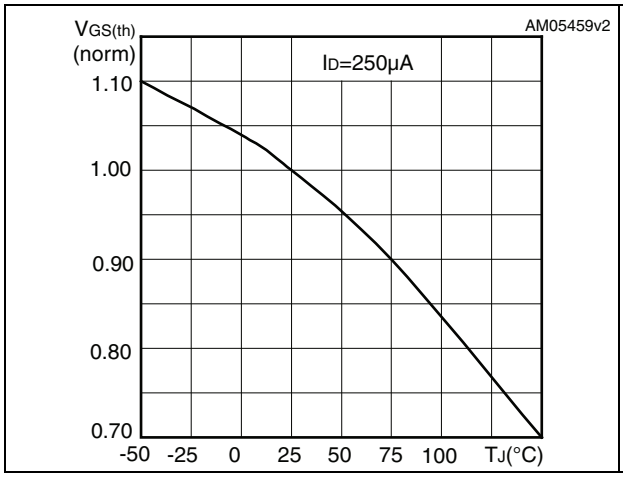



**Figure 13. Normalized on-resistance vs. temperature**

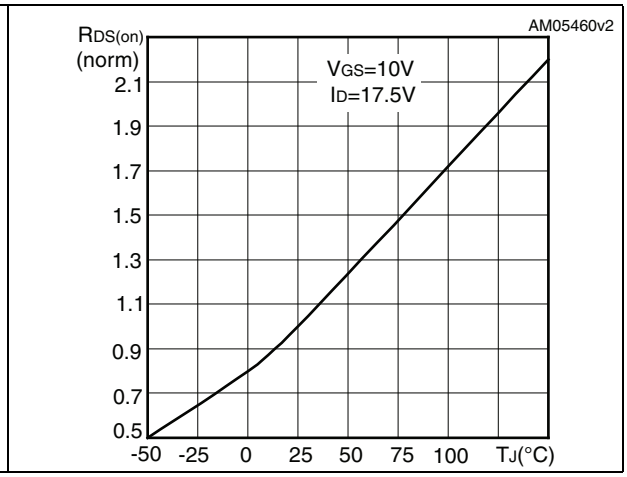


**Figure 14. Drain-source diode forward characteristics**

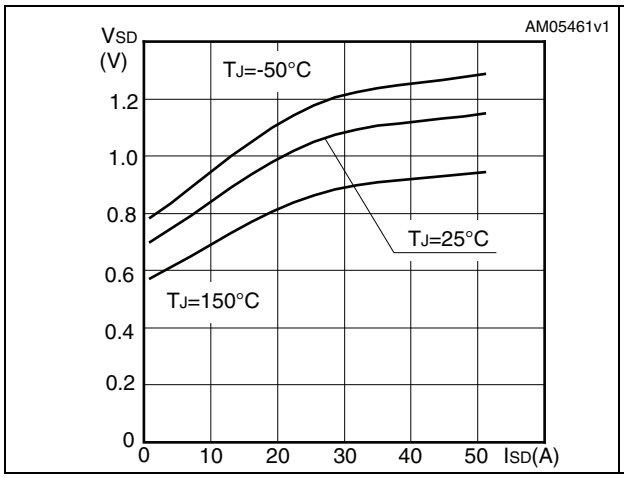



**Figure 15. Normalized $V_{(BR)DSS}$ vs. temperature**

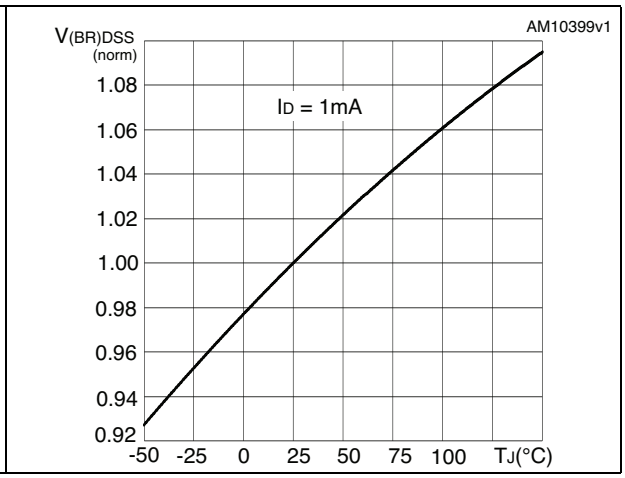
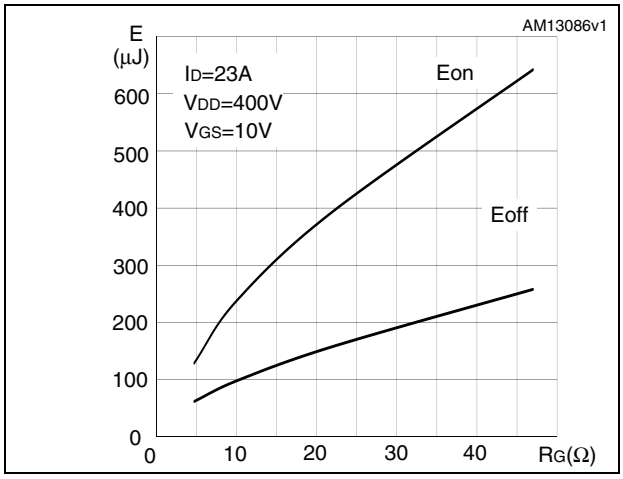



**Figure 16. Switching losses vs. gate resistance (1)**




1. Eon including reverse recovery of a SiC diode

# 3 Test circuits

**Figure 17. Switching times test circuit for resistive load**

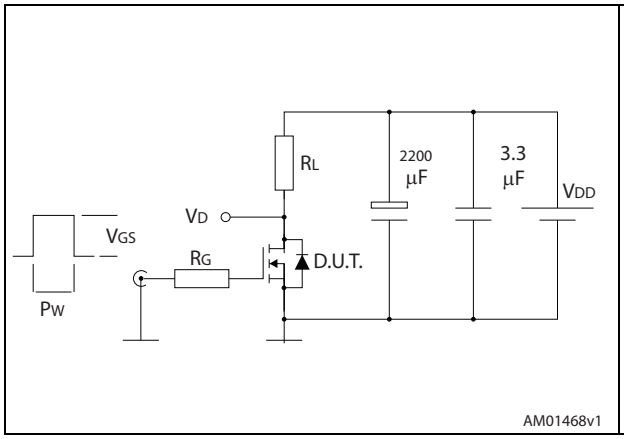



**Figure 18. Gate charge test circuit**

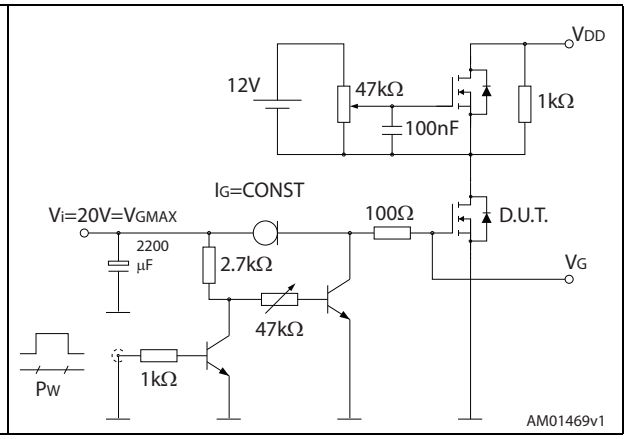



**Figure 19. Test circuit for inductive load switching and diode recovery times**

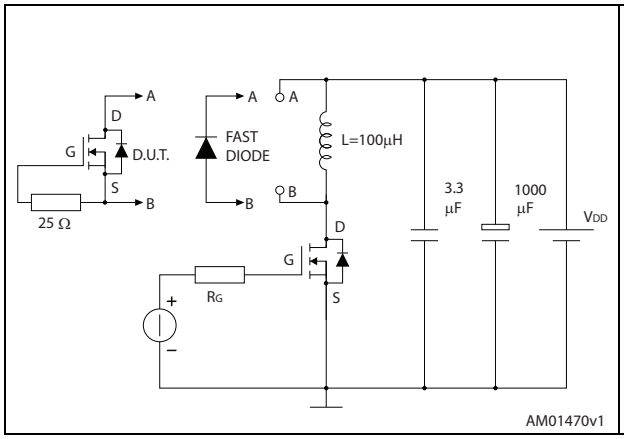



**Figure 20. Unclamped inductive load test circuit**

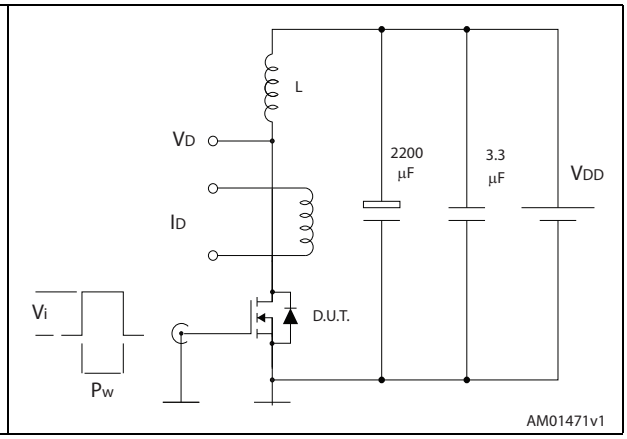



**Figure 21. Unclamped inductive waveform**

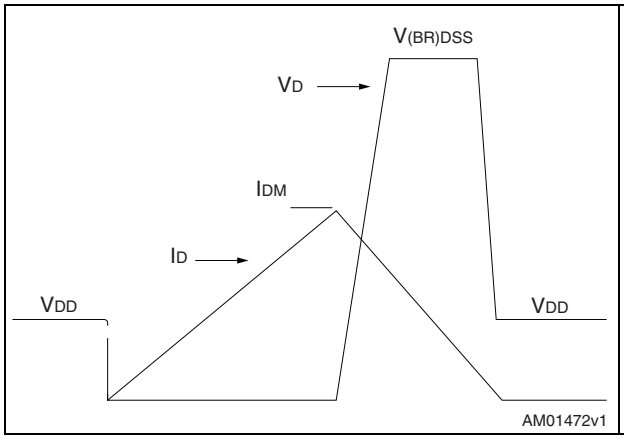
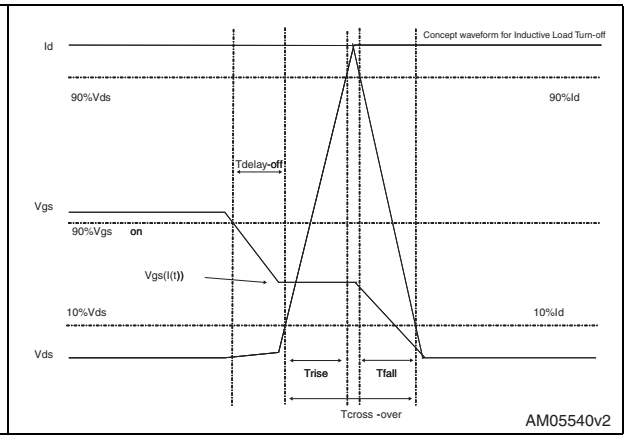



**Figure 22. Switching time waveform**



# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

## 4.1 TO-3PF, STFW45N65M5

**Figure 23. TO-3PF drawing**

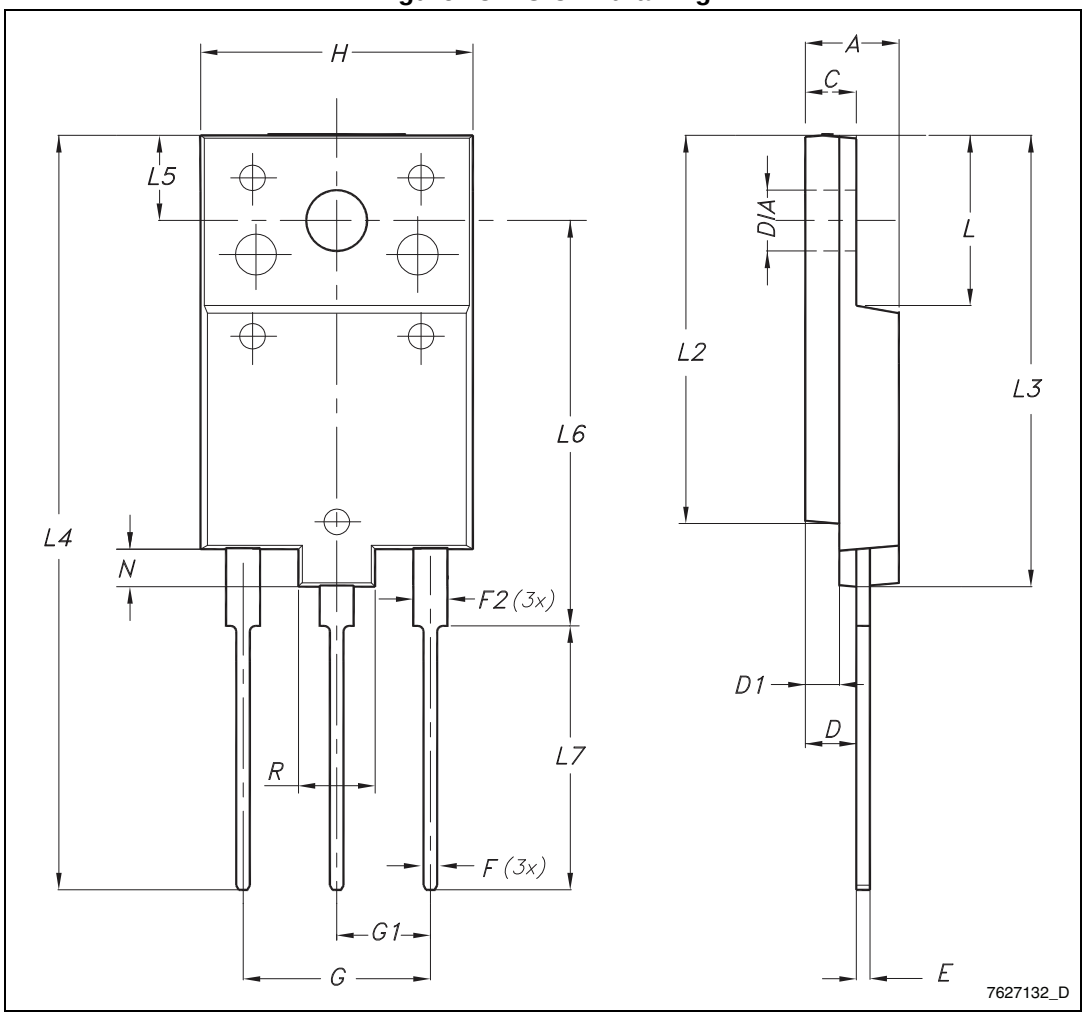


Table 9. TO-3PF mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 5.30 | | 5.70 |
| C | 2.80 | | 3.20 |
| D | 3.10 | | 3.50 |
| D1 | 1.80 | | 2.20 |
| E | 0.80 | | 1.10 |
| F | 0.65 | | 0.95 |
| F2 | 1.80 | | 2.20 |
| G | 10.30 | | 11.50 |
| G1 | | 5.45 | |
| H | 15.30 | | 15.70 |
| L | 9.80 | 10 | 10.20 |
| L2 | 22.80 | | 23.20 |
| L3 | 26.30 | | 26.70 |
| L4 | 43.20 | | 44.40 |
| L5 | 4.30 | | 4.70 |
| L6 | 24.30 | | 24.70 |
| L7 | 14.60 | | 15 |
| N | 1.80 | | 2.20 |
| R | 3.80 | | 4.20 |
| ∅ | 3.40 | | 3.80 |

## 4.2 TO-247, STW45N65M5

**Figure 24. TO-247 drawing**

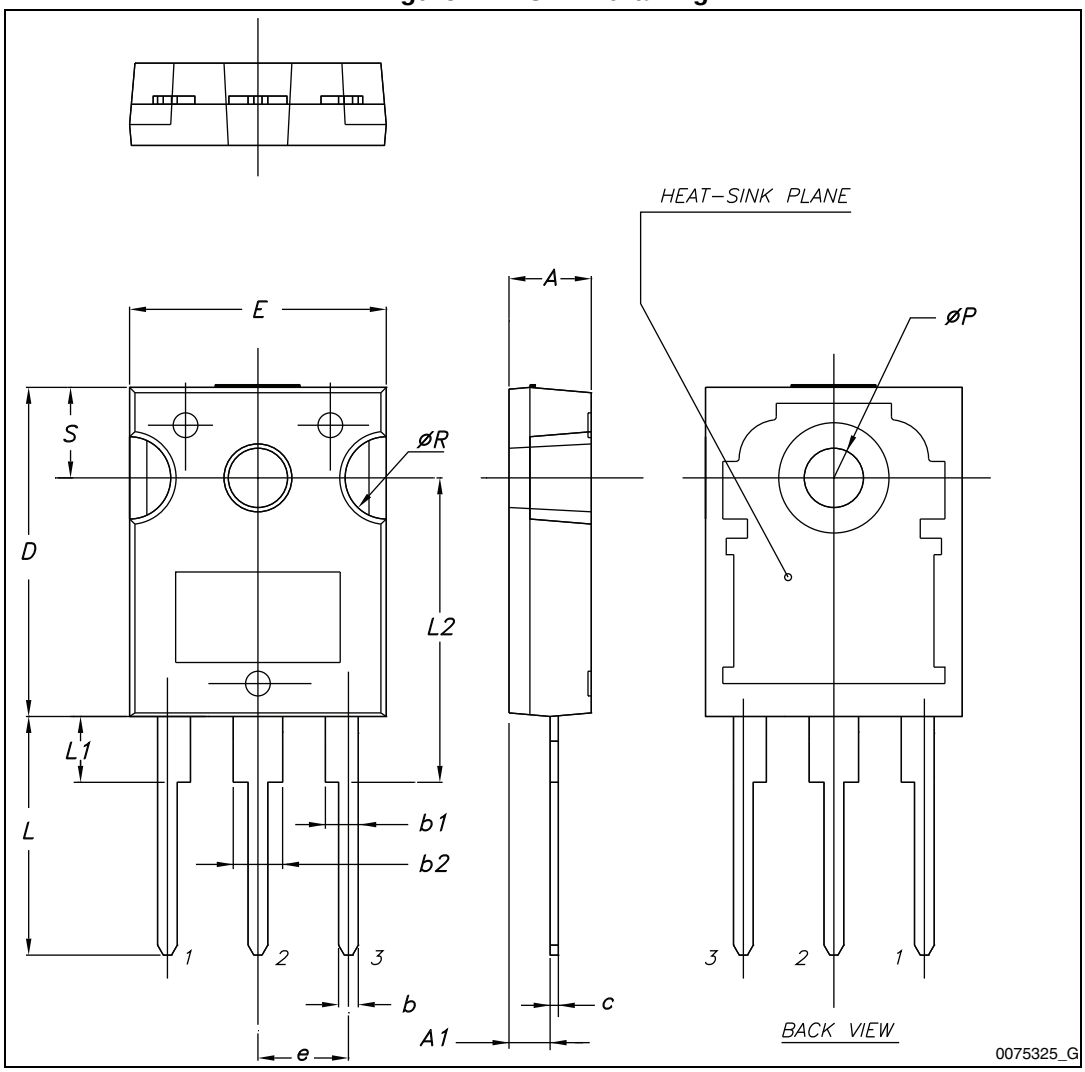


Table 10. TO-247 mechanical data

| Dim. | mm. | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.85 | | 5.15 |
| A1 | 2.20 | | 2.60 |
| b | 1.0 | | 1.40 |
| b1 | 2.0 | | 2.40 |
| b2 | 3.0 | | 3.40 |
| c | 0.40 | | 0.80 |
| D | 19.85 | | 20.15 |
| E | 15.45 | | 15.75 |
| e | 5.30 | 5.45 | 5.60 |
| L | 14.20 | | 14.80 |
| L1 | 3.70 | | 4.30 |
| L2 | | 18.50 | |
| ∅P | 3.55 | | 3.65 |
| ∅R | 4.50 | | 5.50 |
| S | 5.30 | 5.50 | 5.70 |

## 4.3 TO-247 long leads, STWA45N65M5

**Figure 25. TO-247 long leads drawing**

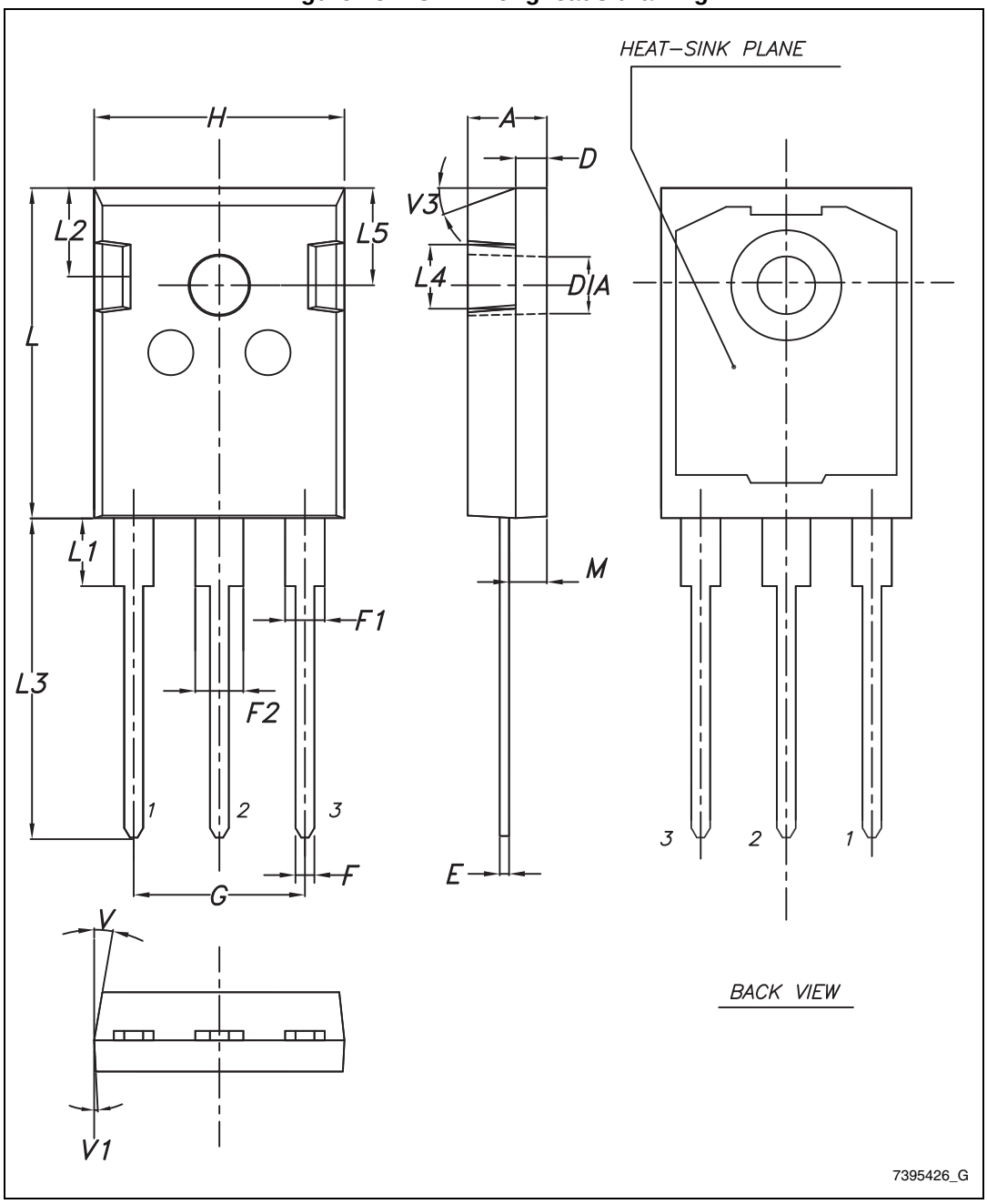


Table 11. TO-247 long leads mechanical data

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 4.90 | | 5.15 |
| D | 1.85 | | 2.10 |
| E | 0.55 | | 0.67 |
| F | 1.07 | | 1.32 |
| F1 | 1.90 | | 2.38 |
| F2 | 2.87 | | 3.38 |
| G | | 10.90 BSC | |
| H | 15.77 | | 16.02 |
| L | 20.82 | | 21.07 |
| L1 | 4.16 | | 4.47 |
| L2 | 5.49 | | 5.74 |
| L3 | 20.05 | | 20.30 |
| L4 | 3.68 | | 3.93 |
| L5 | 6.04 | | 6.29 |
| M | 2.25 | | 2.55 |
| V | | 10° | |
| V1 | | 3° | |
| V3 | | 20° | |
| Dia. | 3.55 | | 3.66 |

# 5 Revision history

Table 12. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 11-Dec-2012 | 1 | First release. |
| 09-May-2014 | 2 | – Added: TO-3PF package<br>– Added: dv/dt (MOSFET dv/dt ruggedness) parameter and $V_{ISO}$<br>– Modified: *Figure 6* and *7*<br>– Minor text changes |

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