# ON Semiconductor

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# BD809 (NPN), BD810 (PNP)

# Plastic High Power Silicon Transistors

These devices are designed for use in high power audio amplifiers utilizing complementary or quasi complementary circuits.

**Features**

- High DC Current Gain
- These Devices are Pb−Free and are RoHS Compliant*

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector−Emitter Voltage | $V_{CEO}$ | 80 | Vdc |
| Collector−Base Voltage | $V_{CBO}$ | 80 | Vdc |
| Emitter−Base Voltage | $V_{EBO}$ | 5.0 | Vdc |
| Collector Current | $I_C$ | 10 | Adc |
| Base Current | $I_B$ | 6.0 | Adc |
| Total Device Dissipation<br>@ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | <br>90<br>0.72 | <br>W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL CHARACTERISTICS**

| Characteristics | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Case | $R_{\theta JC}$ | 1.39 | °C/W |

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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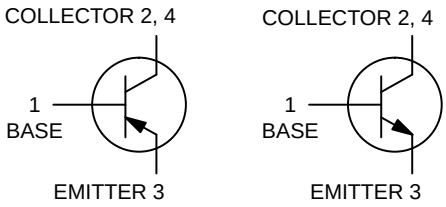
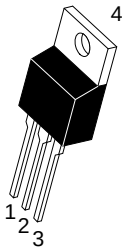
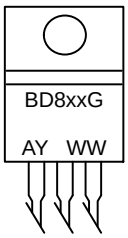
**10 AMPERE POWER TRANSISTORS 80 VOLTS 90 WATTS**




**TO−220**
**CASE 221A**
**STYLE 1**

**MARKING DIAGRAM**




| | | |
|---|---|---|
| BD8xx | = | Device Code<br>x = 09 or 10 |
| A | = | Assembly Location |
| Y | = | Year |
| WW | = | Work Week |
| G | = | Pb−Free Package |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| BD809G | TO−220<br>(Pb−Free) | 50 Units/Rail |
| BD810G | TO−220<br>(Pb−Free) | 50 Units/Rail |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Collector−Emitter Sustaining Voltage (Note 1)<br>($I_C$ = 0.1 Adc, $I_B$ = 0) | $BV_{CEO}$ | 80 | – | Vdc |
| Collector Cutoff Current<br>($V_{CB}$ = 80 Vdc, $I_E$ = 0) | $I_{CBO}$ | – | 1.0 | mAdc |
| Emitter Cutoff Current<br>($V_{BE}$ = 5.0 Vdc, $I_C$ = 0) | $I_{EBO}$ | – | 2.0 | mAdc |
| DC Current Gain<br>($I_C$ = 2.0 A, $V_{CE}$ = 2.0 V)<br>($I_C$ = 4.0 A, $V_{CE}$ = 2.0 V) | $h_{FE}$ | 30<br>15 | –<br>– | – |
| Collector−Emitter Saturation Voltage (Note 1)<br>($I_C$ = 3.0 Adc, $I_B$ = 0.3 Adc) | $V_{CE(sat)}$ | – | 1.1 | Vdc |
| Base−Emitter On Voltage (Note 1)<br>($I_C$ = 4.0 Adc, $V_{CE}$ = 2.0 Vdc) | $V_{BE(on)}$ | – | 1.6 | Vdc |
| Current−Gain Bandwidth Product<br>($I_C$ = 1.0 Adc, $V_{CE}$ = 10 Vdc, f = 1.0 MHz) | $f_T$ | 1.5 | – | MHz |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

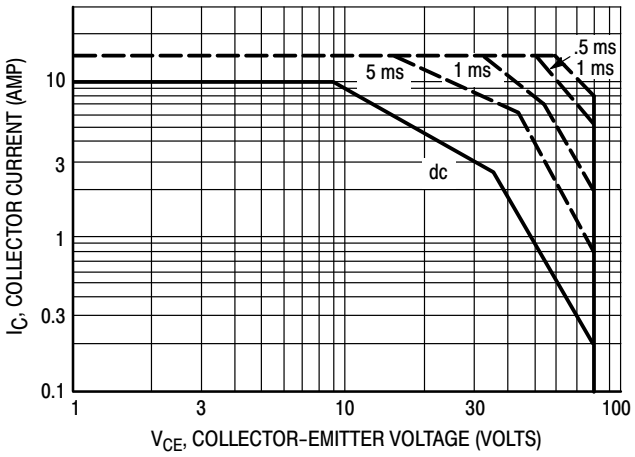



**Figure 1. Active Region DC Safe Operating Area**

(see Note on page 3)

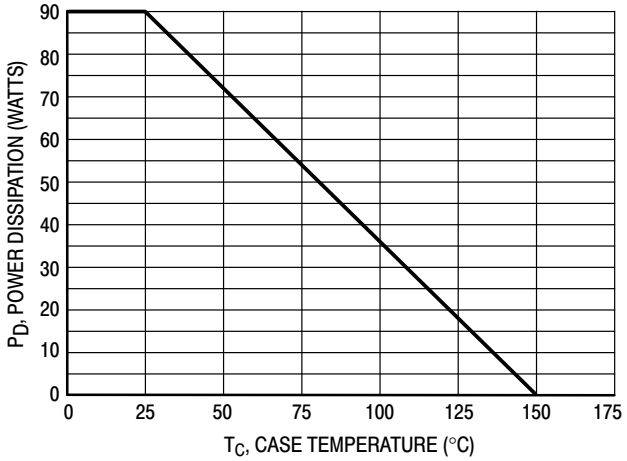



**Figure 2. Power−Temperature Derating Curve**

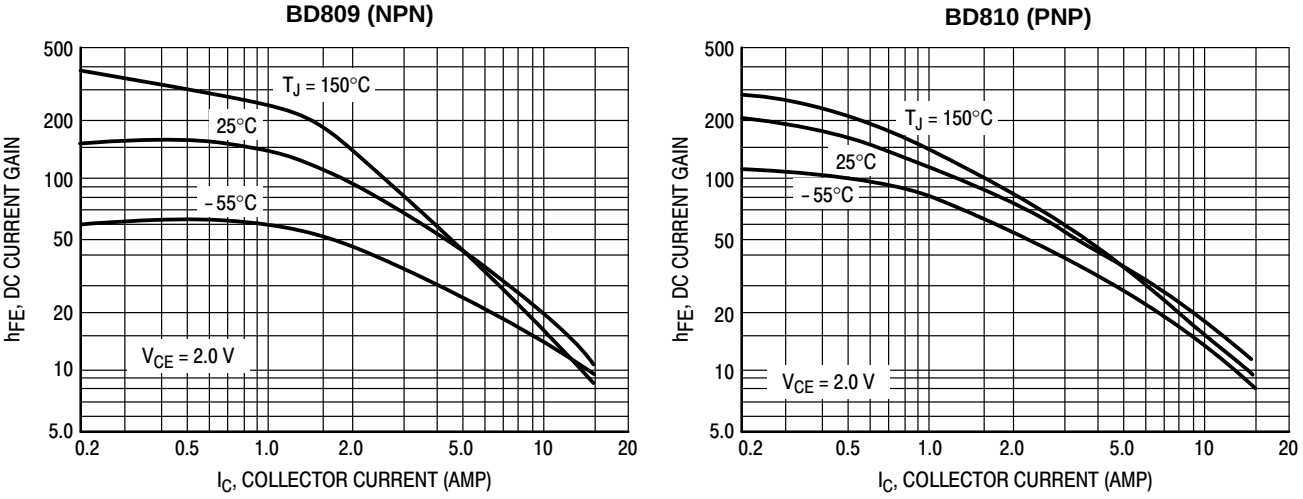



**Figure 3. DC Current Gain**

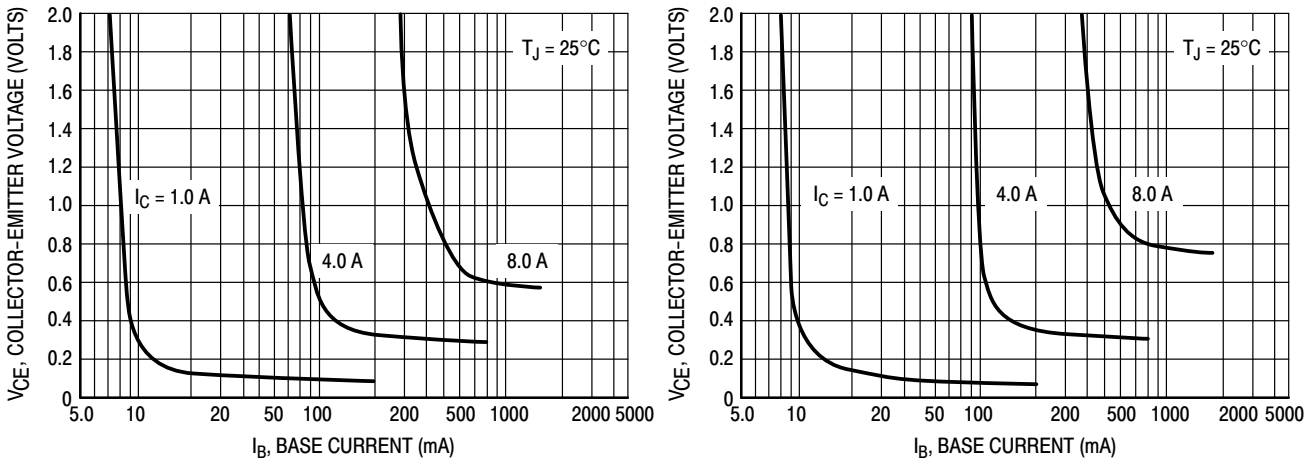



**Figure 4. Collector Saturation Region**

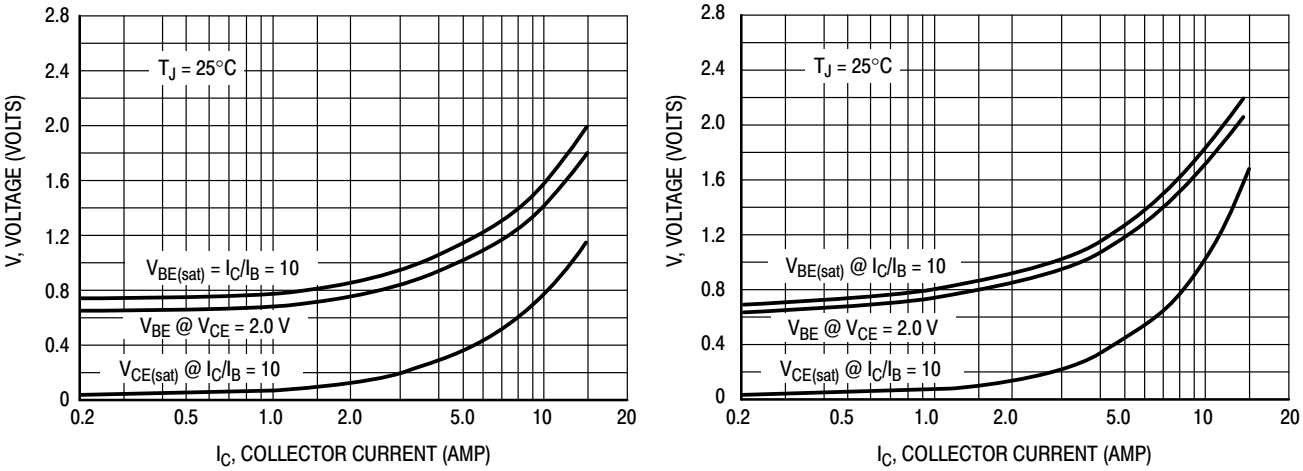



**Figure 5. "On" Voltages**

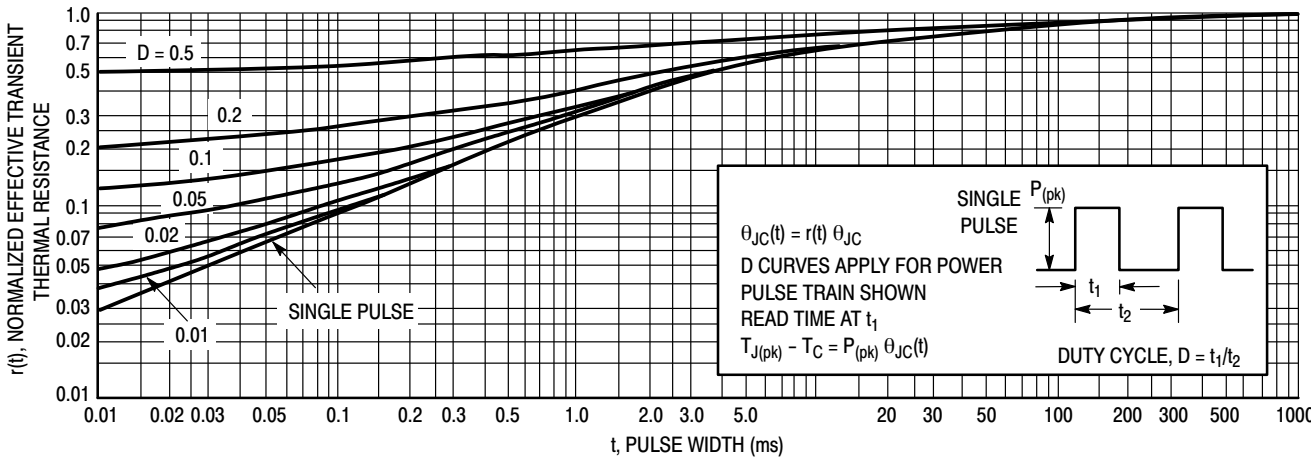



**Figure 6. Thermal Response**

**Note:**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

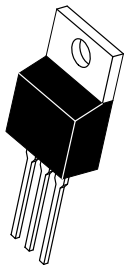
The data of Figure 1 is based on $T_{J(pk)}$ = 150°C; $T_C$ is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150°C. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

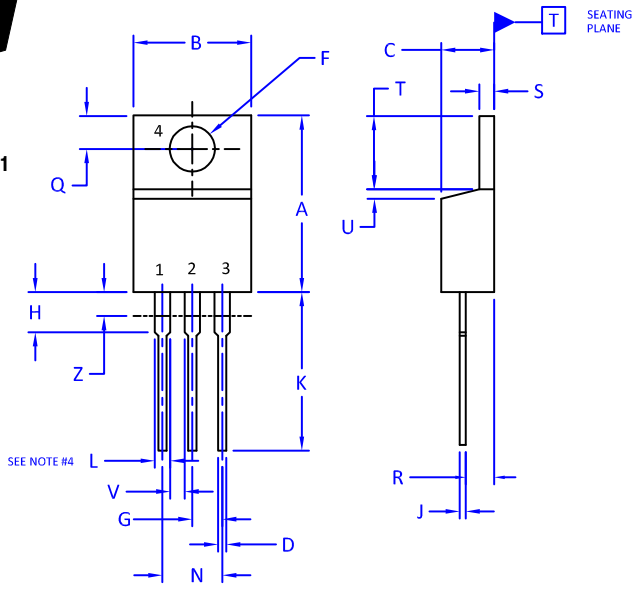
ON Semiconductor®

**TO−220**
CASE 221A−09
ISSUE AJ

DATE 05 NOV 2019



SCALE 1:1




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN. | MAX. | MIN. | MAX. |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.415 | 9.66 | 10.53 |
| C | 0.160 | 0.190 | 4.07 | 4.83 |
| D | 0.025 | 0.038 | 0.64 | 0.96 |
| F | 0.142 | 0.161 | 3.60 | 4.09 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.161 | 2.80 | 4.10 |
| J | 0.014 | 0.024 | 0.36 | 0.61 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.41 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | ---- | 1.15 | --- |
| Z | ---- | 0.080 | --- | 2.04 |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

| | | |
|---|---|---|
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| **DESCRIPTION:** | **TO−220** | **PAGE 1 OF 1** |

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