



2SA2127

Bipolar Transistor -50V, -2A, Low VCE(sat), PNP Single MP

ON Semiconductor®

<http://onsemi.com>

Applications

- Voltage regulators, relay drivers, lamp drivers, electrical equipment

Features

- Adoption of MBIT process
- High current capacity and wide ASO
- Low saturation voltage

Specifications

Absolute Maximum Ratings at Ta=25°C

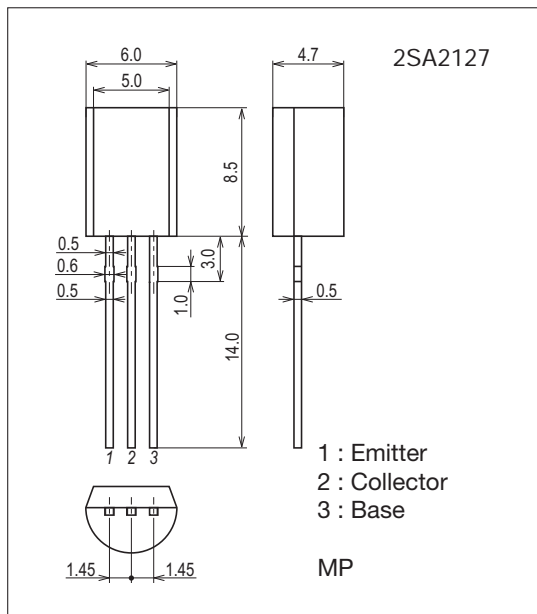
Parameter	Symbol	Conditions	Ratings	Unit
Collector-to-Base Voltage	V _{CBO}		-50	V
Collector-to-Emitter Voltage	V _{CEO}		-50	V
Emitter-to-Base Voltage	V _{EBO}		-6	V
Collector Current	I _C		-2	A
Collector Current (Pulse)	I _{CP}		-4	A
Base Current	I _B		-400	mA
Collector Dissipation	P _C		1	W
Junction Temperature	T _J		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

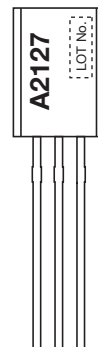
7520-002



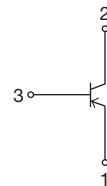
Product & Package Information

- Package : MP
- JEITA, JEDEC : SC-51, TO-92(1-WATT), TO-226AE
- Minimum Packing Quantity : 1,000 pcs./box

Marking



Electrical Connection

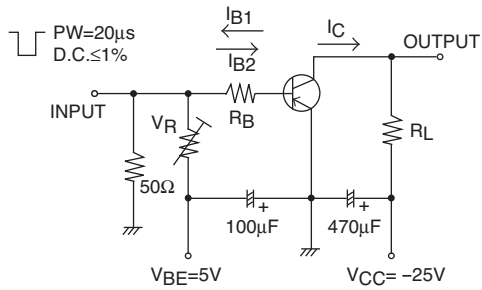


2SA2127

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Collector Cutoff Current	I_{CBO}	$V_{CB} = -40V, I_E = 0A$			-1	μA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = -4V, I_C = 0A$			-1	μA
DC Current Gain	h_{FE1}	$V_{CE} = -2V, I_C = -100mA$	200		560	
	h_{FE2}	$V_{CE} = -2V, I_C = -1.5A$	40			
Gain-Bandwidth Product	f_T	$V_{CE} = -10V, I_C = -300mA$		420		MHz
Output Capacitance	C_{ob}	$V_{CB} = -10V, f = 1MHz$		16		pF
Collector-to-Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = -1A, I_B = -50mA$		-0.2	-0.4	V
Base-to-Emitter Saturation Voltage	$V_{BE(sat)}$	$I_C = -1A, I_B = -50mA$		-0.9	-1.2	V
Collector-to-Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = -10\mu A, I_E = 0A$	-50			V
Collector-to-Emitter Breakdown Voltage	$V_{(BR)CEO}$	$I_C = -1mA, R_{BE} = \infty$	-50			V
Emitter-to-Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = -10\mu A, I_C = 0A$	-6			V
Turn-On Time	t_{on}	See specified Test Circuit.		35		ns
Storage Time	t_{stg}			250		ns
Fall Time	t_f			24		ns

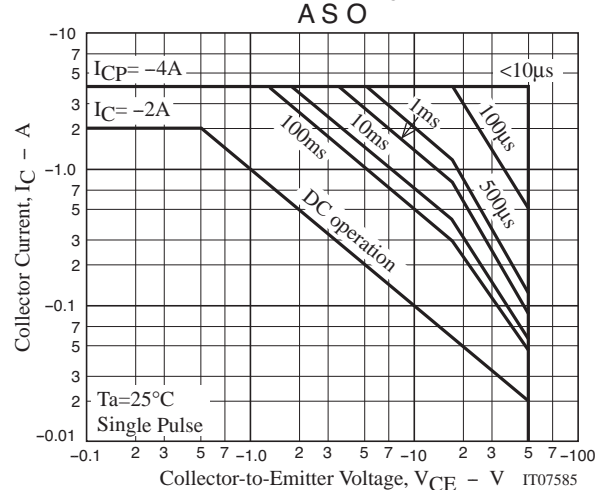
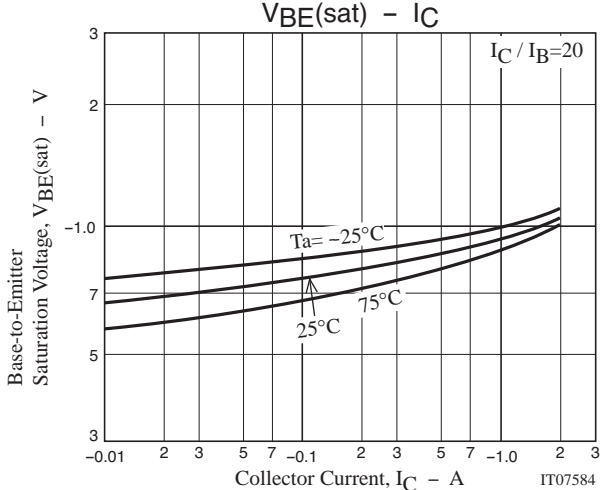
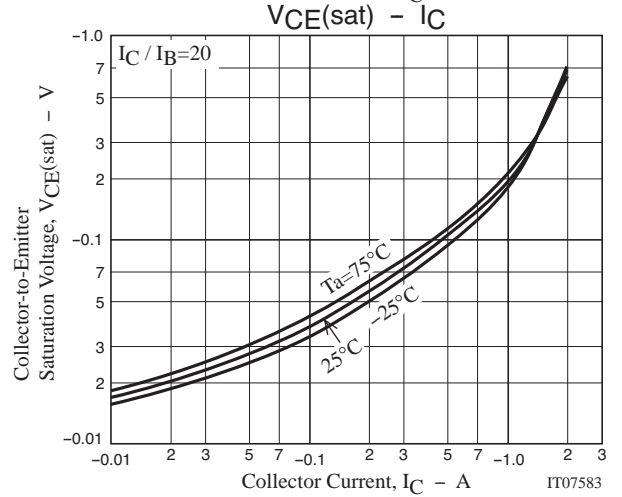
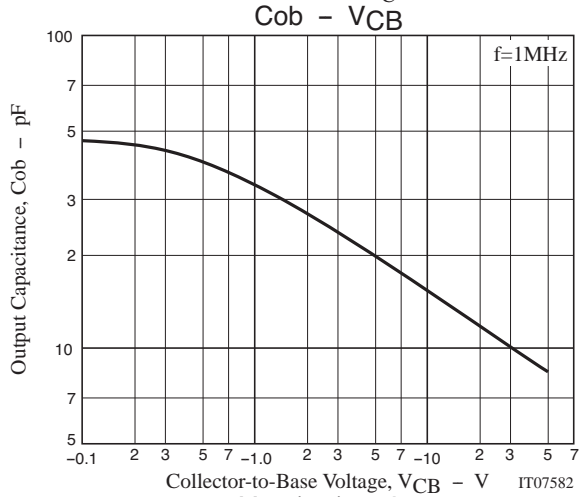
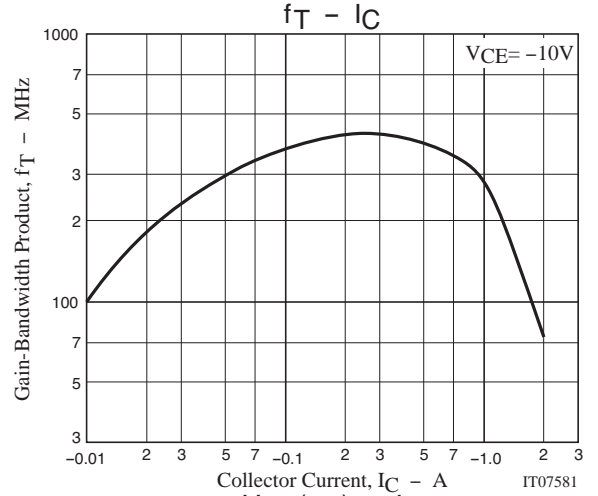
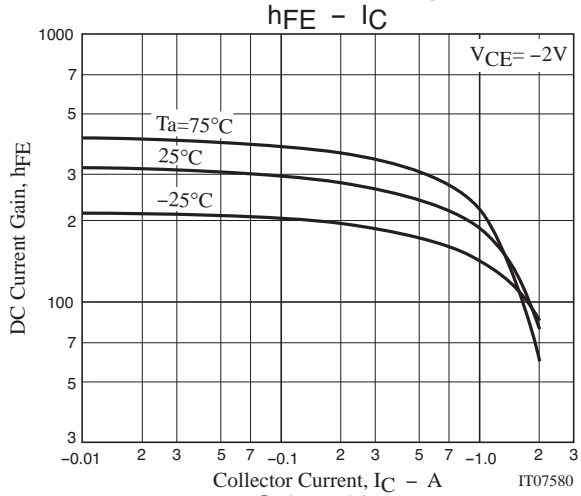
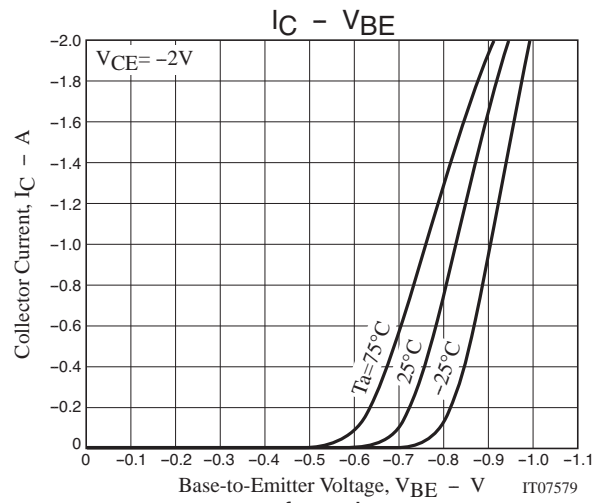
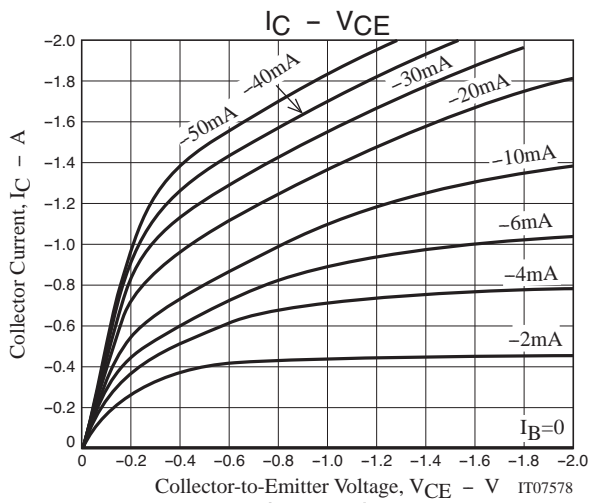
Switching Time Test Circuit

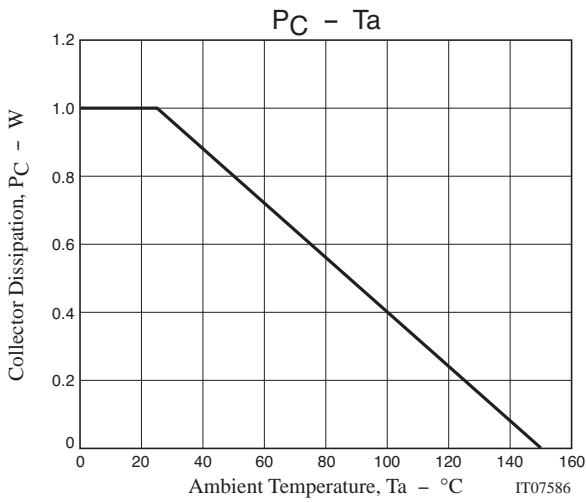


$$I_C = 10I_{B1} = -10I_{B2} = -0.5A$$

Ordering Information

Device	Package	Shipping	memo
2SA2127	MP	500pcs./bag	Pb Free
2SA2127-AE	MP	1,000pcs./box	





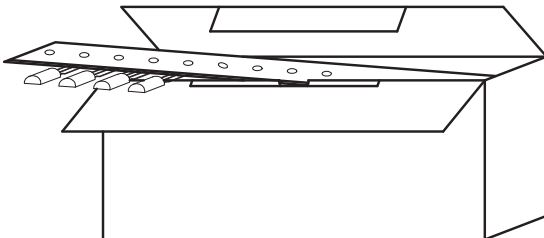
Taping Specification
2SA2127-AE

1. Packing Format

Package Name	Packing Type	Maximum Number of devices contained (pcs)		Packing format	
		Inner BOX	number of contained	Outer Box (C-14)	Outer Box (C-15)
M P	AE/AZ	C-3 Dimensions:mm (external) 330×45×125	1,000	1 Inner Box contained (16,000pcs) Dimensions:mm (external) 500×345×195	8 Inner Box contained (8,000pcs) Dimensions:mm (external) 345×260×195
	A J	C-5 Dimensions:mm (external) 330×45×245	2,000	8 Inner Box contained (16,000pcs) Dimensions:mm (external) 500×345×195	4 Inner Box contained (8,000pcs) Dimensions:mm (external) 345×260×195

Packing method

Put zigzag folding in an inner box.



Inner box label

(unit:mm)

Type No. →	(1) TYPE 00000000	43
Lot No. →	(17) LOT 00	
Quantity →	(20) QTY 0,000 (1) LEAD FREE #	
Origin →	(2) SPECIAL *Z0722005310C* ASSEMBLY:*** (DIFFUSION:***)	

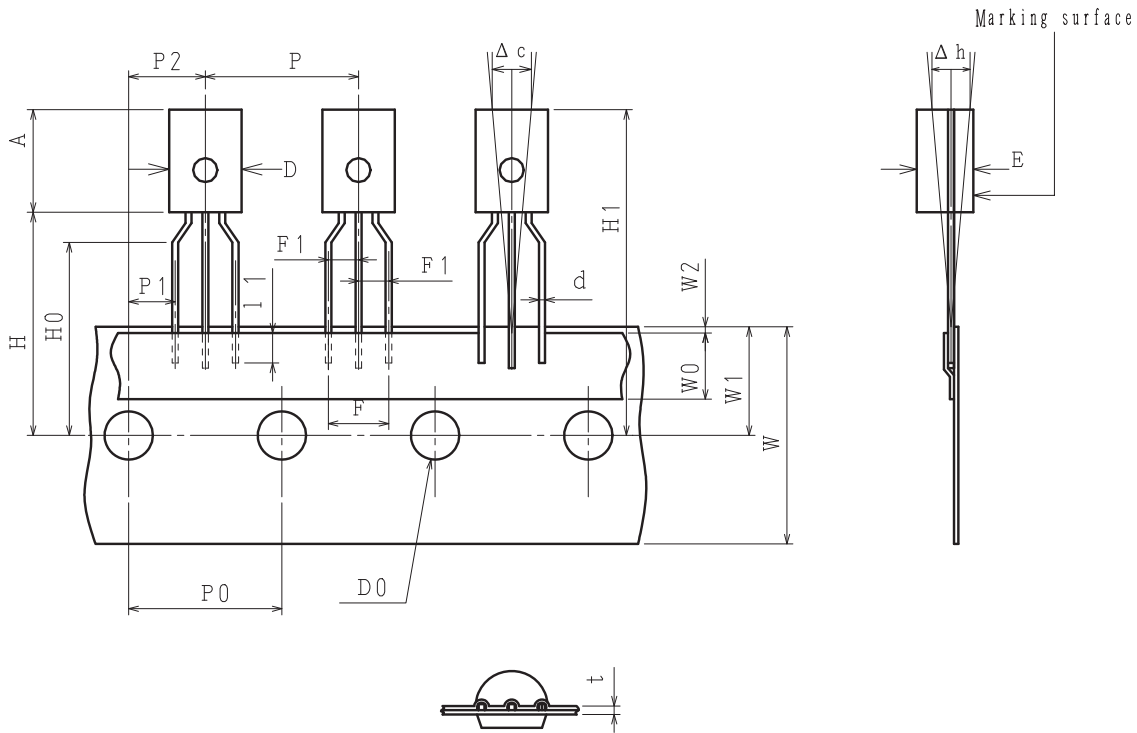
NOTE (1)

The LEAD FREE # description shows that the surface treatment of the terminal is lead free.

Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A
LEAD FREE 4	JEITA Phase 3

2. Taping specifications

2-1. Carrier tape size



2-2. Taping size standard

unit:mm

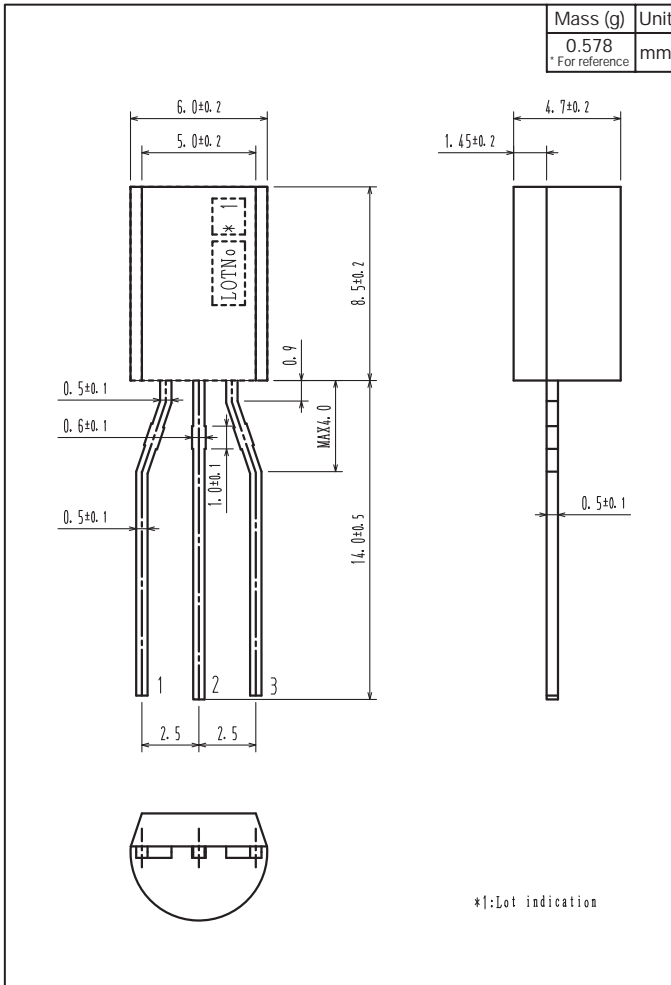
Item	Symbol	Standard	Tolerance	Item	Symbol	Standard	Tolerance
Work piece outside diameter	D	6.0	±0.2	Tape width	W	18.0	+1.0 -0.5
	E	4.7	±0.2	Adhesive tape	W0	6.0	±1.5
Work piece height	A	8.5	±0.2	Displacement of perforations	W1	9.0	±0.5
Lead wire diameter	d	0.5×0.5t	±0.1	Work piece bottom surface position	H	18.5	±1.0
Bonded lead wire	l1	2.5MIN		Insert stopper position	H0	16.0	±0.5
Pitch between products	P	12.7	±1.0	Work piece upper limit position	H1	27.0	±1.5
Pitch between perforations	P0	12.7	±0.2	Perforations diameter	D0	φ4.0	±0.2
Accumulation Pitch	P0×20	254.0	±1.0	Tape thickness	t	0.7	±0.2
Distance between lead wire	F	5.0	+0.8 -0.2	Product inclination	Δc	0	±1.5
Lead wire pitch distance	F1	2.5	+0.4 -0.1				
Product inclination	Δh	0	±2.0				
Displacement of perforations	P1	3.85	±0.3				
	P2	6.35	±0.3				
Displacement of tape	W2	0.5MAX					

Measurement position is the bottom of the clinch

Not to be displaced to the outside of the board

Outline Drawing

2SA2127-AE



Bag Packing Specification

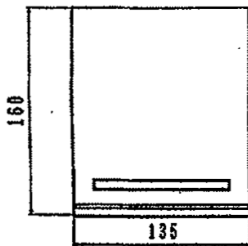
2SA2127

1 . Packing condition

Storage package outline name	Maximum number of devices contained (pcs.)			Packing condition	
	Bags	Inner box	Devices contained	Outer box (A-1)	Outer box (A-2)
MP	500	B-1 Inner box dimensions : mm (external) 445×225×55	5,000	5 inner boxes contained (25,000) Outer box dimensions : mm (external) 470 × 250 × 300	3 inner boxes contained (15,000) Outer box dimensions : mm (external) 470 × 250 × 190

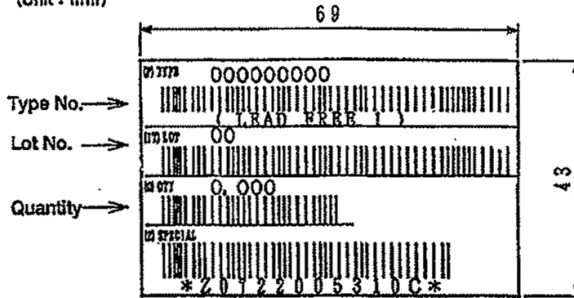
2. Bag dimensions

(Unit : mm)



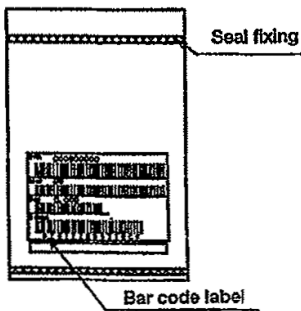
3. Bar code label

(Unit : mm)



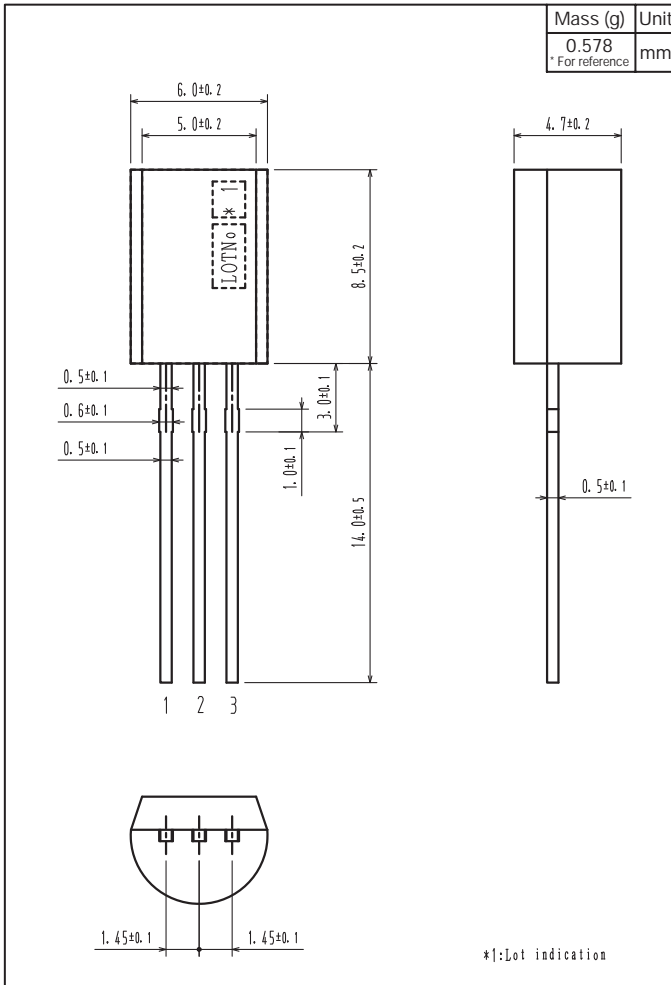
*LEAD FREE 1 :
Lead-free External terminal surface
treatment product.

4. Housing devices in the bag



Outline Drawing

2SA2127



ON Semiconductor and the ON logo are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.