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### FDS3590

### 80V N-Channel PowerTrench® MOSFET

### **General Description**

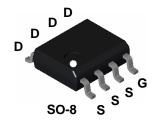
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

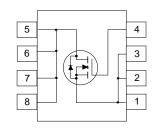
These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{\text{DS(ON)}}$  specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

### **Features**

- 6.5 A, 80 V  $R_{DS(ON)} = 39 \text{ m}\Omega$  @  $V_{GS} = 10 \text{ V}$   $R_{DS(ON)} = 44 \text{ m}\Omega$  @  $V_{GS} = 6 \text{ V}$
- · Low gate charge
- · Fast switching speed
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS(ON)}}$
- High power and current handling capability





Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		80	V
$V_{GSS}$	Gate-Source Voltage		±20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	6.5	A
	- Pulsed		50	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	2.5	W
		(Note 1b)	1.2	
		(Note 1c)	1.0	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	50	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	25	°C/W

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
FDS3590	FDS3590	13"	12mm	2500 units

FDS3590 Rev C (W)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-Sc	ource Avalanche Ratings (Not	te 2)	1	l	l	I
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 40 \text{ V},  I_D = 6.5 \text{ A}$			175	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Current				6.5	Α
Off Char	acteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V},  I_{D} = 250 \mu\text{A}$	80			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		88		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 64 \text{ V},  V_{GS} = 0 \text{ V}$			1	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	$V_{GS} = 20 \text{ V},  V_{DS} = 0 \text{ V}$			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, \ V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)n</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	2		4	V
$\Delta V_{GS(th)} \over \Delta T_{,J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		-6		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$\begin{array}{l} V_{GS} = 10 \; V,  I_D = 6.5 \; A \\ V_{GS} = 10 \; V,  I_D = 6.5 \; A, \; T_J = 125 ^{\circ} C \\ V_{GS} = 6 \; V,  I_D = 4.5 \; A \end{array}$		32 61 34	39 86 44	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V},  V_{DS} = 5 \text{ V}$	25			Α
G <sub>FS</sub>	Forward Transconductance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6.5 A		25		S
Dynamic	Characteristics		•	•		•
Ciss	Input Capacitance	$V_{DS} = 40 \text{ V},  V_{GS} = 0 \text{ V},$		1180		pF
Coss	Output Capacitance	f = 1.0 MHz		171		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			50		pF
Switchin	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 40 \text{ V},  I_{D} = 1 \text{ A},$		11	20	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V},  R_{GEN} = 6 \Omega$		8	16	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			26	50	ns
t <sub>f</sub>	Turn-Off Fall Time			12	25	ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 40 \text{ V},  I_{D} = 6.5 \text{ A},$		25	35	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		4.5		nC
$Q_{gd}$	Gate-Drain Charge			5.8		nC
Drain-So	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source				2.1	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = 2.1 \text{ A}$ (Note 2)		0.74	1.2	V

#### Notes

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 50 °C/W when mounted on a 1in² pad of 2 oz copper



b) 105 °C/W when mounted on a 0.04 in² pad of 2 oz copper



c) 125 °C/W when mounted on a minimum pad.

FDS3590 Rev C. (W)

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

### **Typical Characteristics**

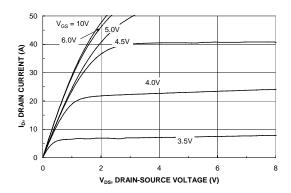


Figure 1. On-Region Characteristics.

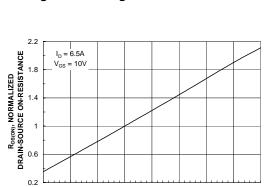


Figure 3. On-Resistance Variation with Temperature.

25

50 75

T<sub>J</sub>, JUNCTION TEMPERATURE (°C)

125 150

100

-25

-50

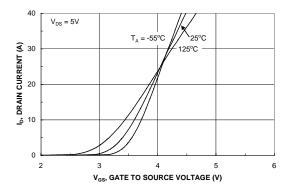


Figure 5. Transfer Characteristics.

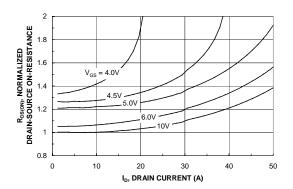


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

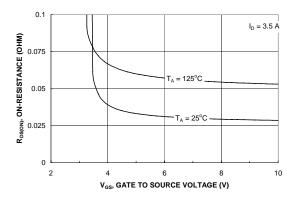


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

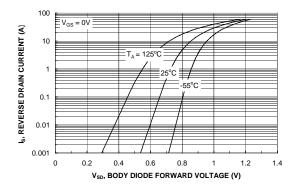
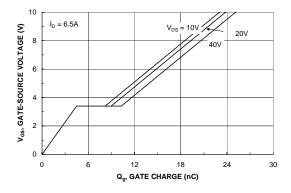


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

FDS3590 Rev C. (W)

### **Typical Characteristics**



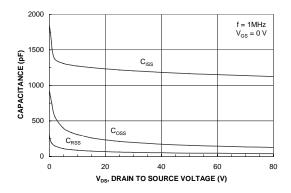


Figure 7. Gate Charge Characteristics.

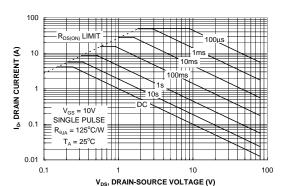


Figure 8. Capacitance Characteristics.

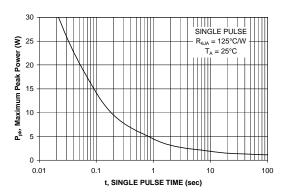


Figure 9. Maximum Safe Operating Area.



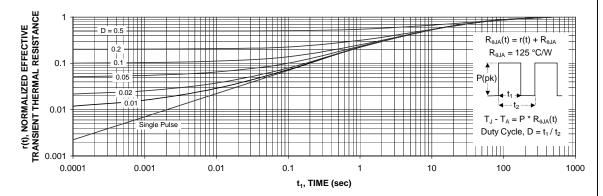


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

FDS3590 Rev C. (W)

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