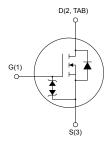


N-channel 650 V, 0.91 Ω typ., 5 A, MDmesh™ M6 Power MOSFET in a DPAK package

Features



DPAK



Order code	V _{DS}	R _{DS(on)} max.	l _D
STD7N65M6	650 V	0.99 Ω	5 A

- · Reduced switching losses
- Lower R_{DS(on)} per area vs previous generation
- · Low gate input resistance
- 100% avalanche tested
- · Zener-protected

Applications

· Switching applications

Description

The new MDmesh $^{\intercal}$ M M6 technology incorporates the most recent advancements to the well-known and consolidated MDmesh family of SJ MOSFETs. STMicroelectronics builds on the previous generation of MDmesh devices through its new M6 technology, which combines excellent $R_{DS(on)}$ per area improvement with one of the most effective switching behaviors available, as well as a user-friendly experience for maximum end-application efficiency.



Product status link STD7N65M6

Product summary			
Order code	STD7N65M6		
Marking	7N65M6		
Package	DPAK		
Packing	Tape and reel		



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±25	V
I _D	Drain current (continuous) at T _C = 25 °C	5	Α
I _D	Drain current (continuous) at T _C = 100 °C	3.2	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	20	Α
P _{TOT}	Total power dissipation at T _C = 25 °C	60	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	5	V/ns
dv/dt ⁽³⁾	MOSFET dv/dt ruggedness	50	V/IIS
TJ	Operating junction temperature range	-55 to 150	°C
T _{stg}	Storage temperature range	-55 to 150	

- 1. Pulse width limited by safe operating area.
- 2. $I_{SD} \le 5$ A, $di/dt \le 400$ A/ μ s, $V_{DS\ peak} < V_{(BR)DSS}$, $V_{DD} = 400$ V
- 3. $V_{DS} \le 520 \text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	2.08	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	50	C/VV

1. When mounted on FR-4 board of inch², 2oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T _{jmax})	1.5	Α
E _{as}	Single pulse avalanche energy (starting $T_j = 25$ °C, $I_D = I_{AR}$, $V_{DD} = 50$ V)	95	mJ

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2 Electrical characteristics

 T_C = 25 °C unless otherwise specified

Table 4. On/off state

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0, I _D = 1 mA	650			V
		V _{GS} = 0 V, V _{DS} = 650 V			1	μA
I _{DSS}	Zero gate voltage drain current	$V_{GS} = 0 \text{ V}, V_{DS} = 650 \text{ V},$ $T_C = 125 {}^{\circ}\text{C}^{(1)}$			100	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±25 V			±5	μA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.25	3	3.75	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 2.5 A		0.91	0.99	Ω

^{1.} Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	220	-	pF
C _{oss}	Output capacitance	$V_{DS} = 100 \text{ V, f} = 1 \text{ MHz, V}_{GS} = 0 \text{ V}$	-	25	-	pF
C _{rss}	Reverse transfer capacitance		-	1.1	-	pF
C _{oss eq.} (1)	Equivalent output capacitance	V _{DS} = 0 to 520 V, V _{GS} = 0 V	-	45	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz, I _D = 0 A	-	6.3	-	Ω
Qg	Total gate charge	V _{DD} = 520 V, I _D = 5 A,	-	6.9	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 0 to 10 V	-	1.3	-	nC
Q _{gd}	Gate-drain charge	(see Figure 14. Test circuit for gate charge behavior)	-	3.1	-	nC

^{1.} $C_{\rm oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as $C_{\rm oss}$ when $V_{\rm DS}$ increases from 0 to 80% $V_{\rm DSS}$.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 325 V, I _D = 2.5 A,	-	6.5	-	ns
t _r	Rise time	$R_G = 4.7 \Omega, V_{GS} = 10 V$	-	4.5	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and	-	21.4	-	ns
t _f	Fall time	resistive load switching times and Figure 18. Switching time waveform)	-	12.4	-	ns

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Table 7. Source-drain diode

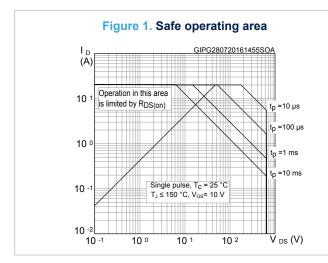
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		5	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		20	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 5 A, V _{GS} = 0 V	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 5 A, di/dt = 100 A/μs,	-	171		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V	-	1		μC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	11.8		A
t _{rr}	Reverse recovery time	I _{SD} = 5 A, di/dt = 100 A/μs,	-	234		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V, T _j = 150 °C	-	1.2		μC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	10.8		A

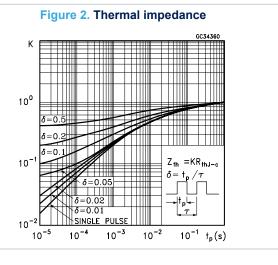
^{1.} Pulse width limited by safe operating area.

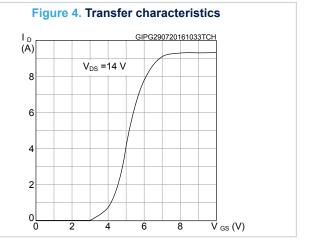
^{2.} Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.

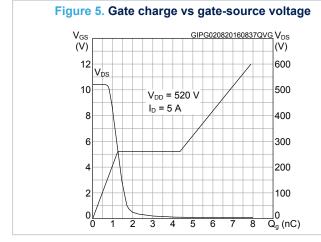


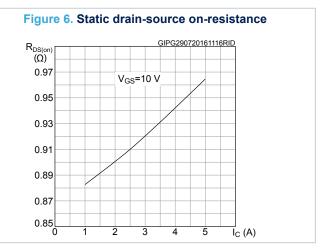
2.1 Electrical characteristics (curves)











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Figure 7. Capacitance variations C (pF) GIPG290720161128CVR 10³ C ISS 10² C oss 10 f = 1 MHz C RSS 10 0 10 -1 $\overline{\mathsf{V}}_{\mathsf{DS}}\left(\mathsf{V}\right)$ 10 -1 10 º 10 ¹ 10²

Figure 8. Normalized gate threshold voltage vs temperature

V _{GS(th)} (norm.)

1.1

1

0.9

0.8

0.7

0.6

-75 -25 25 75 125 T_J (°C)

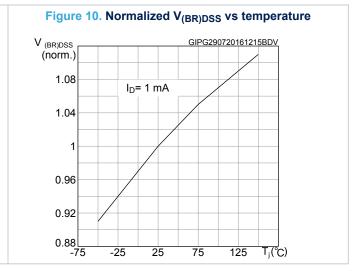
Figure 9. Normalized on-resistance vs temperature

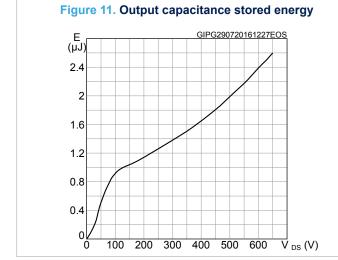
R DS(on) (norm.)

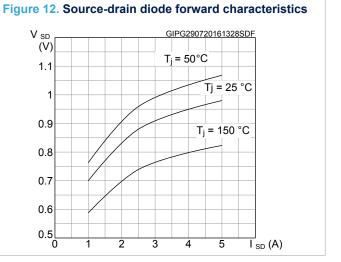
2.2 V GS = 10 V

1.8 1.4 1

0.6 0.2 -75 -25 25 75 125 Tj(°C)







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3 Test circuits

Figure 13. Test circuit for resistive load switching times

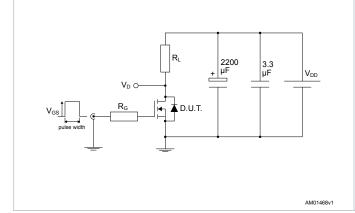


Figure 14. Test circuit for gate charge behavior

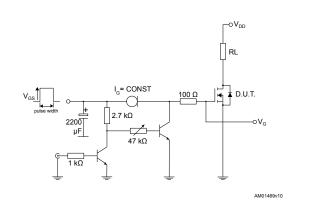


Figure 15. Test circuit for inductive load switching and diode recovery times

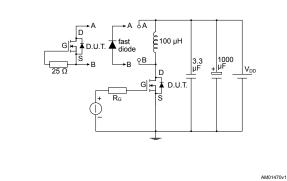


Figure 16. Unclamped inductive load test circuit

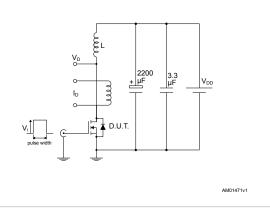


Figure 17. Unclamped inductive waveform

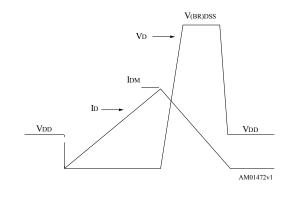
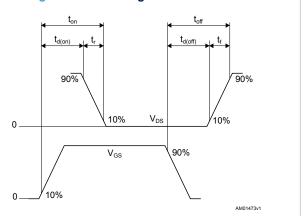


Figure 18. Switching time waveform



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4 Package information

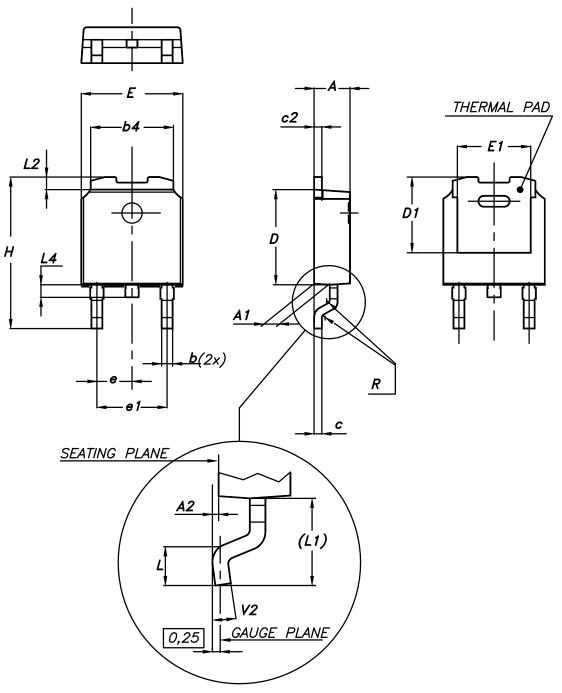
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

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4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



0068772_A_25



Table 8. DPAK (TO-252) type A mechanical data

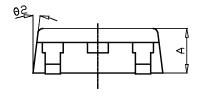
Dim.		mm	
Dilli.	Min.	Тур.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
е	2.159	2.286	2.413
e1	4.445	4.572	4.699
Н	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

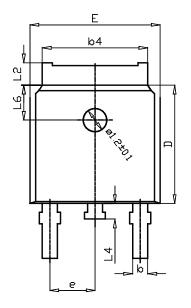
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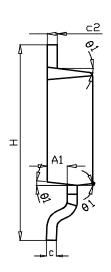


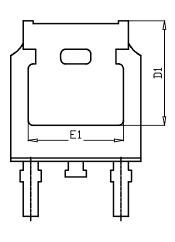
DPAK (TO-252) type C package information 4.2

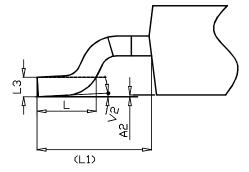
Figure 20. DPAK (TO-252) type C package outline











0068772_C_25



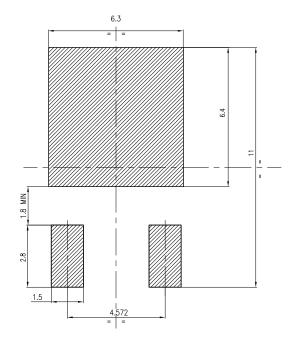
Table 9. DPAK (TO-252) type C mechanical data

Dim.		mm	
Dim.	Min.	Тур.	Max.
А	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
С	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
е	2.186	2.286	2.386
Н	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

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Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)



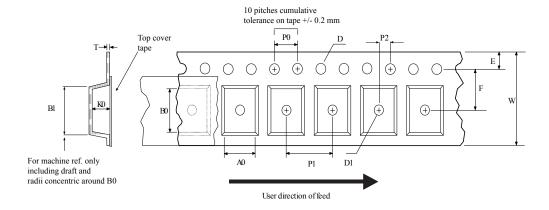
FP_0068772_25_C

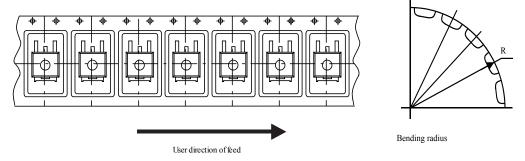
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4.3 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



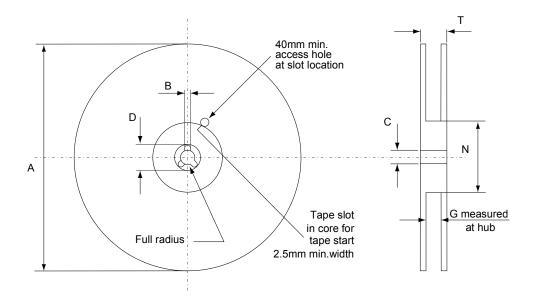


AM08852v1

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Figure 23. DPAK (TO-252) reel outline



AM06038v1

Table 10. DPAK (TO-252) tape and reel mechanical data

Таре			Reel		
Dim.	r	mm Dim.		mm	
Dim.	Min.	Max.	Dim.	Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Bas	e qty.	2500
P1	7.9	8.1	Bul	k qty.	2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

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Revision history

Table 11. Document revision history

Date	Revision	Changes
03-Aug-2016	1	Initial release.
		Updated Figure 14. Test circuit for gate charge behavior.
15-Oct-2018	2	Updated Section 4 Package information.
		Minor text changes

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