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FDC6392S

20V Integrated P-Channel PowerTrench® MOSFET and Schottky Diode

General Description

The FDC6392S combines the exceptional performance of Fairchild's PowerTrench MOSFET technology with a very low forward voltage drop Schottky barrier rectifier in an SSOT-6 package.

This device is designed specifically as a single package solution for DC to DC converters. It features a fast switching, low gate charge MOSFET with very low on-state resistance. The independently connected Schottky diode allows its use in a variety of DC/DC converter topologies.

Features

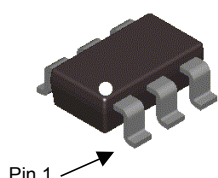
MOSFET:

- -2.2 A, -20V. $R_{DS(ON)} = 150\text{ m}\Omega @ V_{GS} = -4.5\text{V}$
 $R_{DS(ON)} = 200\text{ m}\Omega @ V_{GS} = -2.5\text{V}$
- Low Gate Charge (3.7nC typ)

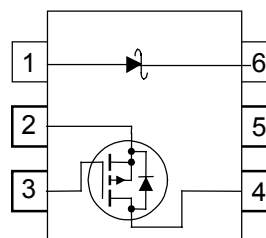
- Compact industry standard SuperSOT™-6 package

Schottky:

- $V_F < 0.45\text{ V} @ 1\text{ A}$



SuperSOT™-6



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V _{DSS}	MOSFET Drain-Source Voltage	-20	V
V _{GSS}	MOSFET Gate-Source Voltage	±12	V
I _D	Drain Current – Continuous (Note 1a)	-2.2	A
	– Pulsed	-6	
P _D	Power Dissipation for Single Operation (Note 1a)	0.96	W
	(Note 1b)	0.9	
	(Note 1c)	0.7	
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C
V _{RRM}	Schottky Repetitive Peak Reverse Voltage	20	V
I _O	Schottky Average Forward Current (Note 1a)	1	A

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	60	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.392	FDC6392S	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		-16		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.6	-1.0	-1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -2.2\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -1.8\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -2.2\text{ A}, T_J = 125^\circ\text{C}$		101 152 132	150 200 211	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-6			A
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -2.2\text{ A}$		6		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		369		pF
C_{oss}	Output Capacitance			80		pF
C_{rss}	Reverse Transfer Capacitance			39		pF
R_G	Gate Resistance	$V_{GS} = -15\text{ mV}, f = 1.0\text{ MHz}$		7.6		Ω

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		8	16	ns
t_r	Turn–On Rise Time			11	20	ns
$t_{d(off)}$	Turn–Off Delay Time			13	23	ns
t_f	Turn–Off Fall Time			4	8	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -2.2\text{ A},$ $V_{GS} = -4.5\text{ V}$		3.7	5.2	nC
Q_{gs}	Gate–Source Charge			1		nC
Q_{gd}	Gate–Drain Charge			1		nC

Drain–Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain–Source Diode Forward Current			-0.8		A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -0.8\text{ A}$ (Note 2)		-0.8	-1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -2.2\text{ A},$ $dI_F/dt = 100\text{ A}/\mu\text{s}$		5.4		nS
Q_{rr}	Diode Reverse Recovery Charge			1.2		nC

Schottky Diode Characteristics

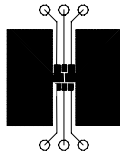
I_R	Reverse Leakage	$V_R = 20\text{ V}$	$T_J = 25^\circ\text{C}$		148	400	μA
			$T_J = 100^\circ\text{C}$		14	20	mA
		$V_R = 10\text{ V}$	$T_J = 25^\circ\text{C}$		55	200	μA
			$T_J = 100^\circ\text{C}$		5.2	10	mA
V_F	Forward Voltage	$I_F = 500\text{ mA}$	$T_J = 25^\circ\text{C}$		0.34	0.4	V
			$T_J = 100^\circ\text{C}$		0.26	0.35	
		$I_F = 1\text{ A}$	$T_J = 25^\circ\text{C}$		0.40	0.45	V
			$T_J = 100^\circ\text{C}$		0.35	0.42	

Electrical Characteristics

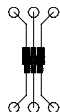
$T_A = 25^\circ\text{C}$ unless otherwise noted

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 130°C/W when mounted on a 0.125 in^2 pad of 2 oz. copper.



b) 140°C/W when mounted on a $.004\text{ in}^2$ pad of 2 oz copper



c) 180°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty Cycle $< 2.0\%$

Typical Characteristics

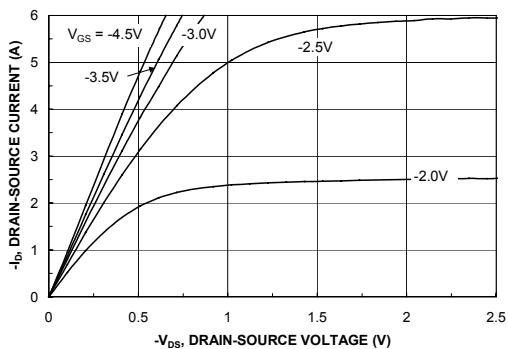


Figure 1. On-Region Characteristics.

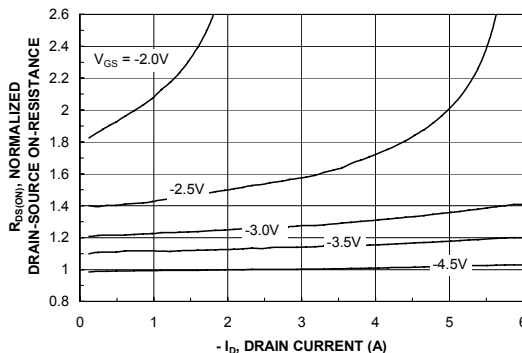


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

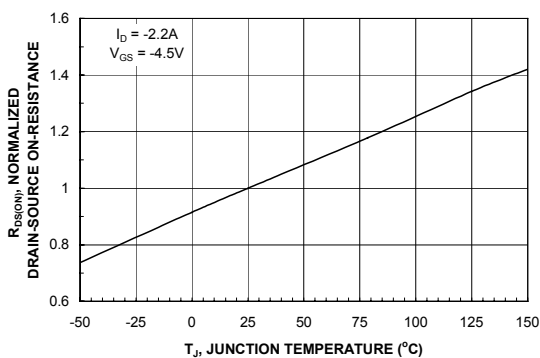


Figure 3. On-Resistance Variation with Temperature.

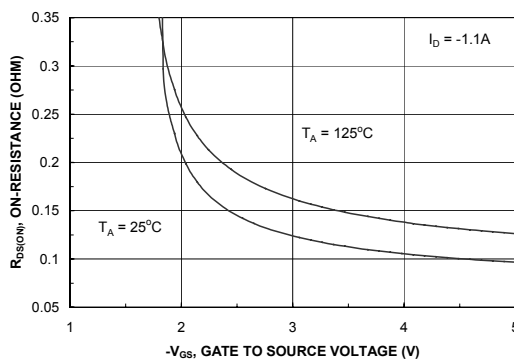


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

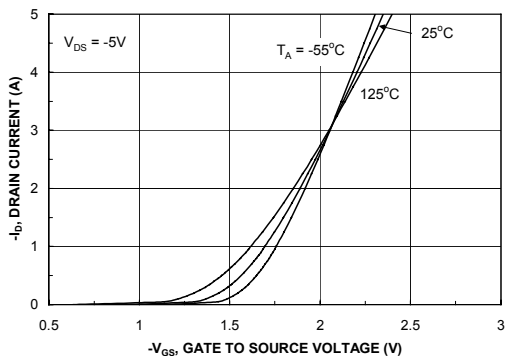


Figure 5. Transfer Characteristics.

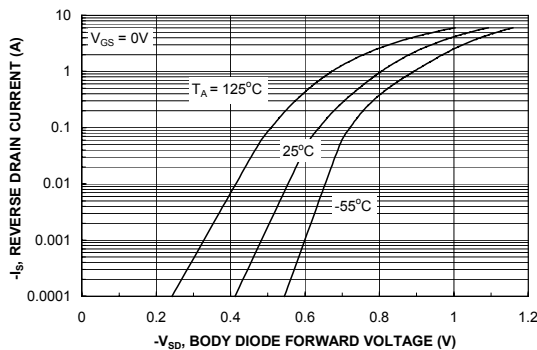


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

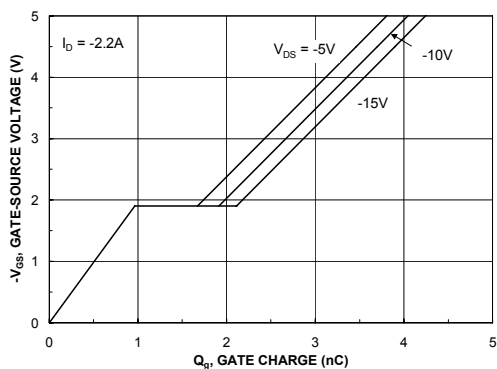


Figure 7. Gate Charge Characteristics.

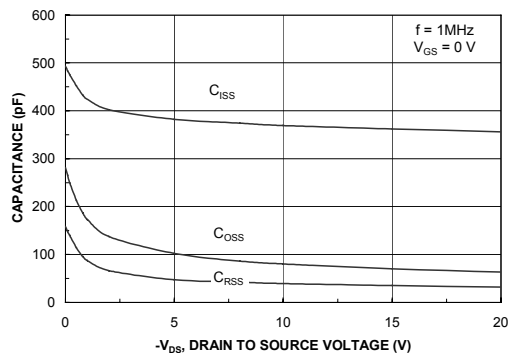


Figure 8. Capacitance Characteristics.

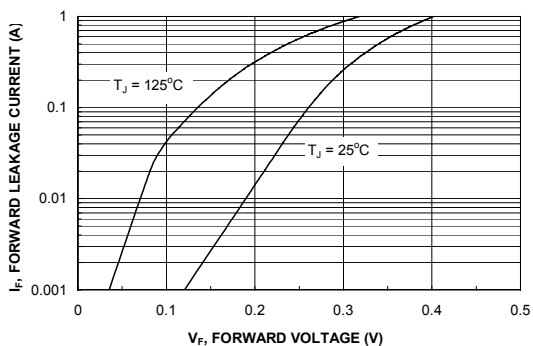


Figure 9. Schottky Diode Forward Voltage.

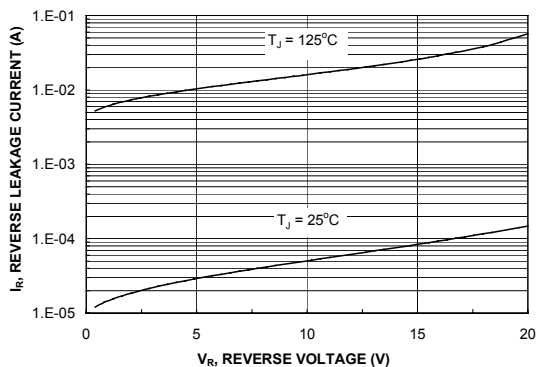


Figure 10. Schottky Diode Reverse Current.

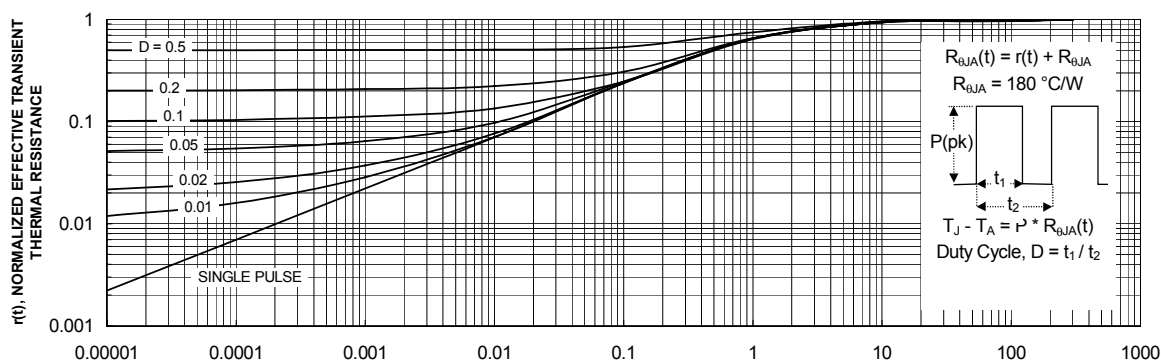


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
 Transient thermal response will change depending on the circuit board design.

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