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FAIRCHILD
SEMICONDUCTOR®

March 2008

FDMC8462

N-Channel Power Trench® MOSFET

40V, 20A, 5.8mΩ

Features

- Max $r_{DS(on)}$ = 5.8mΩ at V_{GS} = 10V, I_D = 13.5A
- Max $r_{DS(on)}$ = 8.0mΩ at V_{GS} = 4.5V, I_D = 11.8A
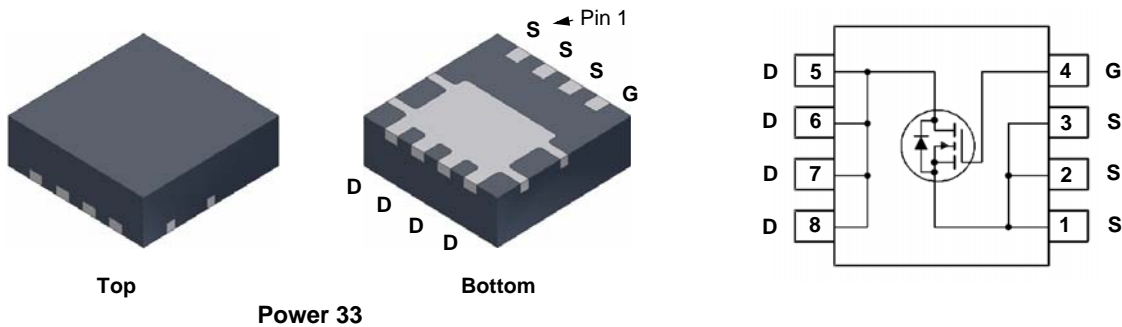- Low Profile - 1mm max in Power 33
- 100% UIL Tested
- RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC - DC Conversion

Top   **Bottom**

Power 33

MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			40	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25°C		20	A
	-Continuous (Silicon limited)	T_C = 25°C		64	
	-Continuous	T_A = 25°C	(Note 1a)	14	
	-Pulsed			50	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	216	mJ
P_D	Power Dissipation	T_C = 25°C		41	W
	Power Dissipation	T_A = 25°C	(Note 1a)	2.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8462	FDMC8462	Power 33	13"	12mm	3000 units

www.fairchildsemi.com

Electrical Characteristics T$_J$ = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV$_{DSS}$	Drain to Source Breakdown Voltage	I$_D$ = 250µA, V$_{GS}$ = 0V	40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I$_D$ = 250µA, referenced to 25°C		31		mV/°C
I$_{DSS}$	Zero Gate Voltage Drain Current	V$_{GS}$ = 0V, V$_{DS}$ = 32V,			1	µA
I$_{GSS}$	Gate to Source Leakage Current	V$_{GS}$ = ±20V, V$_{DS}$ = 0V			±100	nA
On Characteristics						
V$_{GS(th)}$	Gate to Source Threshold Voltage	V$_{GS}$ = V$_{DS}$, I$_D$ = 250µA	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I$_D$ = 250µA, referenced to 25°C		-6.6		mV/°C
r$_{DS(on)}$	Static Drain to Source On Resistance	V$_{GS}$ = 10V, I$_D$ = 13.5A		4.7	5.8	mΩ
		V$_{GS}$ = 4.5V, I$_D$ = 11.8A		6.4	8.0	
		V$_{GS}$ = 10V, I$_D$ = 13.5A, T$_J$ = 125°C		7.1	9.3	
g$_{FS}$	Forward Transconductance	V$_{DD}$ = 5V, I$_D$ = 13.5A		60		S
Dynamic Characteristics						
C$_{iss}$	Input Capacitance	V$_{DS}$ = 20V, V$_{GS}$ = 0V, f = 1MHz		2000	2660	pF
C$_{oss}$	Output Capacitance			545	725	pF
C$_{rss}$	Reverse Transfer Capacitance			80	120	pF
R$_g$	Gate Resistance	f = 1MHz		2.7		Ω
Switching Characteristics						
t$_{d(on)}$	Turn-On Delay Time	V$_{DD}$ = 20V, I$_D$ = 13.5A, V$_{GS}$ = 10V, R$_{GEN}$ = 6Ω		12	21	ns
t$_r$	Rise Time			4	10	ns
t$_{d(off)}$	Turn-Off Delay Time			27	43	ns
t$_f$	Fall Time			3	10	ns
Q$_g$	Total Gate Charge	V$_{GS}$ = 0V to 10V		30	43	nC
Q$_g$	Total Gate Charge	V$_{GS}$ = 0V to 4.5V, V$_{DD}$ = 20V, I$_D$ = 13.5A		15	21	nC
Q$_{gs}$	Gate to Source Charge			6		nC
Q$_{gd}$	Gate to Drain "Miller" Charge			5		nC
Drain-Source Diode Characteristics						
V$_{SD}$	Source to Drain Diode Forward Voltage	V$_{GS}$ = 0V, I$_S$ = 13.5A (Note 2)		0.8	1.3	V
		V$_{GS}$ = 0V, I$_S$ = 1.7A (Note 2)		0.7	1.2	
t$_{rr}$	Reverse Recovery Time	I$_F$ = 13.5A, di/dt = 100A/µs		35	57	ns
Q$_{rr}$	Reverse Recovery Charge			20	32	nC

NOTES:

1. R$_{θJA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R$_{θJC}$ is guaranteed by design while R$_{θCA}$ is determined by the user's board design.
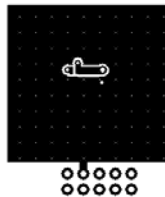
a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300µs, Duty cycle < 2.0%.

3. Starting T$_J$ = 25°C; N-ch: L = 3 mH, I$_{AS}$ = 12A, V$_{DD}$ = 40V, V$_{GS}$ = 10V

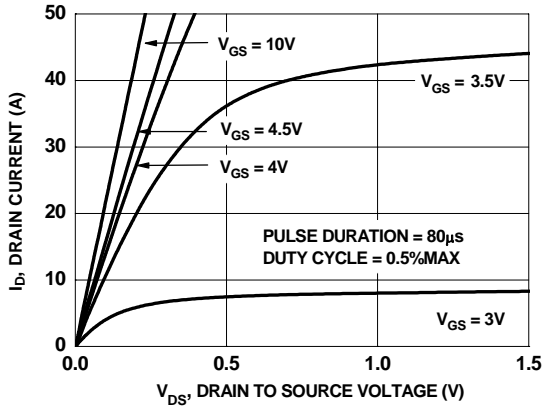## Typical Characteristics T_J = 25°C unless otherwise noted

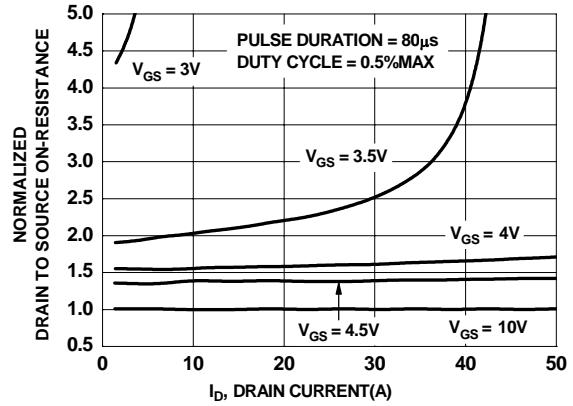Figure 1. On-Region Characteristics

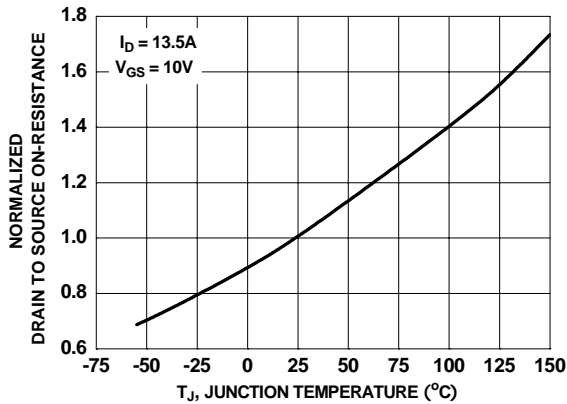Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

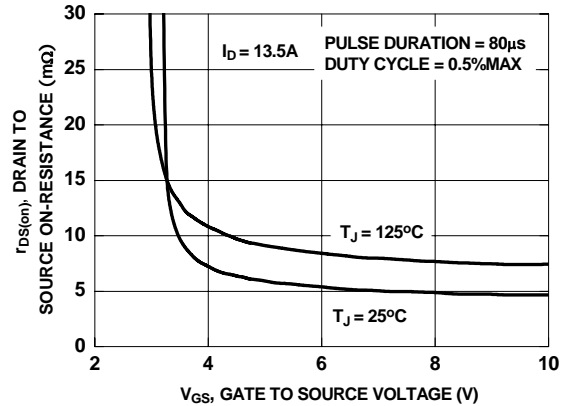Figure 3. Normalized On-Resistance vs Junction Temperature
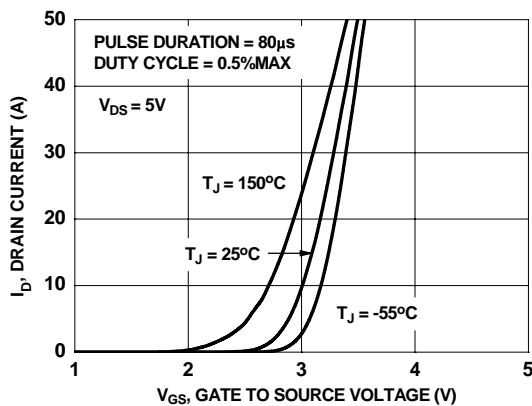

Figure 4. On-Resistance vs Gate to Source Voltage

Figure 5. Transfer Characteristics
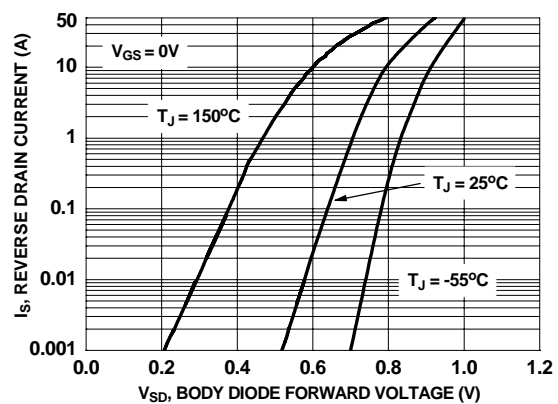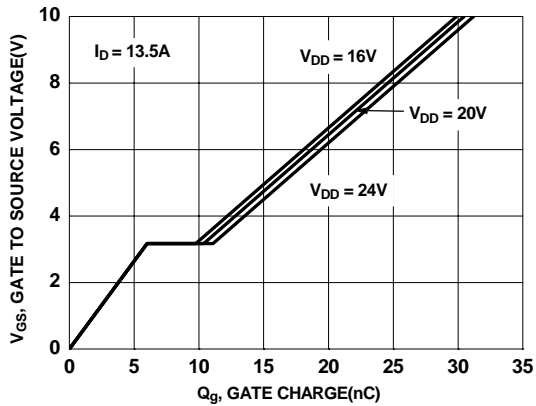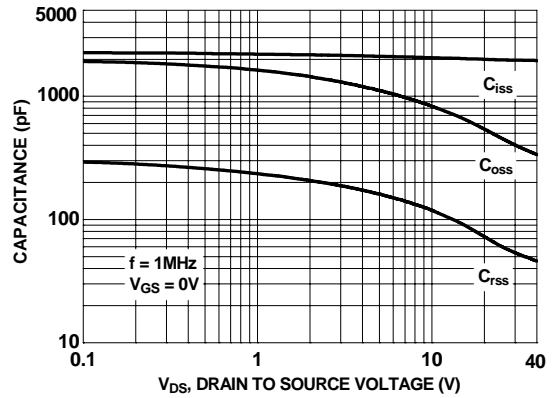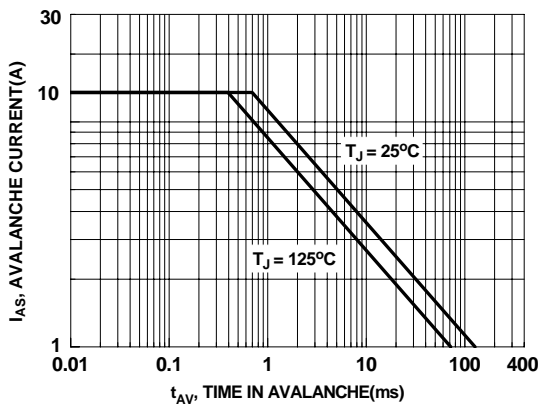

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

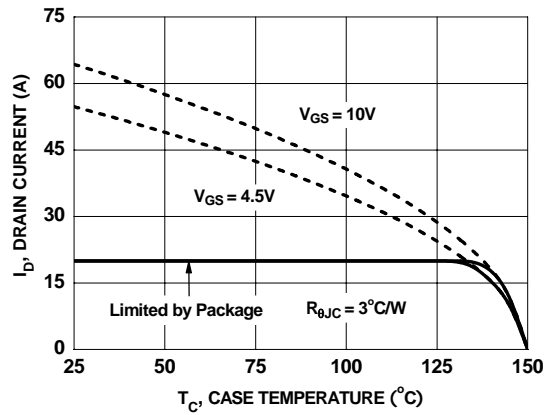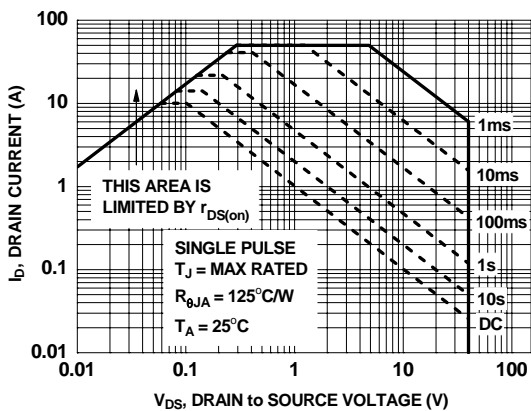**Figure 7. Gate Charge Characteristics**

I_D = 13.5A V_{DD} = 16V, V_{DD} = 20V, V_{DD} = 24V

Figure 8. Capacitance vs Drain to Source Voltage

f = 1MHz, V_{GS} = 0V, C_{iss}, C_{oss}, C_{rss}

Figure 9. Unclamped Inductive Switching Capability

T_J = 25°C, T_J = 125°C

Figure 10. Maximum Continuous Drain Current vs Case Temperature

V_{GS} = 10V, V_{GS} = 4.5V, Limited by Package, $R_{\theta JC}$ = 3°C/W

Figure 11. Forward Bias Safe Operating Area

THIS AREA IS LIMITED BY $r_{DS(on)}$, SINGLE PULSE, T_J = MAX RATED, $R_{\theta JA}$ = 125°C/W, T_A = 25°C, 1ms, 10ms, 100ms, 1s, 10s, DC
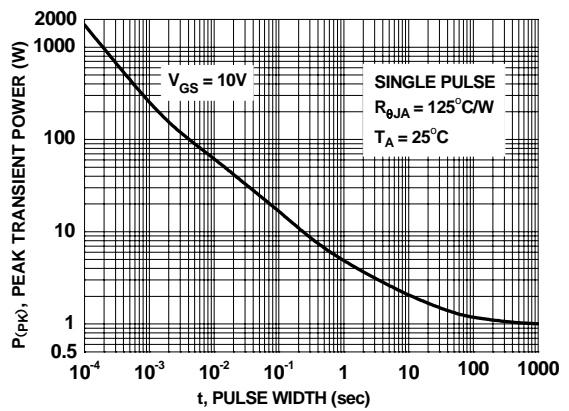
Figure 12. Single Pulse Maximum Power Dissipation

V_{GS} = 10V, SINGLE PULSE, $R_{\theta JA}$ = 125°C/W, T_A = 25°C

Typical Characteristics T_J = 25°C unless otherwise noted

DUTY CYCLE-DESCENDING ORDER

D = 0.5
0.2
0.1
0.05
0.02
0.01

NORMALIZED THERMAL IMPEDANCE, $Z_{\theta JA}$

SINGLE PULSE
$R_{\theta JA}$ = 125°C/W

P_{DM}

t_1

t_2

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JA}$ x $R_{\theta JA}$ + T_A

t, RECTANGULAR PULSE DURATION (sec)
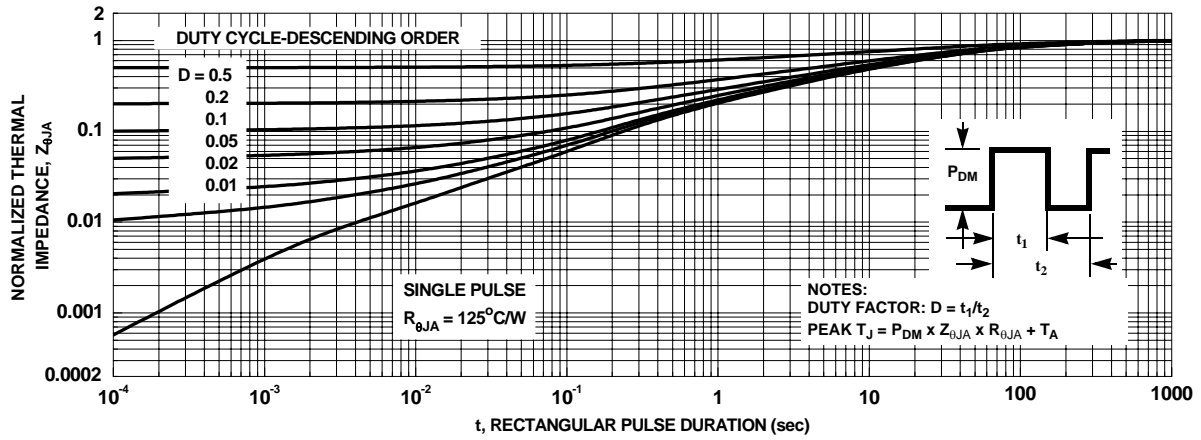
Figure 13. Transient Thermal Response Curve

Dimensional Outline and Pad Layout

3.30±0.10 [A]

PKG C̸L

8   5   [B]

PKG C̸L   3.30±0.10

1   4

SEE
DETAIL A

2.37 MIN

SYM C̸L

(0.45)   8   5

(0.40)   2.15 MIN

PKG C̸L

(0.65)

0.70 MIN

1   4

0.65   0.42 MIN

1.95

LAND PATTERN
RECOMMENDATION

1.95

0.32±0.05   [0.65]

[⊕ 0.10 C A B]   1   4

0.40±0.10

(0.20)

PKG C̸L

2.00±0.10

(0.39)   8   5

(2.27)

(0.52)

[∥ 0.10 C]

1.10
0.90

[⌒ 0.08 C]   0.05
0.00   [C]

0.20±0.025

SEATING
PLANE

DETAIL A
SCALE: 2X

NOTES: UNLESS OTHERWISE SPECIFIED

A)   PACKAGE STANDARD REFERENCE:
       JEDEC MO−240, ISSUE A, VAR. BA,
       DATED OCTOBER 2002.
B)   ALL DIMENSIONS ARE IN MILLIMETERS.
C)   DIMENSIONS DO NOT INCLUDE BURRS
       OR MOLD FLASH. MOLD FLASH OR
       BURRS DOES NOT EXCEED 0.10MM.
D)   DIMENSIONING AND TOLERANCING PER
       ASME Y14.5M−1994.
E)   DRAWING FILE NAME: PQFN08BREV1

PQFN08BREV1

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Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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