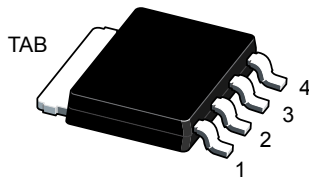
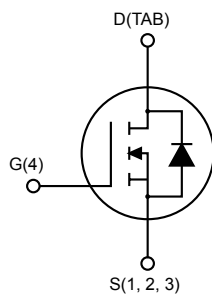


## Automotive-grade N-channel 40 V, 1.2 mΩ typ., 100 A STripFET™ F7 Power MOSFET in a LFPAK 5x6 package



LFPAK 5x6




G4S123DTAB\_LFPAK



### Features

Order code	$V_{DS}$	$R_{DS(on)}$ max	$I_D$
STK224N4F7AG	40 V	1.5 mΩ	100 A

- AEC-Q101 qualified 
- Among the lowest  $R_{DS(on)}$  on the market
- Excellent FoM (figure of merit)
- Low  $C_{rSS}/C_{iSS}$  ratio for EMI immunity
- High avalanche ruggedness

### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

#### Product status

STK224N4F7AG

#### Product summary

Order code	STK224N4F7AG
Marking	224N4F7
Package	LFPAK 5x6
Packing	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	40	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	100	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	100	A
$I_{DM}^{(2)}$	Drain current (pulsed)	400	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
$I_{AV}$	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	56	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$ , $I_D = I_{AV}$ , $V_{DD} = 25\text{ V}$ )	470	mJ
$T_j$	Operating junction temperature range	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature range		

1. Drain current is limited by package, the current capability of the silicon is 224 A at 25 °C.
2. Pulse width limited by safe operating area

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb.	31.3	$^\circ\text{C/W}$
$R_{thj-case}$	Thermal resistance junction-case.	1.0	$^\circ\text{C/W}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$ .

## 2 Electrical characteristics

( $T_C = 25\text{ }^\circ\text{C}$  unless otherwise specified)

**Table 3. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	40			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 40\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 50\text{ A}$		1.2	1.5	m $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	4060	-	pF
$C_{oss}$	Output capacitance		-	1100	-	pF
$C_{rss}$	Reverse transfer capacitance		-	300	-	pF
$Q_g$	Total gate charge	$V_{DD} = 20\text{ V}$ , $I_D = 100\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	50	-	nC
$Q_{gs}$	Gate-source charge		-	23	-	nC
$Q_{gd}$	Gate-drain charge		-	9.8	-	nC

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 20\text{ V}$ , $I_D = 50\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	25	-	ns
$t_r$	Rise time		-	20	-	ns
$t_{d(off)}$	Turn-off delay time		-	48	-	ns
$t_f$	Fall time		-	31	-	ns

**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 100\text{ A}$ , $V_{GS} = 0\text{ V}$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_D = 100\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	41		ns
$Q_{rr}$	Reverse recovery charge		-	32		nC
$I_{RRM}$	Reverse recovery current		-	1.6		A

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics curves

Figure 1. Safe operating area

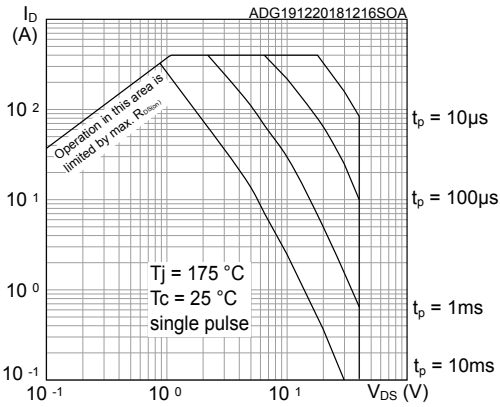


Figure 2. Thermal impedance

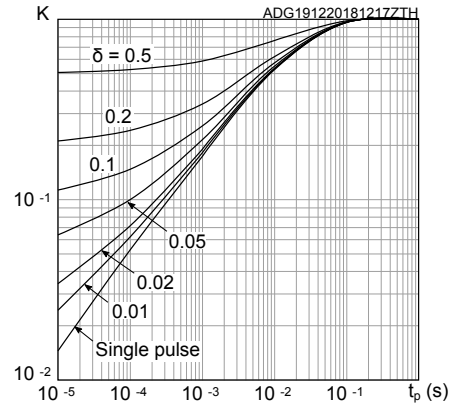


Figure 3. Output characteristics

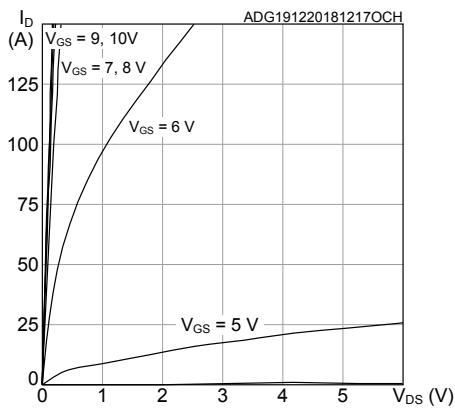


Figure 4. Transfer characteristics

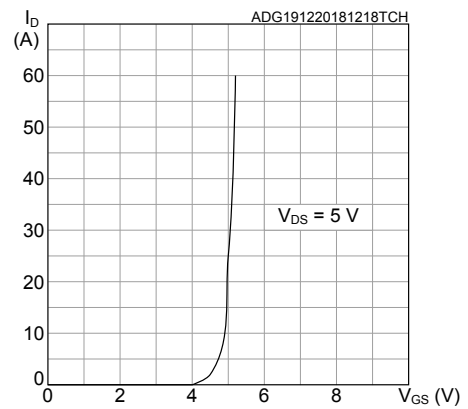


Figure 5. Static drain-source on resistance

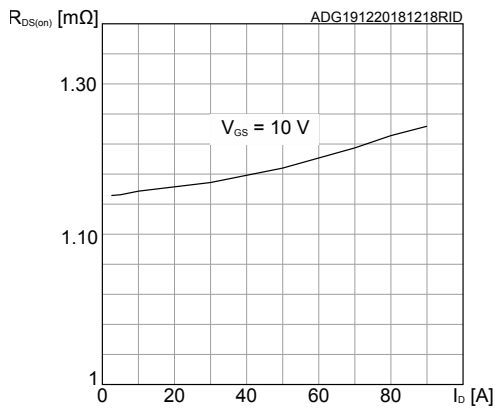


Figure 6. Gate charge vs gate-source voltage

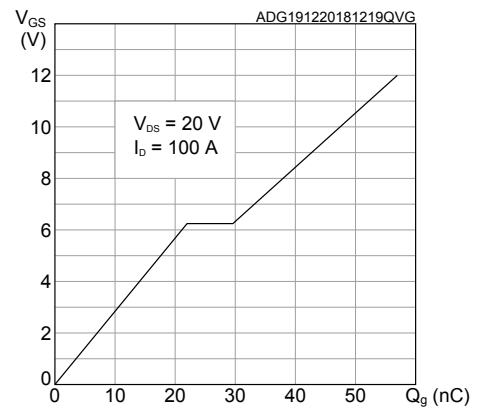


Figure 7. Capacitance variations

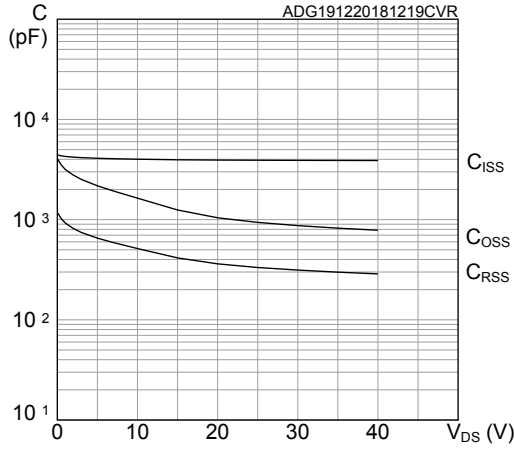


Figure 8. Normalized gate threshold voltage vs temperature

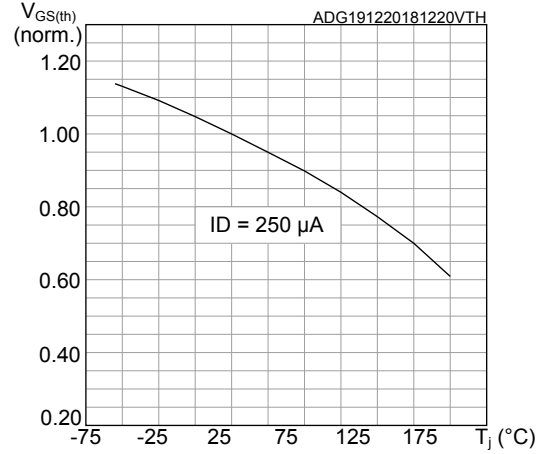


Figure 9. Normalized on resistance vs temperature

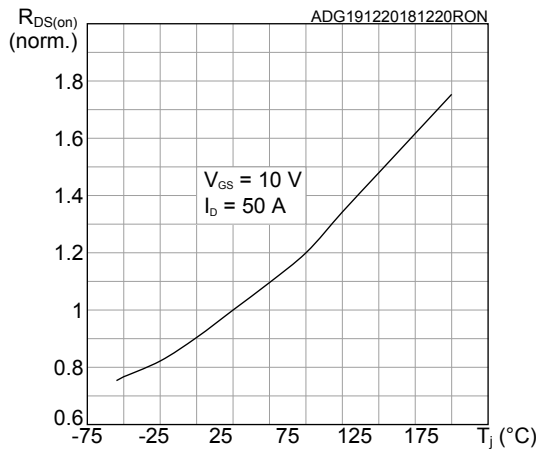


Figure 10. Source-drain diode forward characteristic

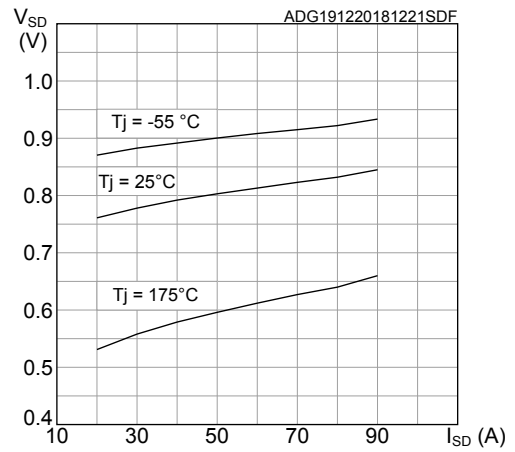
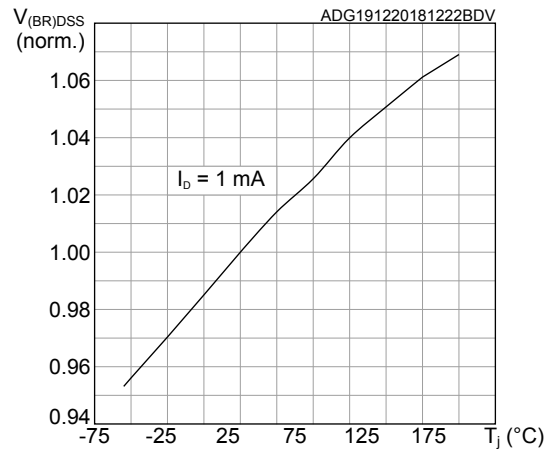
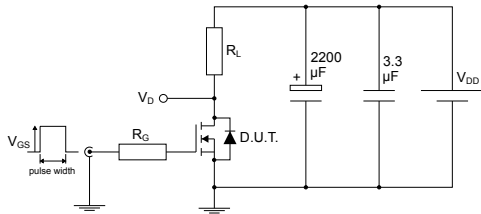


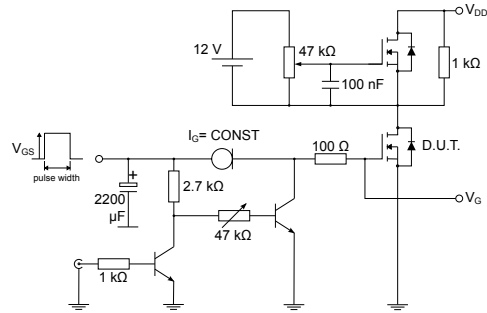
Figure 11. Normalized  $V_{(BR)DSS}$  vs temperature



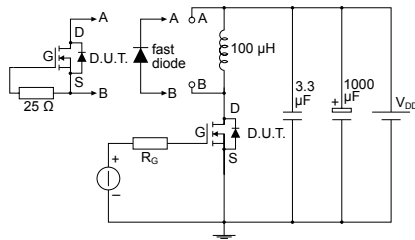
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


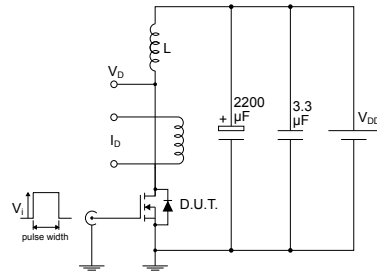
AM01468v1

**Figure 13. Test circuit for gate charge behavior**


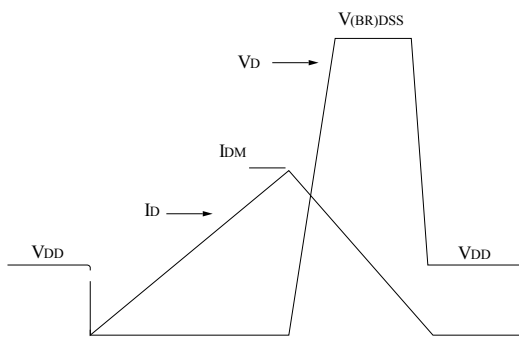
AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**


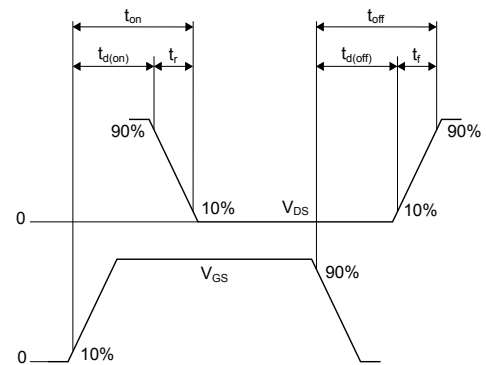
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**Figure 15. Unclamped inductive load test circuit**


AM01471v1

**Figure 16. Unclamped inductive waveform**


AM01472v1

**Figure 17. Switching time waveform**


AM01473v1

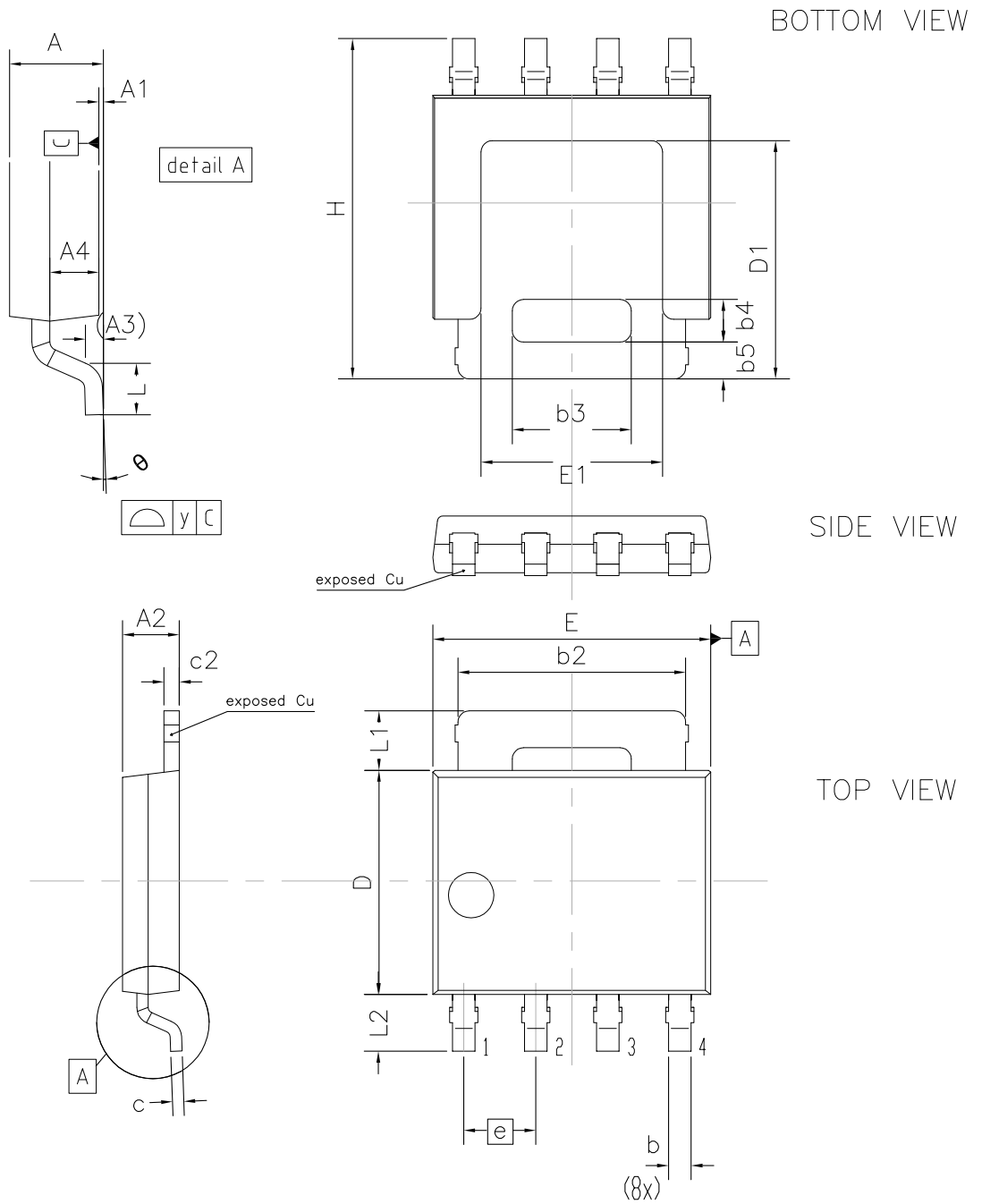
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 LFPACK 5x6 package information

Figure 18. LFPACK 5x6 package outline



00299525\_A

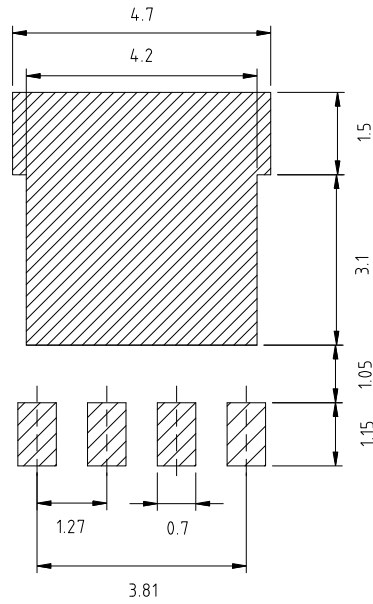


**Table 7. LFPACK 5x6 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	1.01		1.20
A1	0.00		0.15
A2	0.95		1.10
A3		0.25	
A4	0.50	0.55	0.65
b	0.35		0.50
b2	3.62		4.41
b3	2.0		2.20
b4	0.70		0.90
b5			0.7
c	0.19	0.20 <sup>(1)</sup>	0.25
c2	0.24		0.30
D	3.80		4.10
D1	3.80	4.00	4.20
E	4.8		5.0
E1	3.1		3.3
e		1.27	
H	5.8		6.2
L	0.40		0.85
L1	0.80		1.30
L2	0.80		1.3
w		0.25	
y		0.10	
θ	0°		8°

1. Dimension without plating

Figure 19. LFPACK 5x6 recommended footprint



00299525\_FP\_A

## Revision history

**Table 8. Document revision history**

Date	Revision	Changes
09-Apr-2018	1	First release.
14-Jan-2019	2	Updated title in cover page, <a href="#">Section 1 Electrical ratings</a> and <a href="#">Section 2 Electrical characteristics</a> . Added <a href="#">Section 2.1 Electrical characteristics curves</a> Minor text changes.

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