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NJD2873

Power Transistors

NPN Silicon DPAK For Surface Mount Applications

Designed for high-gain audio amplifier applications.

Features

- High DC Current Gain
- Low Collector–Emitter Saturation Voltage
- High Current–Gain – Bandwidth Product
- Epoxy Meets UL 94 V–0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q101 Qualified and PPAP Capable
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Base Voltage	V_{CB}	50	Vdc
Collector–Emitter Voltage	V_{CEO}	50	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current – Continuous	I_C	2	Adc
Collector Current – Peak	I_{CM}	3	Adc
Base Current	I_B	0.4	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	15 0.1	W W/ $^\circ\text{C}$
Total Device Dissipation @ $T_A = 25^\circ\text{C}^*$ Derate above 25°C	P_D	1.68 0.011	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +175	$^\circ\text{C}$
ESD – Human Body Model	HBM	3B	V
ESD – Machine Model	MM	C	V

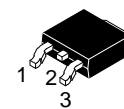
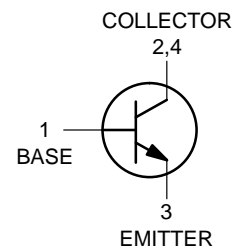
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



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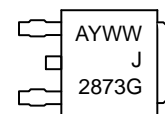
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SILICON POWER TRANSISTORS 2 AMPERES 50 VOLTS 15 WATTS



DPAK
CASE 369C
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
G = Pb–Free Device

ORDERING INFORMATION

Device	Package	Shipping†
NJD2873T4G	DPAK (Pb–Free)	2,500 Units / Reel
NJVNJD2873T4G	DPAK (Pb–Free)	2,500 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1)	$R_{\theta JC}$ $R_{\theta JA}$	10 89.3	°C/W

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (Note 2) ($I_C = 10 \text{ mAdc}$, $I_B = 0$)	$V_{CEO(sus)}$	50	-	Vdc
Collector Cutoff Current ($V_{CB} = 50 \text{ Vdc}$, $I_E = 0$)	I_{CBO}	-	100	nAdc
Emitter Cutoff Current ($V_{BE} = 5 \text{ Vdc}$, $I_C = 0$)	I_{EBO}	-	100	nAdc

ON CHARACTERISTICS

DC Current Gain (Note 2) ($I_C = 0.5 \text{ A}$, $V_{CE} = 2 \text{ V}$) ($I_C = 2 \text{ Adc}$, $V_{CE} = 2 \text{ Vdc}$) ($I_C = 0.75 \text{ Adc}$, $V_{CE} = 1.6 \text{ Vdc}$, $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$)	h_{FE}	120 40 80	360 -	-
Collector-Emitter Saturation Voltage (Note 2) ($I_C = 1 \text{ A}$, $I_B = 0.05 \text{ A}$)	$V_{CE(sat)}$	-	0.3	Vdc
Base-Emitter Saturation Voltage (Note 2) ($I_C = 1 \text{ A}$, $I_B = 0.05 \text{ Adc}$)	$V_{BE(sat)}$	-	1.2	Vdc
Base-Emitter On Voltage (Note 2) ($I_C = 1 \text{ Adc}$, $V_{CE} = 2 \text{ Vdc}$) ($I_C = 0.75 \text{ Adc}$, $V_{CE} = 1.6 \text{ Vdc}$, $-40^\circ\text{C} \leq T_J \leq 150^\circ\text{C}$)	$V_{BE(on)}$	- -	1.2 0.95	Vdc

DYNAMIC CHARACTERISTICS

Current-Gain - Bandwidth Product (Note 3) ($I_C = 100 \text{ mAdc}$, $V_{CE} = 10 \text{ Vdc}$, $f_{test} = 10 \text{ MHz}$)	f_T	65	-	MHz
Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$)	C_{ob}	-	80	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width = 300 μs , Duty Cycle \approx 2%.

3. $f_T = |h_{fe}| \cdot f_{test}$

TYPICAL CHARACTERISTICS

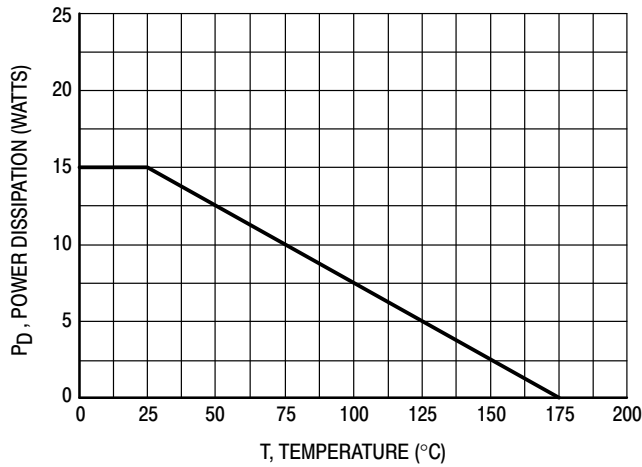


Figure 1. Power Derating

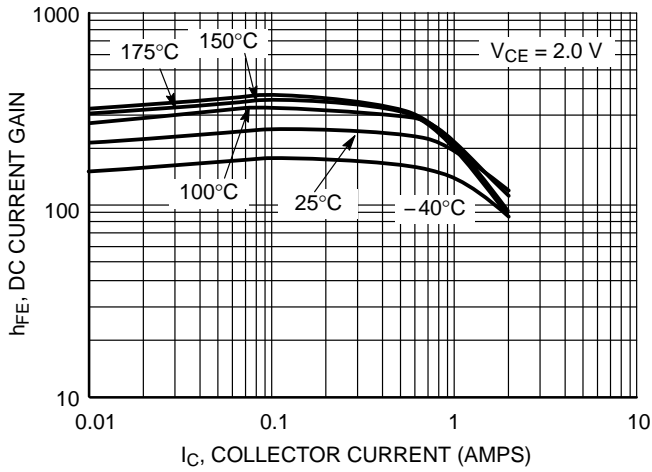


Figure 2. DC Current Gain

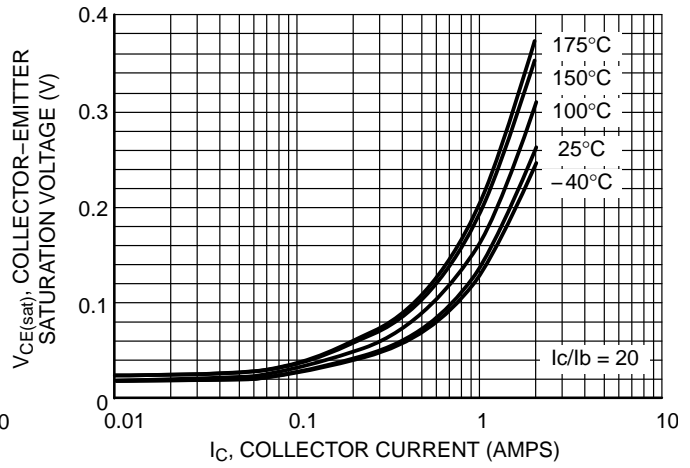


Figure 3. Collector-Emitter Saturation Voltage

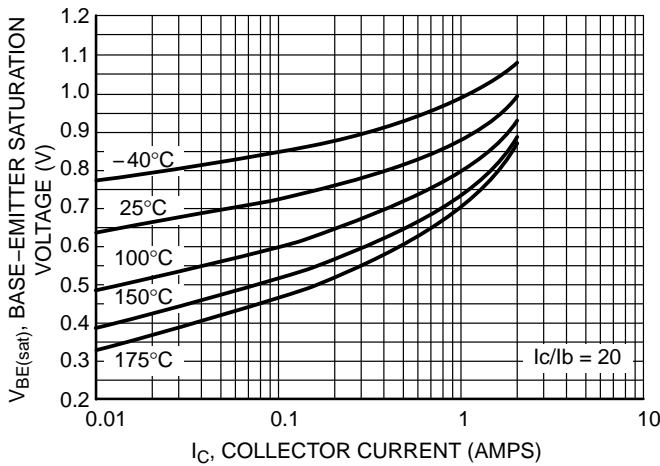


Figure 4. Base-Emitter Saturation Voltage

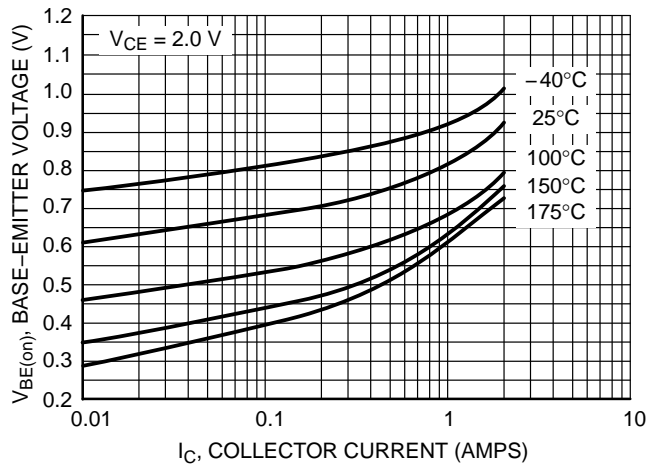


Figure 5. Base-Emitter Voltage

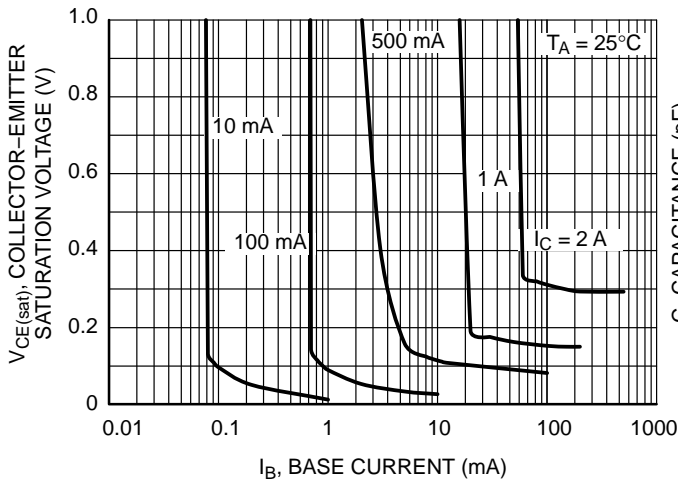


Figure 6. Saturation Region

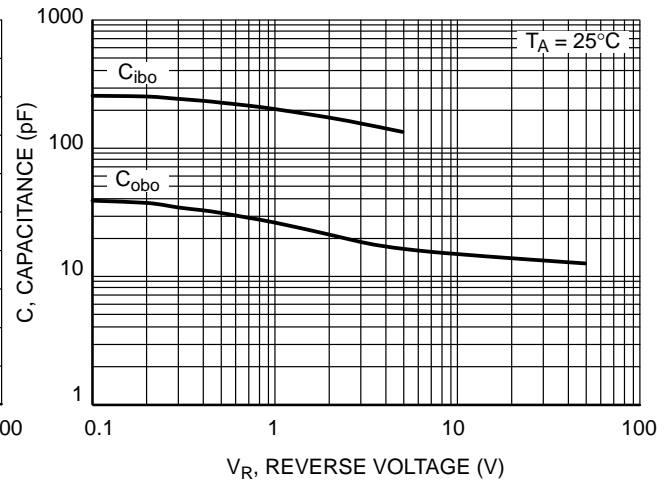


Figure 7. Capacitance

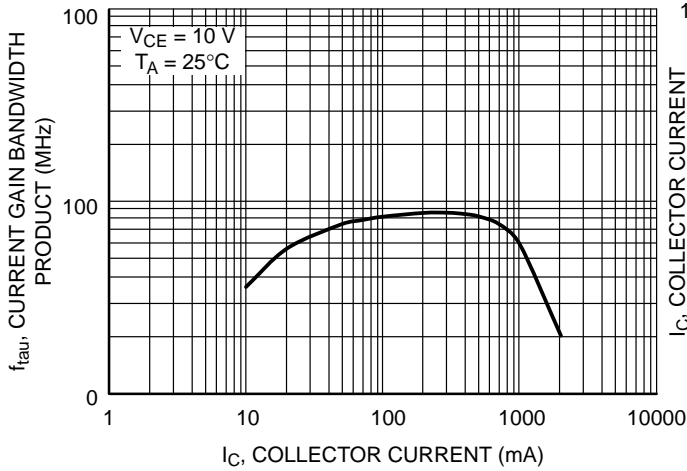


Figure 8. Saturation Region

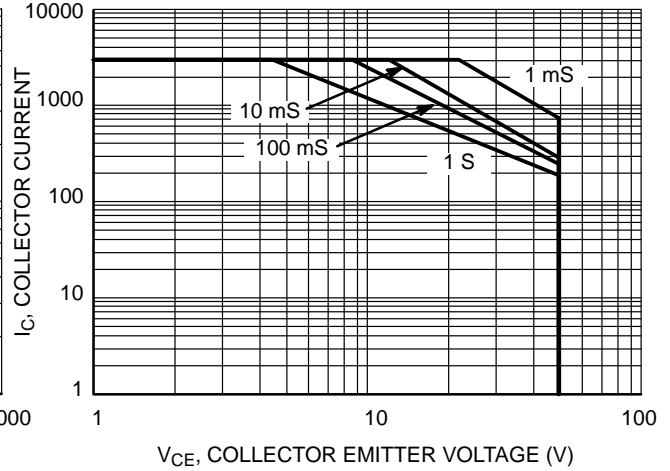


Figure 9. Capacitance

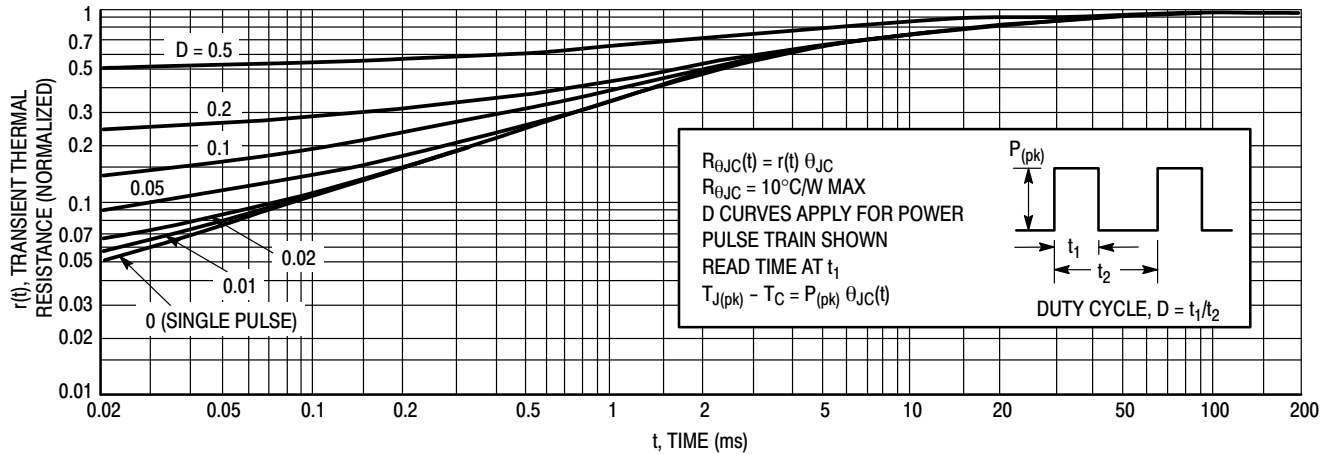


Figure 10. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

DPAK (SINGLE GAUGE) CASE 369C ISSUE F

DATE 21 JUL 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

GENERIC MARKING DIAGRAM*



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

- | | | | | |
|--|--|---|---|--|
| <p>STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN</p> | <p>STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE</p> | <p>STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE</p> |
| <p>STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2</p> | <p>STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR</p> | <p>STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE</p> | <p>STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE</p> | <p>STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE</p> |

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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