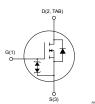


Datasheet

# N-channel 600 V, 286 m $\Omega$ typ., 12 A MDmesh DM6 Power MOSFET in a DPAK package





#### **Features**

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD15N60DM6	600 V	338 mΩ	12 A

- · Fast-recovery body diode
- Lower R<sub>DS(on)</sub> per area vs previous generation
- · Low gate charge, input capacitance and resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- · Zener-protected

#### **Applications**

· Switching applications

#### **Description**

lectronics sales office

This high-voltage N-channel Power MOSFET is part of the MDmesh DM6 fast-recovery diode series. Compared with the previous MDmesh fast generation, DM6 combines very low recovery charge ( $Q_{rr}$ ), recovery time ( $t_{rr}$ ) and excellent improvement in  $R_{DS(on)}$  per area with one of the most effective switching behaviors available in the market for the most demanding high-efficiency bridge topologies and ZVS phase-shift converters.



Product status
STD15N60DM6

Product summary			
Order code	STD15N60DM6		
Marking	15N60DM6		
Package	DPAK		
Packing	Tape and reel		



# 1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	±25	V
1_	Drain current (continuous) at T <sub>C</sub> = 25 °C	12	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	7.3	_ A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	32	А
P <sub>TOT</sub>	Total power dissipation at T <sub>C</sub> = 25 °C	110	W
I <sub>AR</sub> (2)	Avalanche current, repetitive or not repetitive	3	Α
E <sub>AS</sub> (3)	Single pulse avalanche energy	240	mJ
dv/dt (4)	Peak diode recovery voltage slope	100	V/ns
di/dt <sup>(4)</sup>	Peak diode recovery current slope	1000	A/µs
dv/dt (5)	MOSFET dv/dt ruggedness	100	V/ns
T <sub>stg</sub>	Storage temperature range	-55 to 150	°C
TJ	Operating junction temperature range	-55 to 150	

- 1. Pulse width is limited by safe operating area.
- 2. Pulse width limited by  $T_J$  max.
- 3. Starting  $T_J = 25$  °C,  $I_D = I_{AR}$ ,  $V_{DD} = 50$  V.
- 4.  $I_{SD} \le 12 \text{ A}$ ,  $V_{DS \text{ (peak)}} < V_{\text{(BR)DSS}}$ ,  $V_{DD} = 400 \text{ V}$ .
- 5.  $V_{DS} \le 480 \text{ V}$ .

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	1.14	°C/W
R <sub>thj-pcb</sub> <sup>(1)</sup>	Thermal resistance junction-pcb	50	C/VV

1. When mounted on an 1-inch<sup>2</sup> FR-4, 2 Oz copper board.

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## 2 Electrical characteristics

(T<sub>C</sub> = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit	
$V_{(BR)DSS}$	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1 mA	600			V	
I	Zana mata walta na duala awana	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 600 V			1		
I <sub>DSS</sub>	Zero gate voltage drain current	$V_{GS}$ = 0 V, $V_{DS}$ = 600 V, $T_{C}$ = 125 °C <sup>(1)</sup>			100	μΑ	
I <sub>GSS</sub>	Gate-body leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±25 V			±5	μA	
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_{D} = 250 \mu A$	3.25	4	4.75	V	
R <sub>DS(on)</sub>	Static drain-source on-resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 6 A		286	338	mΩ	

<sup>1.</sup> Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter Test conditions		Min.	Тур.	Max.	Unit
C <sub>iss</sub>	Input capacitance		-	607	-	
C <sub>oss</sub>	Output capacitance	$V_{GS} = 100 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0 \text{ V}$	-	40	-	pF
C <sub>rss</sub>	Reverse transfer capacitance		-	4	-	
C <sub>oss eq.</sub> <sup>(1)</sup>	Equivalent output capacitance	V <sub>DS</sub> = 0 to 480 V, V <sub>GS</sub> = 0 V	-	100	-	pF
R <sub>G</sub>	Intrinsic gate resistance	f = 1 MHz open drain	-	5.7	-	Ω
Qg	Total gate charge	V <sub>DD</sub> = 480 V, I <sub>D</sub> = 12 A, V <sub>GS</sub> = 0 to 10 V	-	15.3	-	
Q <sub>gs</sub>	Gate-source charge	(see Figure 14. Test circuit for gate		4.1	-	nC
Q <sub>gd</sub>	Gate-drain charge	charge behavior)	-	7.7	-	

<sup>1.</sup>  $C_{\text{oss eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{\text{oss}}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 300 V, I <sub>D</sub> = 6 A,	-	8.8	-	
t <sub>r</sub>	Rise time	$R_G = 4.7 \Omega$ , $V_{GS} = 10 V$	-	7.4	-	
t <sub>d(off)</sub>	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and	-	29.2	-	ns
t <sub>f</sub>	Fall time	Figure 18. Switching time waveform)	-	7.2	-	

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Table 6. Source-drain diode

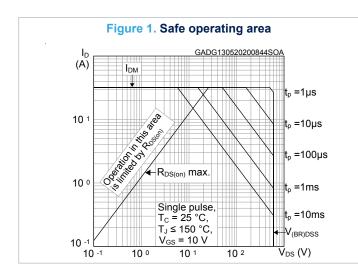
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain current		-		12	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)		-		32	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 12 A	-		1.6	V
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 12 A, di/dt = 100 A/μs,	-	85		ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> = 60 V	-	0.268		μC
I <sub>RRM</sub>	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	6.3		Α
t <sub>rr</sub>	Reverse recovery time	I <sub>SD</sub> = 12 A, di/dt = 100 A/μs,	-	147		ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DD</sub> = 60 V, T <sub>J</sub> = 150 °C	-	0.661		μC
I <sub>RRM</sub>	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9		Α

<sup>1.</sup> Pulse width is limited by safe operating area.

<sup>2.</sup> Pulse test: pulse duration = 300  $\mu$ s, duty cycle 1.5%.



#### 2.1 Electrical characteristics (curves)



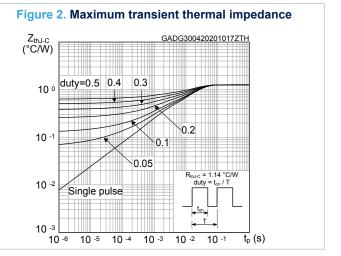


Figure 3. Typical output characteristics

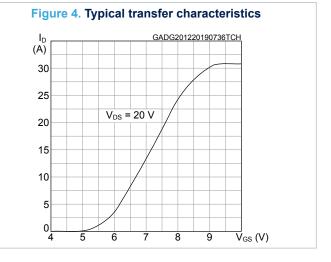
(A)

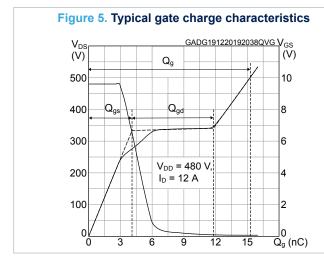
(B)

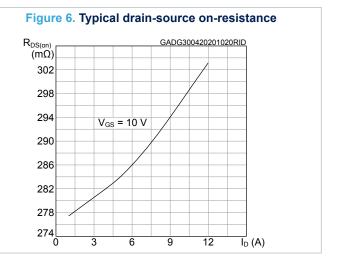
(B)

(CA)

(CA







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10 1

10 º

10 0

f = 1 MHz

10 ¹

C GADG201220190738CVR 10 3 Clss

10 <sup>2</sup>

Coss

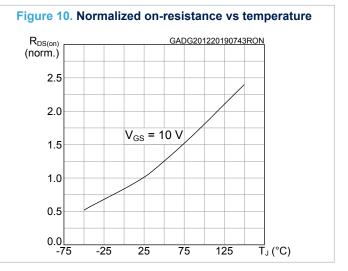
C<sub>RSS</sub>

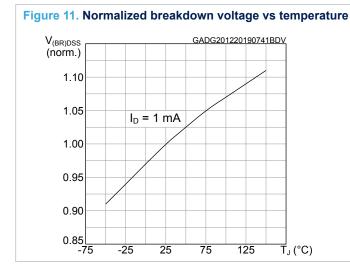
 $\overline{V}_{DS}\left(V\right)$ 

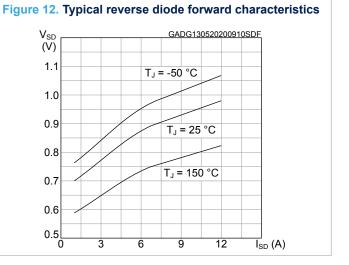
Figure 8. Typical output capacitance stored energy

Eoss (μJ)
6
5
4
3
2
1
0
100 200 300 400 500 600 V<sub>DS</sub> (V)

Figure 9. Normalized gate threshold vs temperature  $V_{GS(th)}$  (norm.) GADG201220190743VTH 1.1 1.0 0.9  $I_D=250~\mu A$  0.8 0.7 0.6 -75 -25 25 75 125  $T_J$  (°C)







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### 3 Test circuits

Figure 13. Test circuit for resistive load switching times

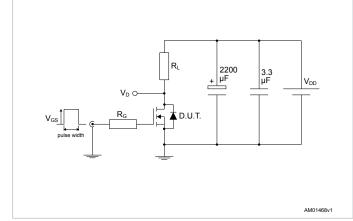


Figure 14. Test circuit for gate charge behavior

V<sub>GS</sub>

Pulse width

2.7 kΩ

47 kΩ

AMD(469+10

Figure 15. Test circuit for inductive load switching and diode recovery times

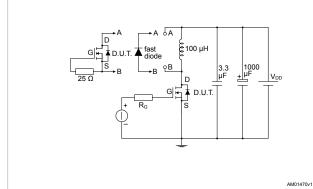


Figure 16. Unclamped inductive load test circuit

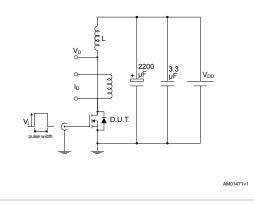


Figure 17. Unclamped inductive waveform

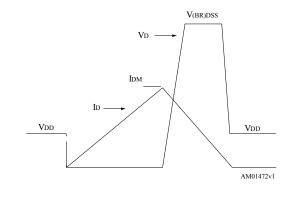
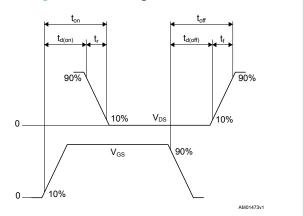


Figure 18. Switching time waveform



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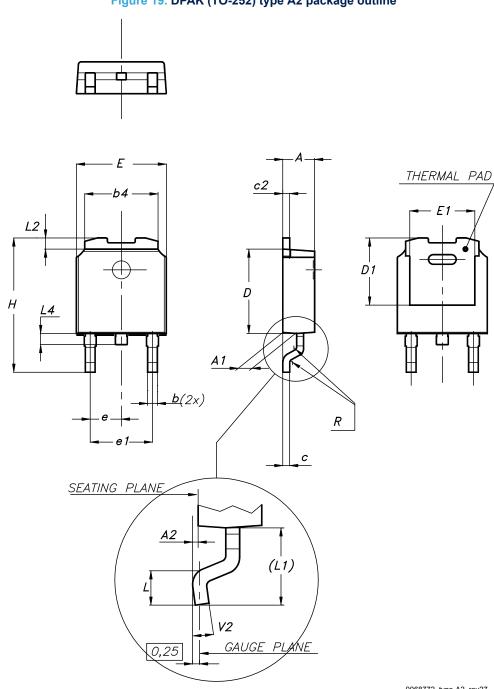


# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type A2 package information

Figure 19. DPAK (TO-252) type A2 package outline



0068772\_type-A2\_rev27

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Table 7. DPAK (TO-252) type A2 mechanical data

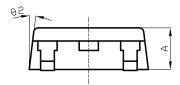
Dim.		mm	
DIM.	Min.	Тур.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
Е	6.40		6.60
E1	5.10	5.20	5.30
е	2.159	2.286	2.413
e1	4.445	4.572	4.699
Н	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

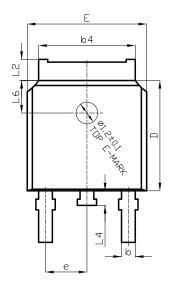
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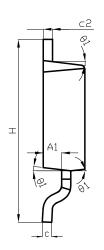


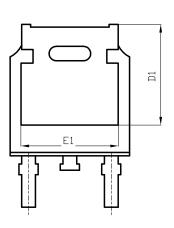
# 4.2 DPAK (TO-252) type C2 package information

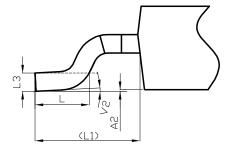
Figure 20. DPAK (TO-252) type C2 package outline











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Table 8. DPAK (TO-252) type C2 mechanical data

Dim.		mm	
Dilli.	Min.	Тур.	Max.
А	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
С	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
Е	6.50	6.60	6.70
E1	5.20		5.50
е	2.186	2.286	2.386
Н	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

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6.3 NIM 8: 1.5 4,572 = =

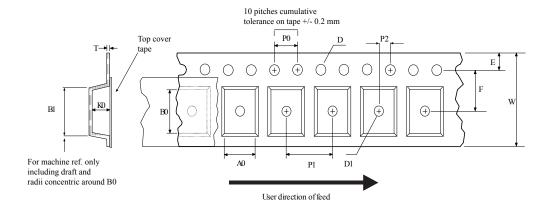
Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)

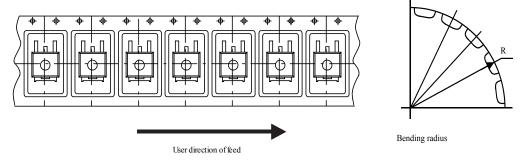
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# 4.3 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



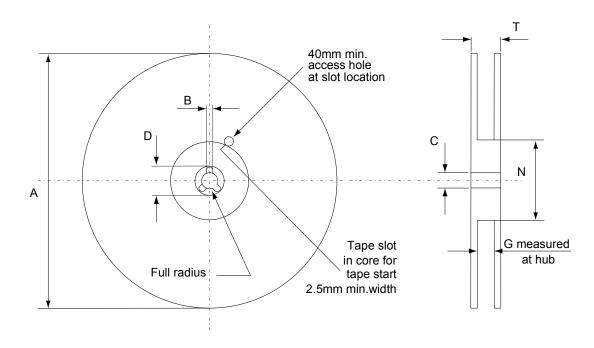


AM08852v1

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Figure 23. DPAK (TO-252) reel outline



AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

Таре			Reel		
Dim.	mm		Dim.		mm
Dim.	Min.	Max.	Dilli.	Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Bas	e qty.	2500
P1	7.9	8.1	Bull	k qty.	2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

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# **Revision history**

Table 10. Document revision history

Date	Revision	Changes
19-May-2020	1	First release.

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