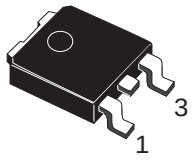
STD16NE06L

N-CHANNEL 60V - 0.06 Ω - 16A DPAK
STripFET™ POWER MOSFET

TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD16NE6L	60 V	<0.07 Ω	16 A

- TYPICAL $R_{DS}(on)$ = 0.06 Ω
- AVALANCHE RUGGED TECHNOLOGY
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175 ºC OPERATING TEMPERATURE
- LOW THRESHOLD DRIVE
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX “T4")

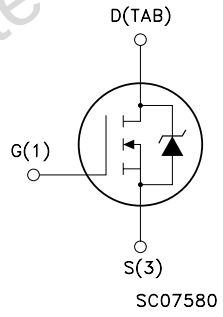


DPAK
TO-252
(Suffix “T4”)

DESCRIPTION

This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

INTERNAL SCHEMATIC DIAGRAM



APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RALAY DRIVERS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	16	A
I_D	Drain Current (continuous) at T_C = 100°C	11	A
I_{DM}(•)	Drain Current (pulsed)	64	A
P_{tot}	Total Dissipation at T_C = 25°C	40	W
	Derating Factor	0.3	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	60	mJ
T_{stg}	Storage Temperature	-55 to 175	°C
T_j	Operating Junction Temperature		

(•) Pulse width limited by safe operating area

(1) I_{SD} ≤16A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ T_{JMAX}
(2) Starting T_j = 25 ºC, I_D = 8A, V_{DD}= 50V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	3.75	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	100	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating T_C = 125°C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20 V			±100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS} I_D = 250 µA	1	1.7	2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10 V I_D = 8 A V_{GS} = 5 V I_D = 8 A		0.06 0.07	0.070 0.085	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (*)	Forward Transconductance	V_{DS}>$I_{D(on)}$x$R_{DS(on)max}$ I_D=8A		9		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		800 125 50		pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD} = 30 V I_D = 10 A R_G = 4.7 Ω V_{GS} = 5 V (Resistive Load, Figure 3)		20 45		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 48 V I_D = 20 A V_{GS}= 5V		14 8 4	20	nC nC nC

SWITCHING OFF

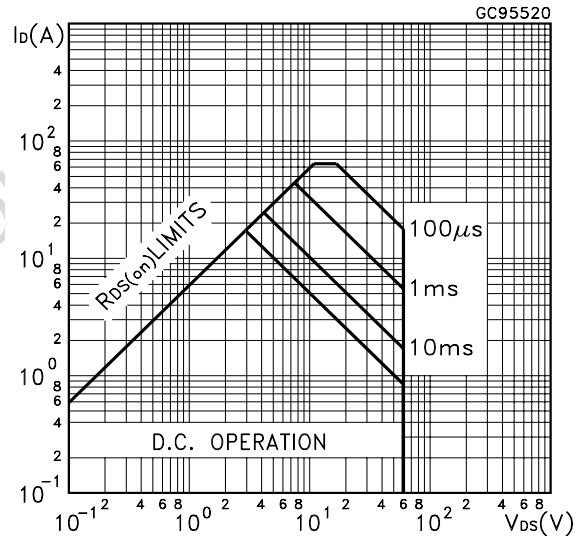
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	V_{clamp} = 48 V I_D = 20 A R_G = 4.7Ω, V_{GS} = 5 V (Inductive Load, Figure 5)		10 25 42		ns ns ns

SOURCE DRAIN DIODE

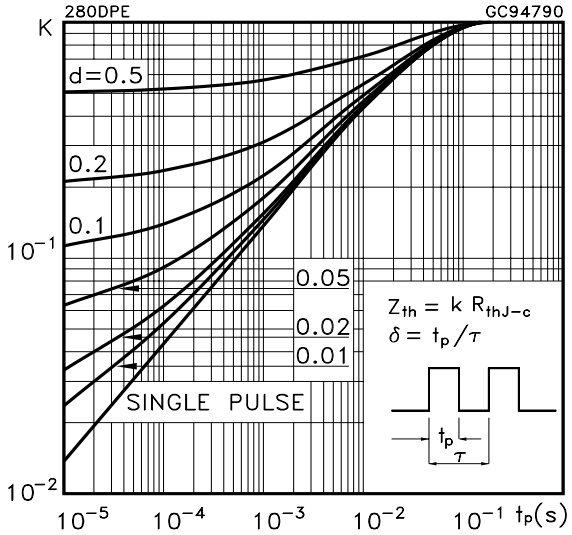
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (•)	Source-drain Current Source-drain Current (pulsed)				20 80	A A
V_{SD} (*)	Forward On Voltage	I_{SD} = 16 A V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 20 A di/dt = 100A/µs V_{DD} = 40 V T_j = 150°C (see test circuit, Figure 5)		65 130 4		ns nC A

(*)Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
(•)Pulse width limited by safe operating area.

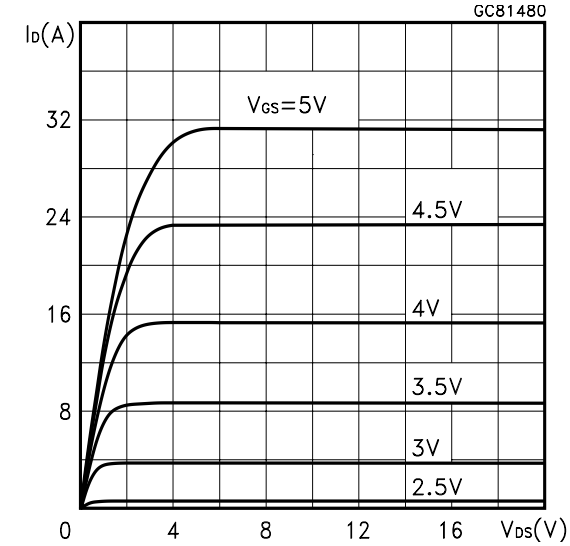
Safe Operating Area



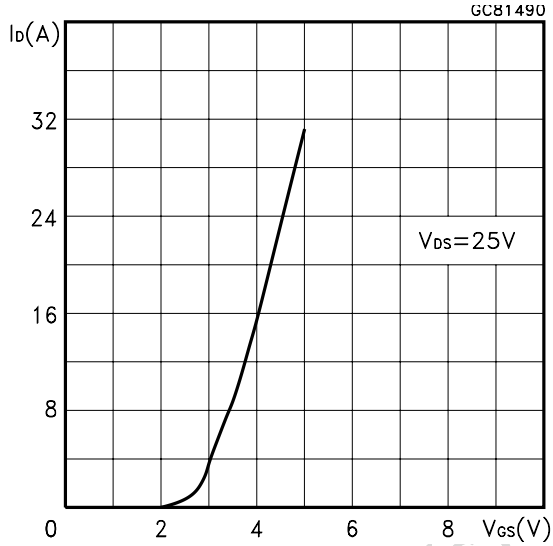
Thermal Impedance



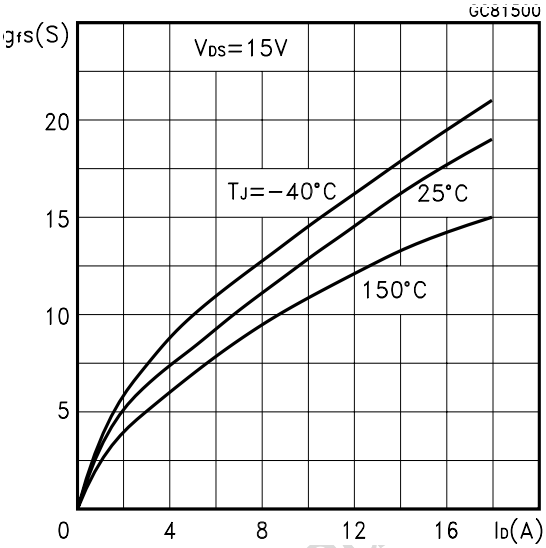
Output Characteristics



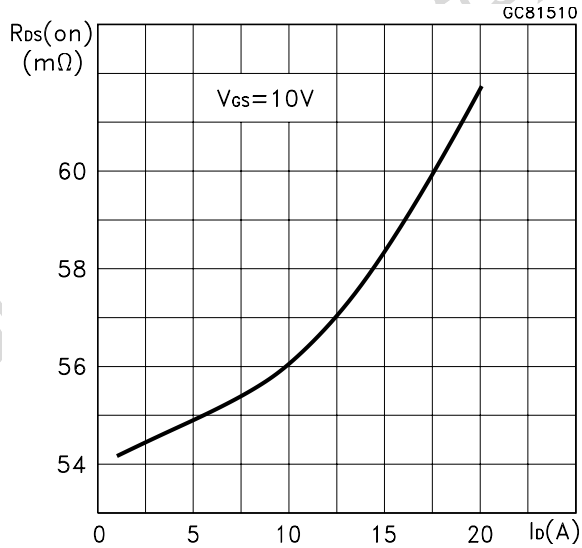
Transfer Characteristics



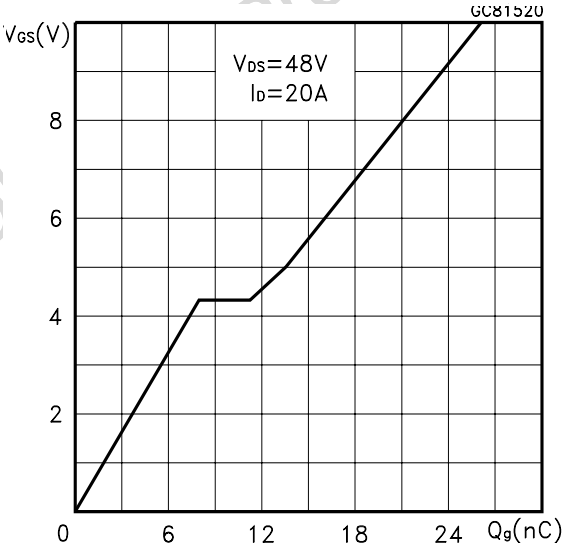
Transconductance



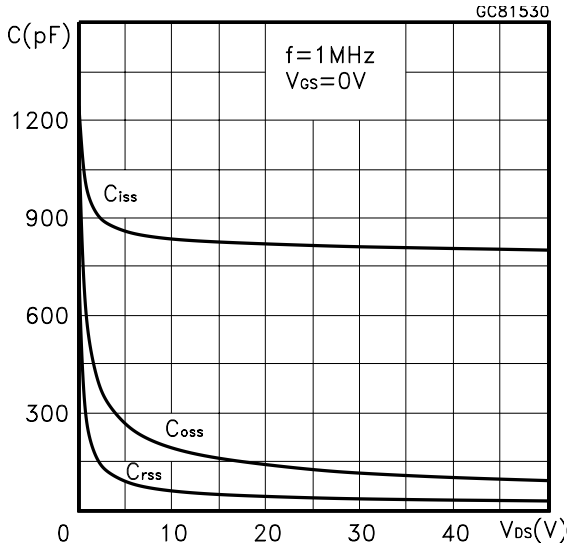
Static Drain-source On Resistance



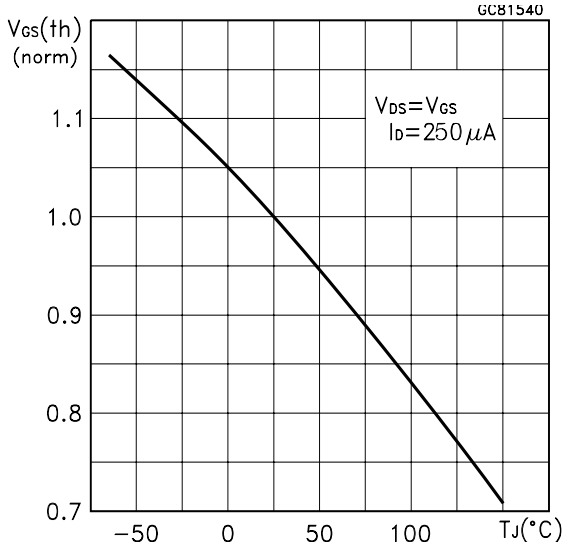
Gate Charge vs Gate-source Voltage



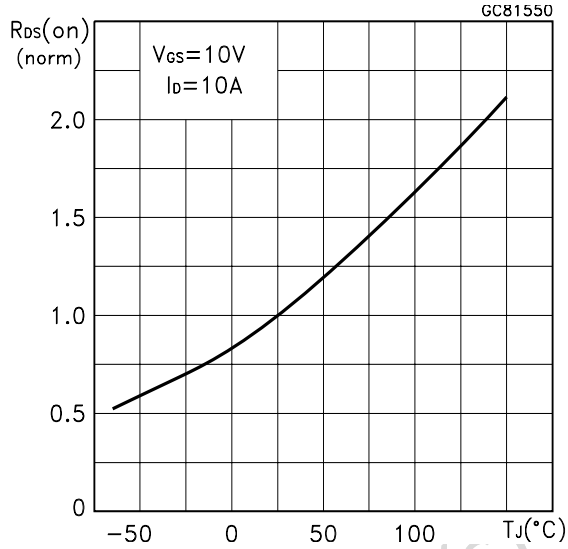
Capacitance Variations



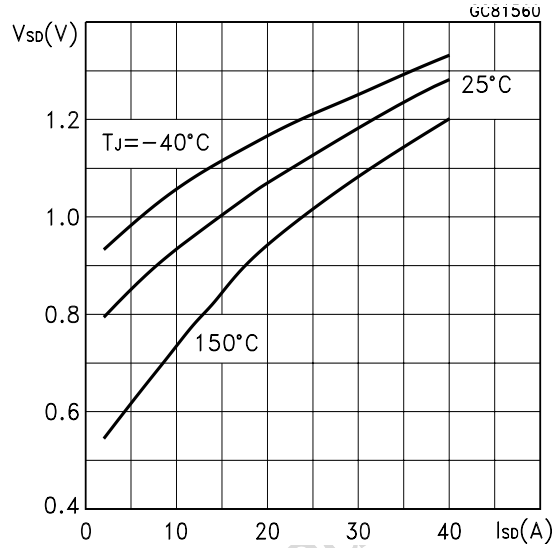
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage Temperature

Fig. 1: Unclamped Inductive Load Test Circuit

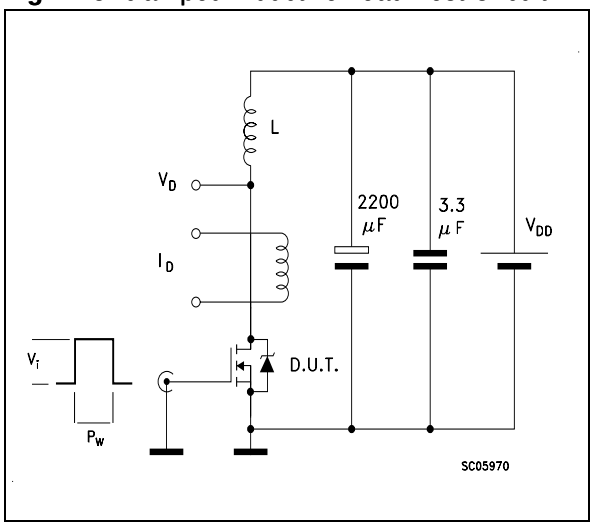


Fig. 2: Unclamped Inductive Waveform

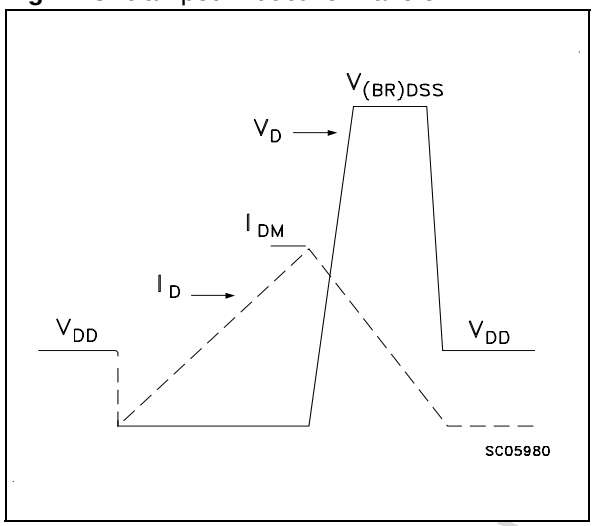


Fig. 3: Switching Times Test Circuits For Resistive Load

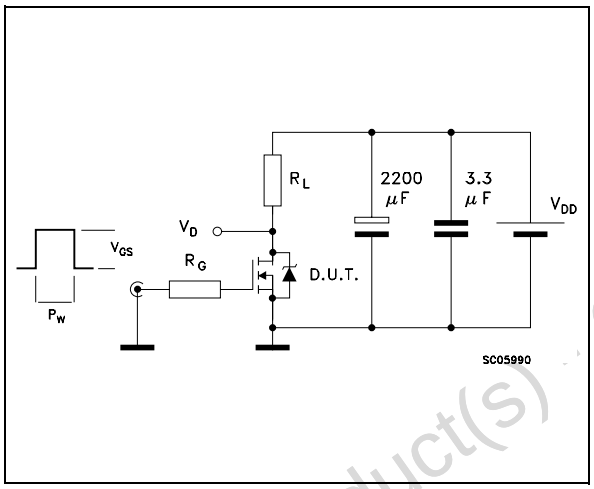


Fig. 4: Gate Charge test Circuit

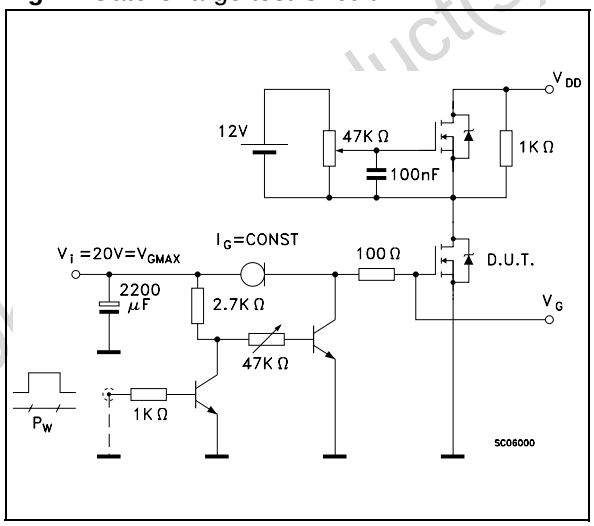
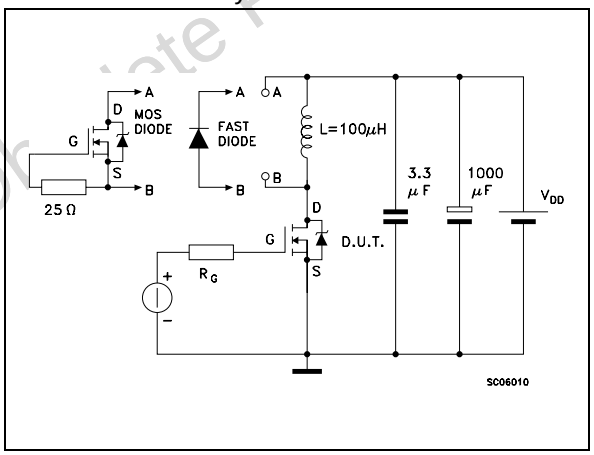
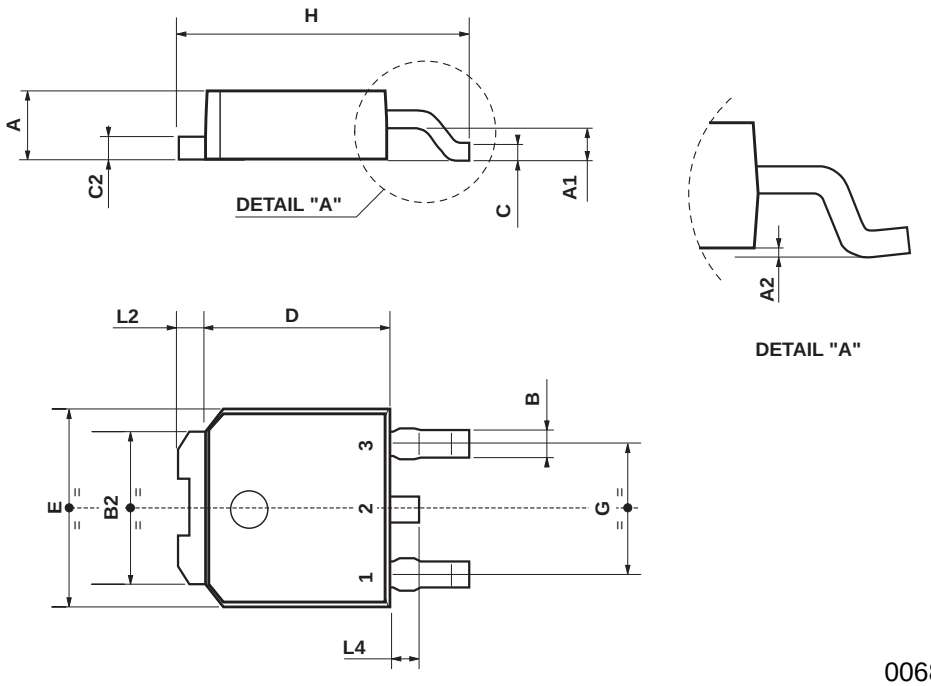


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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