

# MPSA13, MPSA14

MPSA14 is a Preferred Device

## Darlington Transistors

### NPN Silicon

#### Features

- Pb-Free Packages are Available\*

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	$V_{CES}$	30	Vdc
Collector–Base Voltage	$V_{CBO}$	30	Vdc
Emitter–Base Voltage	$V_{EBO}$	10	Vdc
Collector Current – Continuous	$I_C$	500	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	625 5.0	mW mW/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	1.5 12	W mW/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

#### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	200	$^\circ\text{C}/\text{mW}$
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	83.3	$^\circ\text{C}/\text{mW}$

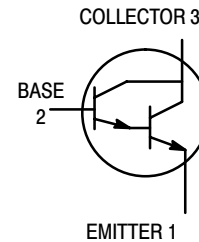
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

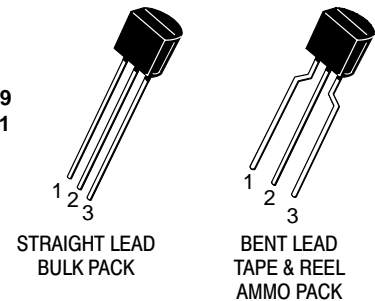


ON Semiconductor®

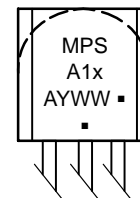
<http://onsemi.com>



TO-92  
CASE 29  
STYLE 1



#### MARKING DIAGRAM



- x = 3 or 4
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

# MPSA13, MPSA14

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit	
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Breakdown Voltage ( $I_C = 100 \mu\text{Adc}$ , $I_B = 0$ )	$V_{(BR)CES}$	30	–	Vdc	
Collector Cutoff Current ( $V_{CB} = 30 \text{ Vdc}$ , $I_E = 0$ )	$I_{CBO}$	–	100	nAdc	
Emitter Cutoff Current ( $V_{EB} = 10 \text{ Vdc}$ , $I_C = 0$ )	$I_{EBO}$	–	100	nAdc	
<b>ON CHARACTERISTICS (Note 1)</b>					
DC Current Gain ( $I_C = 10 \text{ mAdc}$ , $V_{CE} = 5.0 \text{ Vdc}$ )  ( $I_C = 100 \text{ mAdc}$ , $V_{CE} = 5.0 \text{ Vdc}$ )	$h_{FE}$	MPSA13 MPSA14 MPSA13 MPSA14	5,000 10,000 10,000 20,000	– – – –	–
Collector–Emitter Saturation Voltage ( $I_C = 100 \text{ mAdc}$ , $I_B = 0.1 \text{ mAdc}$ )	$V_{CE(sat)}$	–	1.5	Vdc	
Base–Emitter On Voltage ( $I_C = 100 \text{ mAdc}$ , $V_{CE} = 5.0 \text{ Vdc}$ )	$V_{BE(on)}$	–	2.0	Vdc	
<b>SMALL–SIGNAL CHARACTERISTICS</b>					
Current–Gain – Bandwidth Product (Note 2) ( $I_C = 10 \text{ mAdc}$ , $V_{CE} = 5.0 \text{ Vdc}$ , $f = 100 \text{ MHz}$ )	$f_T$	125	–	MHz	

1. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ ; Duty Cycle  $\leq 2.0\%$ .

2.  $f_T = |h_{fe}| \cdot f_{test}$ .

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
MPSA13	TO–92	5000 Units / Bulk
MPSA13G	TO–92 (Pb–Free)	5000 Units / Bulk
MPSA13RLRA	TO–92	2000 / Tape & Reel
MPSA13RLRAG	TO–92 (Pb–Free)	2000 / Tape & Reel
MPSA13RLRMG	TO–92 (Pb–Free)	2000 / Ammo Pack
MPSA13RLRPG	TO–92 (Pb–Free)	2000 / Ammo Pack
MPSA13ZL1G	TO–92 (Pb–Free)	2000 / Ammo Pack
MPSA14G	TO–92 (Pb–Free)	5000 Units / Bulk
MPSA14RLRAG	TO–92 (Pb–Free)	2000 / Tape & Reel
MPSA14RLRPG	TO–92 (Pb–Free)	2000 / Ammo Pack

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MPSA13, MPSA14

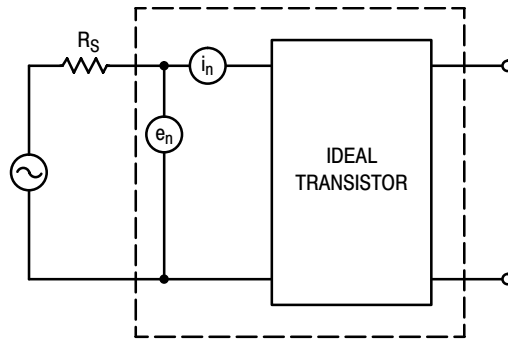


Figure 1. Transistor Noise Model

## NOISE CHARACTERISTICS

( $V_{CE} = 5.0 \text{ Vdc}$ ,  $T_A = 25^\circ\text{C}$ )

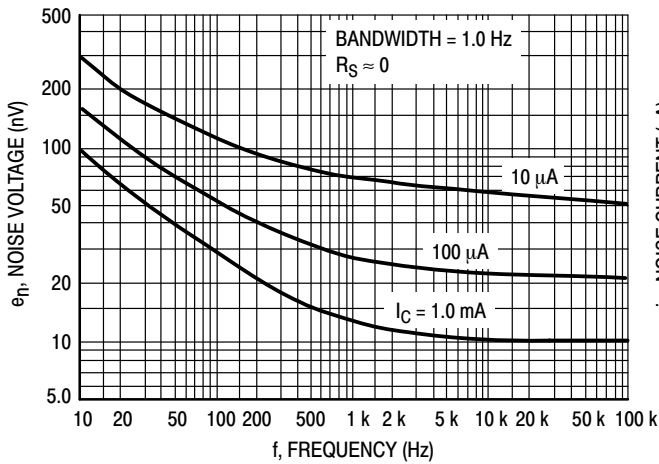


Figure 2. Noise Voltage

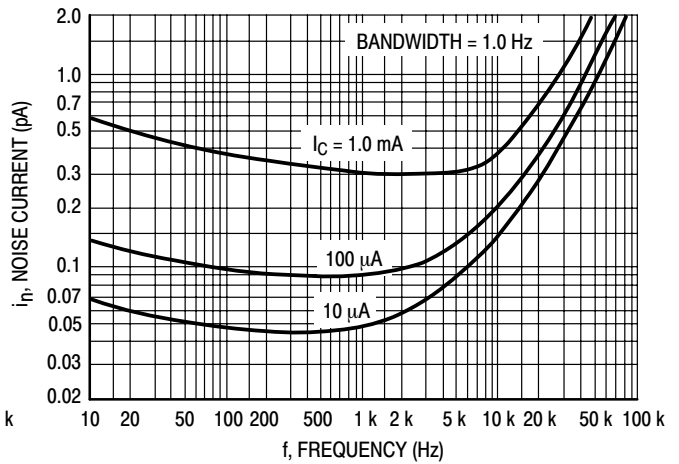


Figure 3. Noise Current

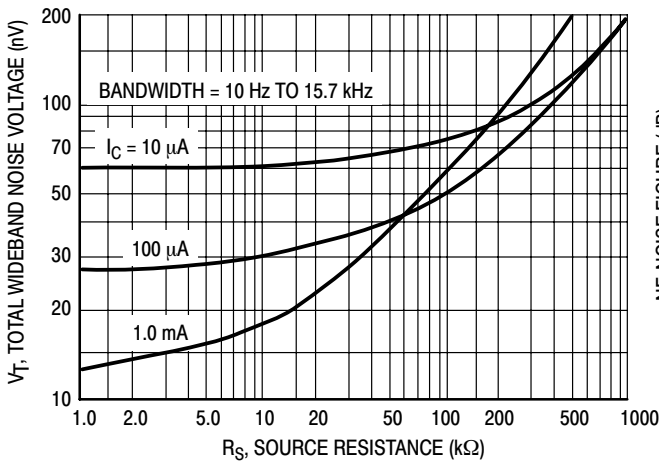


Figure 4. Total Wideband Noise Voltage

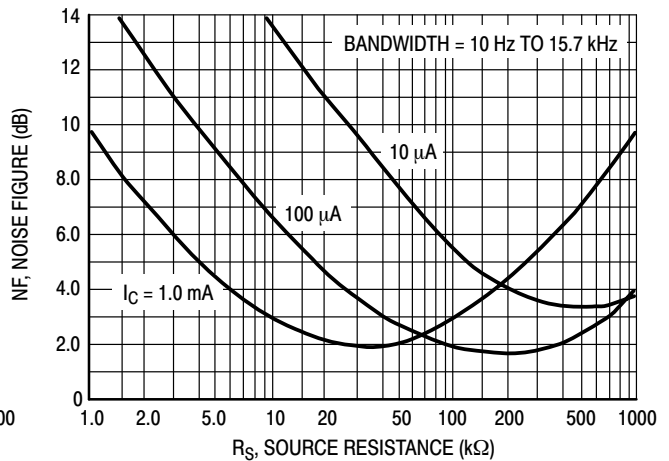


Figure 5. Wideband Noise Figure

# MPSA13, MPSA14

## SMALL-SIGNAL CHARACTERISTICS

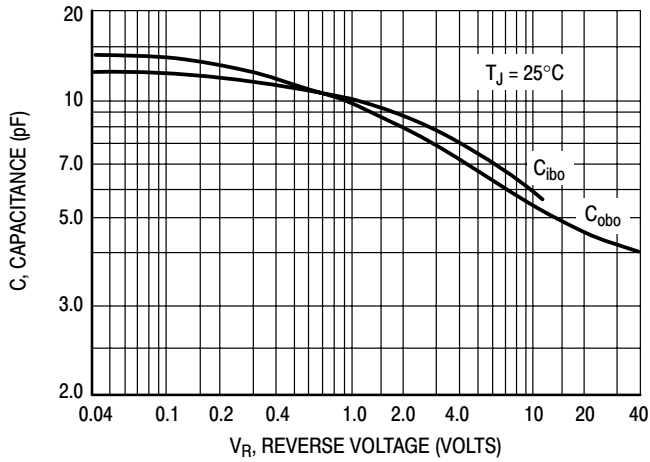


Figure 6. Capacitance

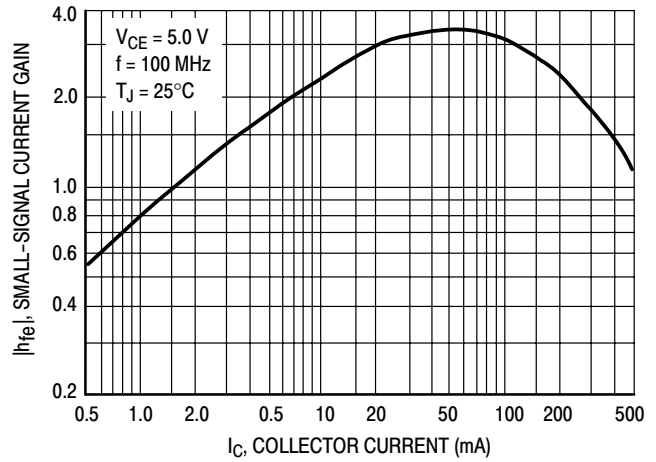


Figure 7. High Frequency Current Gain

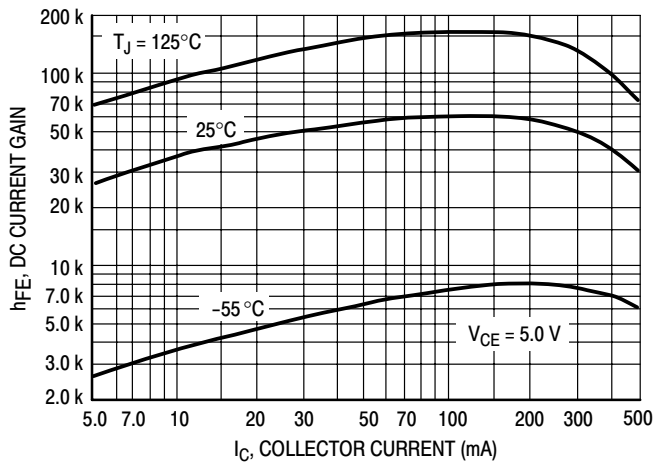


Figure 8. DC Current Gain

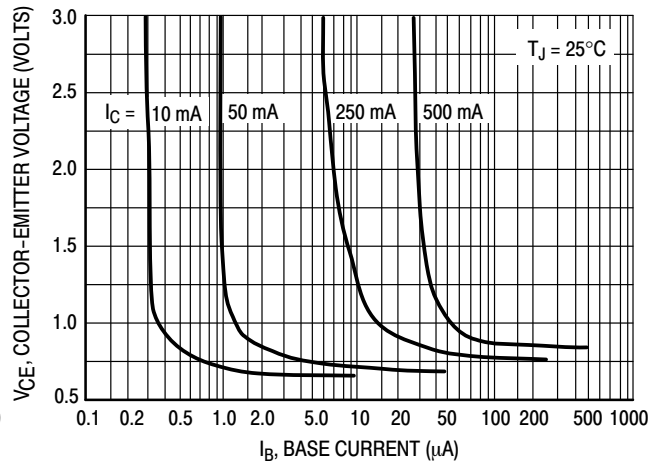


Figure 9. Collector Saturation Region

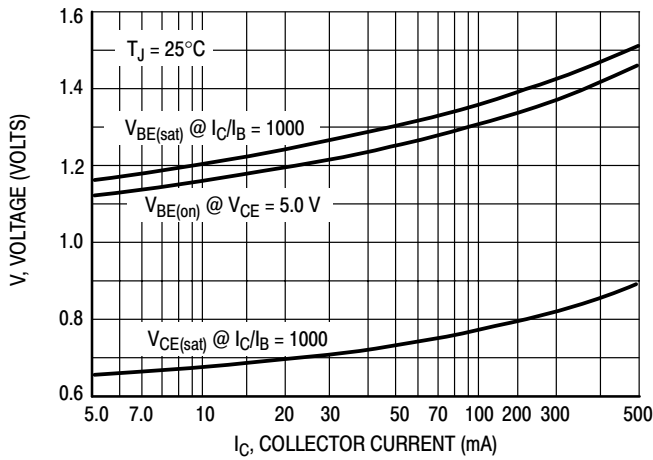


Figure 10. "On" Voltages

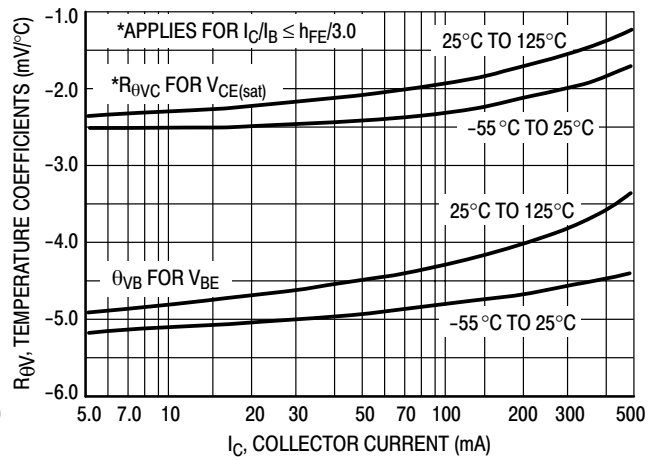


Figure 11. Temperature Coefficients

# MPSA13, MPSA14

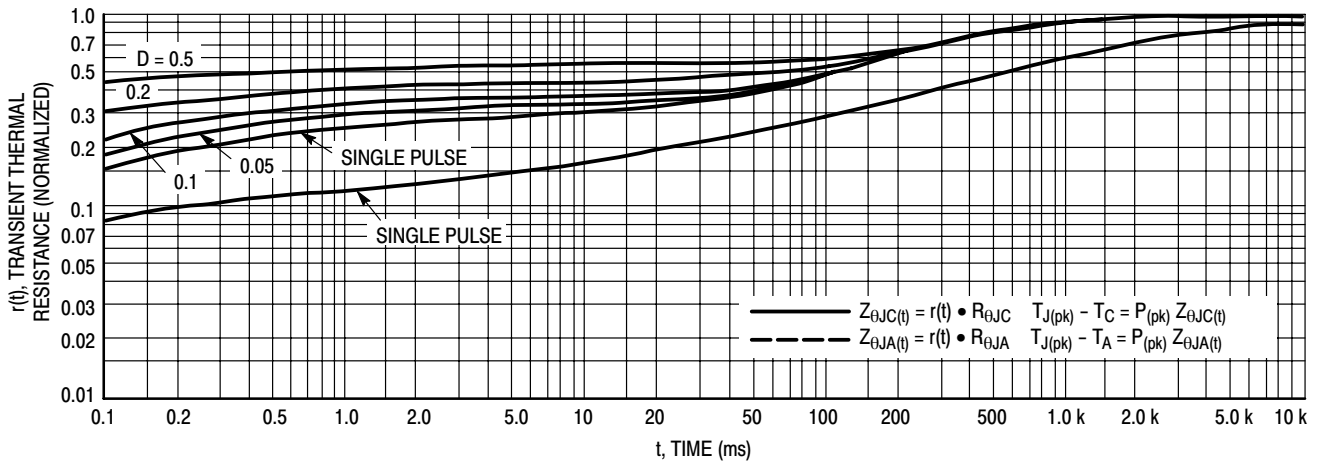


Figure 12. Thermal Response

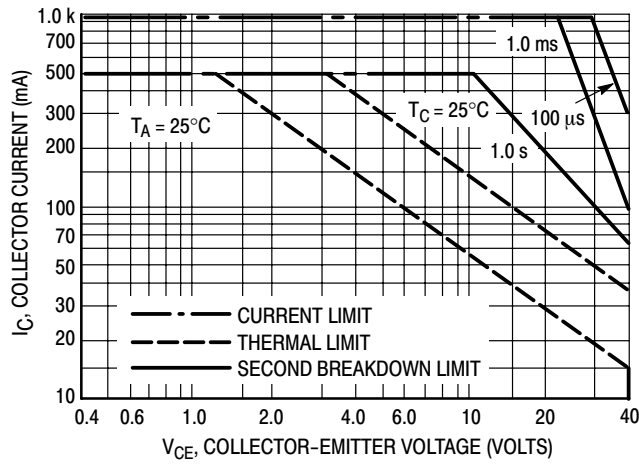
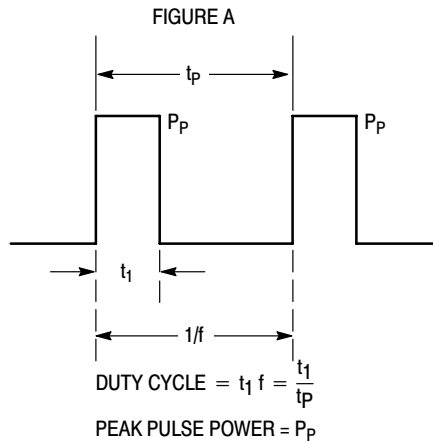


Figure 13. Active Region Safe Operating Area



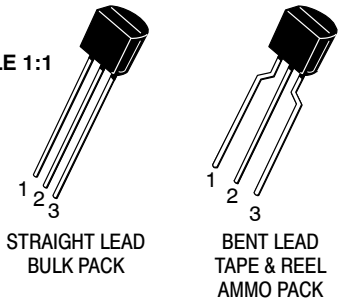
Design Note: Use of Transient Thermal Resistance Data

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

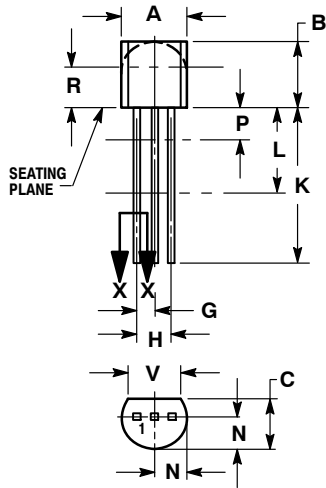


SCALE 1:1

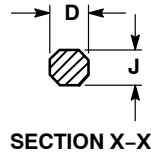


TO-92 (TO-226)  
CASE 29-11  
ISSUE AM

DATE 09 MAR 2007



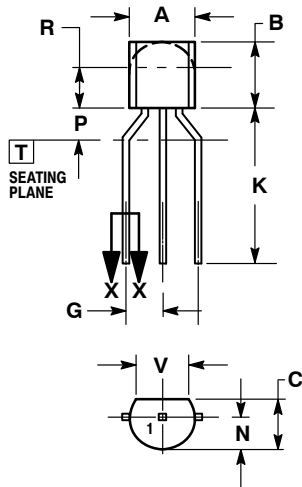
STRAIGHT LEAD  
BULK PACK



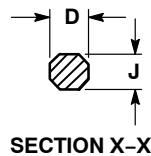
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD  
TAPE & REEL  
AMMO PACK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS	
	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42022B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO-92 (TO-226)	PAGE 1 OF 3

**TO-92 (TO-226)**  
**CASE 29-11**  
**ISSUE AM**

DATE 09 MAR 2007

- |  |   |   |  |  |
|--|---|---|--|--|
| <p>STYLE 1:<br/>         PIN 1. EMITTER<br/>         2. BASE<br/>         3. COLLECTOR</p>             | <p>STYLE 2:<br/>         PIN 1. BASE<br/>         2. EMITTER<br/>         3. COLLECTOR</p>                | <p>STYLE 3:<br/>         PIN 1. ANODE<br/>         2. ANODE<br/>         3. CATHODE</p>               | <p>STYLE 4:<br/>         PIN 1. CATHODE<br/>         2. CATHODE<br/>         3. ANODE</p>            | <p>STYLE 5:<br/>         PIN 1. DRAIN<br/>         2. SOURCE<br/>         3. GATE</p>            |
| <p>STYLE 6:<br/>         PIN 1. GATE<br/>         2. SOURCE &amp; SUBSTRATE<br/>         3. DRAIN</p>  | <p>STYLE 7:<br/>         PIN 1. SOURCE<br/>         2. DRAIN<br/>         3. GATE</p>                     | <p>STYLE 8:<br/>         PIN 1. DRAIN<br/>         2. GATE<br/>         3. SOURCE &amp; SUBSTRATE</p> | <p>STYLE 9:<br/>         PIN 1. BASE 1<br/>         2. EMITTER<br/>         3. BASE 2</p>            | <p>STYLE 10:<br/>         PIN 1. CATHODE<br/>         2. GATE<br/>         3. ANODE</p>          |
| <p>STYLE 11:<br/>         PIN 1. ANODE<br/>         2. CATHODE &amp; ANODE<br/>         3. CATHODE</p> | <p>STYLE 12:<br/>         PIN 1. MAIN TERMINAL 1<br/>         2. GATE<br/>         3. MAIN TERMINAL 2</p> | <p>STYLE 13:<br/>         PIN 1. ANODE 1<br/>         2. GATE<br/>         3. CATHODE 2</p>           | <p>STYLE 14:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR<br/>         3. BASE</p>          | <p>STYLE 15:<br/>         PIN 1. ANODE 1<br/>         2. CATHODE<br/>         3. ANODE 2</p>     |
| <p>STYLE 16:<br/>         PIN 1. ANODE<br/>         2. GATE<br/>         3. CATHODE</p>                | <p>STYLE 17:<br/>         PIN 1. COLLECTOR<br/>         2. BASE<br/>         3. EMITTER</p>               | <p>STYLE 18:<br/>         PIN 1. ANODE<br/>         2. CATHODE<br/>         3. NOT CONNECTED</p>      | <p>STYLE 19:<br/>         PIN 1. GATE<br/>         2. ANODE<br/>         3. CATHODE</p>              | <p>STYLE 20:<br/>         PIN 1. NOT CONNECTED<br/>         2. CATHODE<br/>         3. ANODE</p> |
| <p>STYLE 21:<br/>         PIN 1. COLLECTOR<br/>         2. EMITTER<br/>         3. BASE</p>            | <p>STYLE 22:<br/>         PIN 1. SOURCE<br/>         2. GATE<br/>         3. DRAIN</p>                    | <p>STYLE 23:<br/>         PIN 1. GATE<br/>         2. SOURCE<br/>         3. DRAIN</p>                | <p>STYLE 24:<br/>         PIN 1. EMITTER<br/>         2. COLLECTOR/ANODE<br/>         3. CATHODE</p> | <p>STYLE 25:<br/>         PIN 1. MT 1<br/>         2. GATE<br/>         3. MT 2</p>              |
| <p>STYLE 26:<br/>         PIN 1. V<sub>CC</sub><br/>         2. GROUND 2<br/>         3. OUTPUT</p>    | <p>STYLE 27:<br/>         PIN 1. MT<br/>         2. SUBSTRATE<br/>         3. MT</p>                      | <p>STYLE 28:<br/>         PIN 1. CATHODE<br/>         2. ANODE<br/>         3. GATE</p>               | <p>STYLE 29:<br/>         PIN 1. NOT CONNECTED<br/>         2. ANODE<br/>         3. CATHODE</p>     | <p>STYLE 30:<br/>         PIN 1. DRAIN<br/>         2. GATE<br/>         3. SOURCE</p>           |
| <p>STYLE 31:<br/>         PIN 1. GATE<br/>         2. DRAIN<br/>         3. SOURCE</p>                 | <p>STYLE 32:<br/>         PIN 1. BASE<br/>         2. COLLECTOR<br/>         3. EMITTER</p>               | <p>STYLE 33:<br/>         PIN 1. RETURN<br/>         2. INPUT<br/>         3. OUTPUT</p>              | <p>STYLE 34:<br/>         PIN 1. INPUT<br/>         2. GROUND<br/>         3. LOGIC</p>              | <p>STYLE 35:<br/>         PIN 1. GATE<br/>         2. COLLECTOR<br/>         3. EMITTER</p>      |

<b>DOCUMENT NUMBER:</b>	<b>98ASB42022B</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>STATUS:</b>	<b>ON SEMICONDUCTOR STANDARD</b>	
<b>NEW STANDARD:</b>		
<b>DESCRIPTION:</b>	<b>TO-92 (TO-226)</b>	<b>PAGE 2 OF 3</b>



ISSUE	REVISION	DATE
AM	ADDED BENT-LEAD TAPE & REEL VERSION. REQ. BY J. SUPINA.	09 MAR 2007

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

