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MPSW55, MPSW56

One Watt Amplifier Transistors

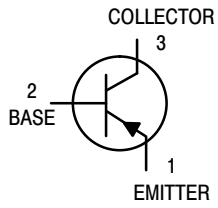
PNP Silicon

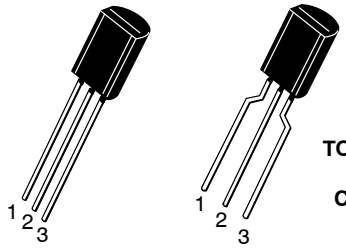
ON Semiconductor®

http://onsemi.com

Features

- Pb−Free Packages are Available*





STRAIGHT LEAD BULK PACK

BENT LEAD TAPE & REEL AMMO PACK

TO−92 1 WATT (TO−226) CASE 29−10 STYLE 1

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Collector − Emitter Voltage	MPSW55 MPSW56	V_{CEO}	−60 −80	Vdc
Collector − Base Voltage	MPSW55 MPSW56	V_{CBO}	−60 −80	Vdc
Emitter − Base Voltage		V_{EBO}	−4.0	Vdc
Collector Current − Continuous		I_C	−500	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C		P_D	1.0 8.0	W mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C		P_D	2.5 20	W mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to +150	°C

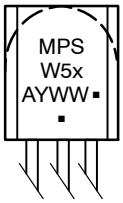
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	125	°C/W
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	50	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM



x = 5 or 6
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MPSW55G	TO−92 (Pb−Free)	5000 Units/Bulk
MPSW55RLRAG	TO−92 (Pb−Free)	2000/Tape & Reel
MPSW56RLRP	TO−92	2000/Ammo Pack
MPSW56RLRPG	TO−92 (Pb−Free)	2000/Ammo Pack

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (Note 1)		$V_{(BR)CEO}$			Vdc
(I_C = –1.0 mAdc, I_B = 0)	MPSW55		–60	–	
	MPSW56		–80	–	
Emitter – Base Breakdown Voltage		$V_{(BR)EBO}$			Vdc
(I_E = –100 μAdc, I_C = 0)			–4.0	–	
Collector Cutoff Current		I_{CES}			μAdc
(V_{CE} = –40 Vdc, I_B = 0)	MPSW55		–	–0.5	
(V_{CE} = –60 Vdc, I_B = 0)	MPSW56		–	–0.5	
Collector Cutoff Current		I_{CBO}			μAdc
(V_{CB} = –40 Vdc, I_E = 0)	MPSW55		–	–0.1	
(V_{CB} = –60 Vdc, I_E = 0)	MPSW56		–	–0.1	
Emitter Cutoff Current		I_{EBO}			μAdc
(V_{EB} = –3.0 Vdc, I_C = 0)			–	–0.1	
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			–
(I_C = –50 mAdc, V_{CE} = –1.0 Vdc)			100	–	
(I_C = –250 mAdc, V_{CE} = –1.0 Vdc)			50	–	
Collector – Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = –250 mAdc, I_B = –10 mAdc)			–	–0.5	
Base–Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = –250 mAdc, V_{CE} = –5.0 Vdc)			–	–1.2	
SMALL–SIGNAL CHARACTERISTICS					
Current – Gain — Bandwidth Product		f_T			MHz
(I_C = –250 mAdc, V_{CE} = –5.0 Vdc, f = 20 MHz)			50	–	
Output Capacitance		C_{obo}			pF
(V_{CB} = –10 Vdc, f = 1.0 MHz)			–	15	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

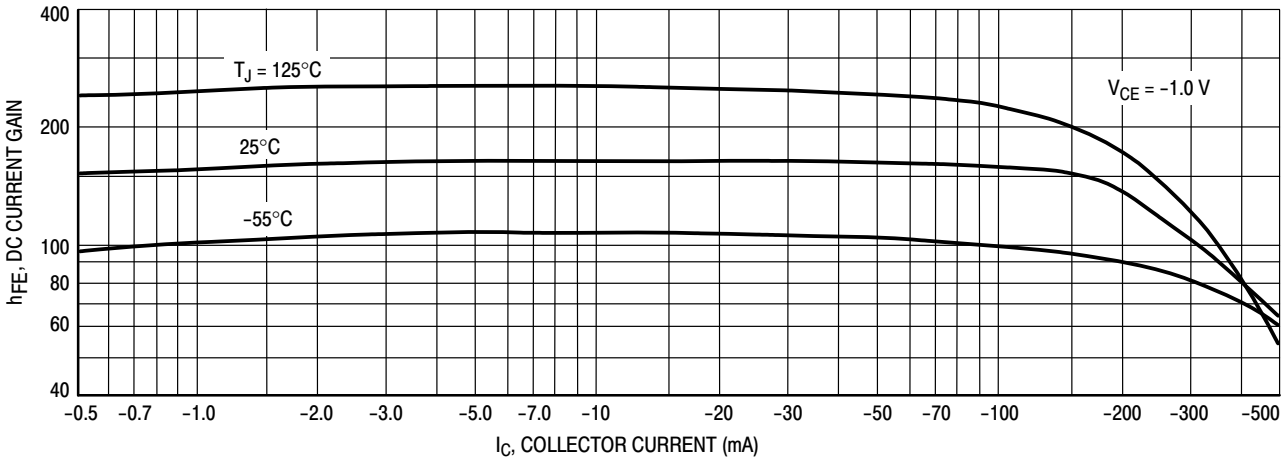


Figure 1. DC Current Gain

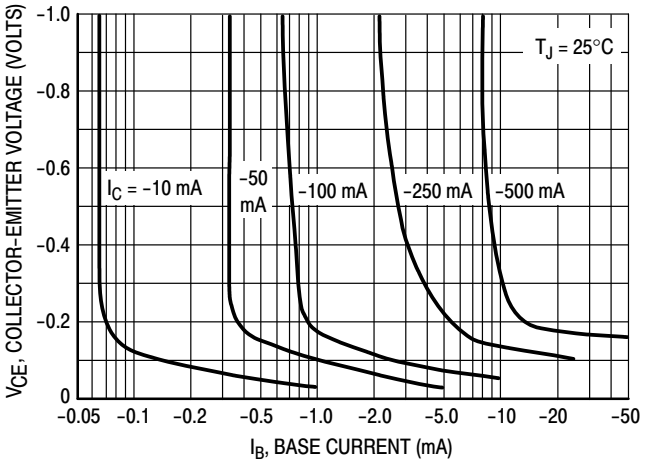


Figure 2. Collector Saturation Region

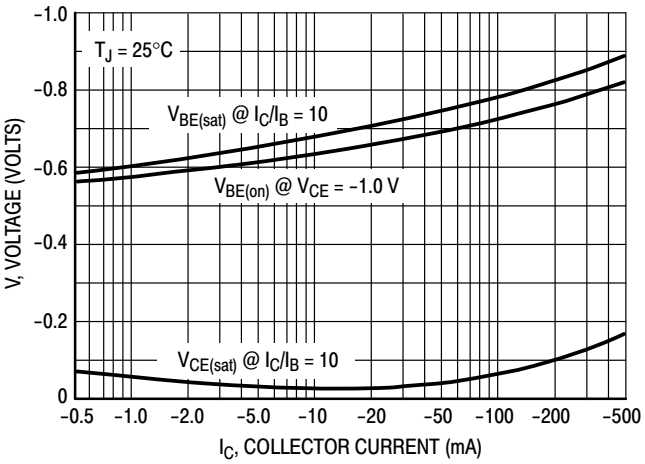


Figure 3. “On” Voltages

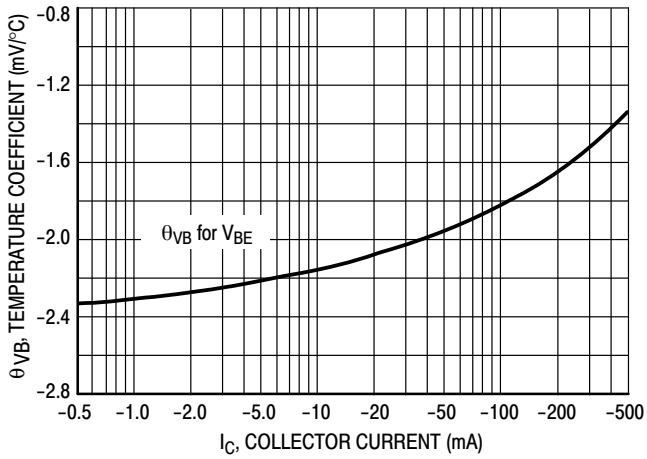


Figure 4. Base−Emitter Temperature Coefficient

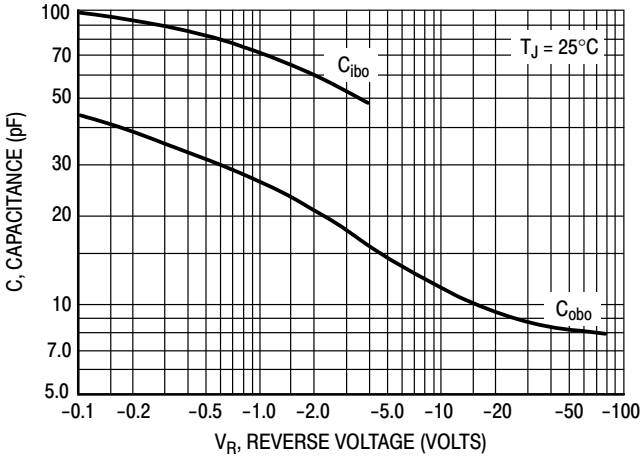


Figure 5. Capacitance

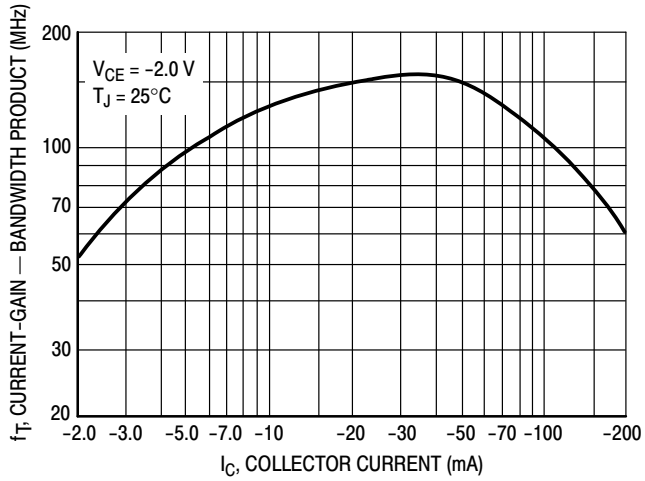


Figure 6. Current−Gain — Bandwidth Product

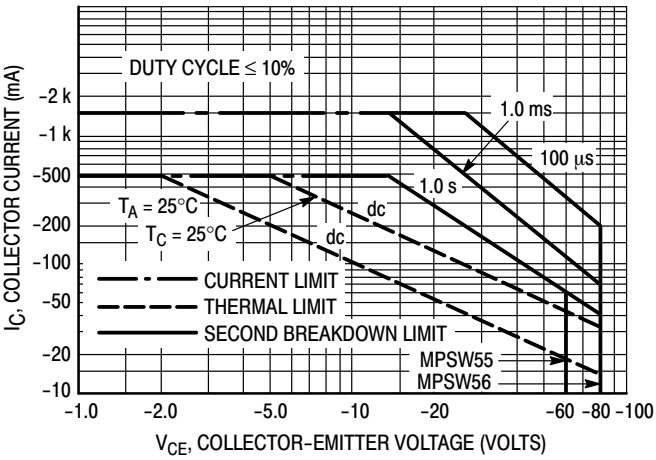


Figure 7. Active Region — Safe Operating Area

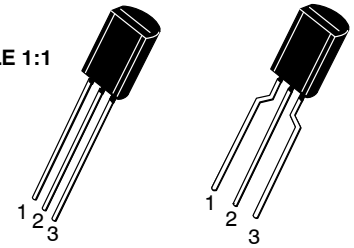
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

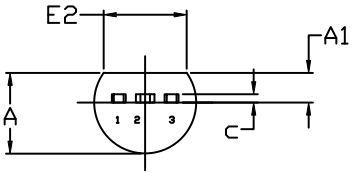
DATE 05 MAR 2021

SCALE 1:1

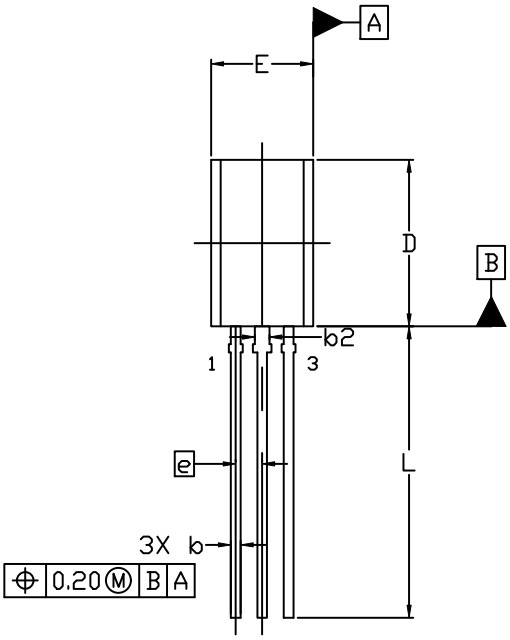


STRAIGHT LEAD BENT LEAD

STRAIGHT LEAD



END VIEW



TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS.
4. DIMENSION b AND b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 0.20. DIMENSION b2 LOCATED ABOVE THE DAMBAR PORTION OF MIDDLE LEAD.

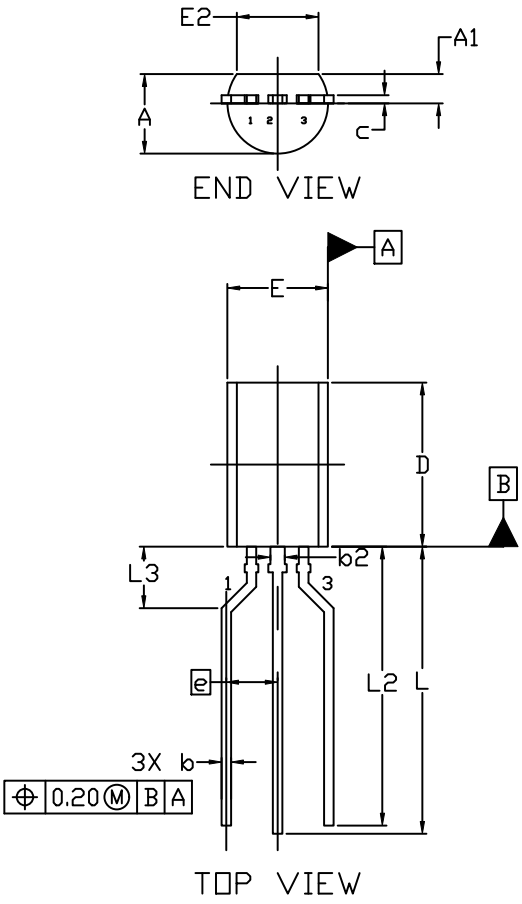
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	3.75	3.90	4.05
A1	1.28	1.43	1.58
b	0.38	0.465	0.55
b2	0.62	0.70	0.78
c	0.35	0.40	0.45
D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	1.27 BSC		
L	13.80	14.00	14.20

STYLES AND MARKING ON PAGE 3

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

FORMED LEAD



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D	7.85	8.00	8.15
E	4.75	4.90	5.05
E2	3.90	---	---
e	2.50 BSC		
L	13.80	14.00	14.20
L2	13.20	13.60	14.00
L3	3.00 REF		

STYLES AND MARKING ON PAGE 3

TO−92 (TO−226) 1 WATT
CASE 29−10
ISSUE D

DATE 05 MAR 2021

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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