

## N-channel 600 V, 0.290 $\Omega$ typ., 8 A MDmesh™ M2 Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet - production data

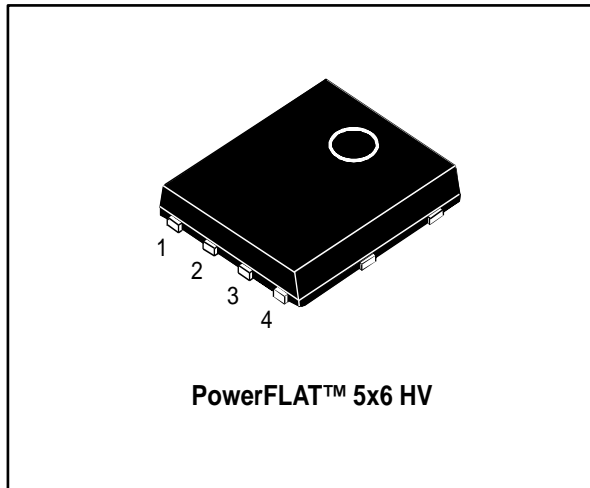
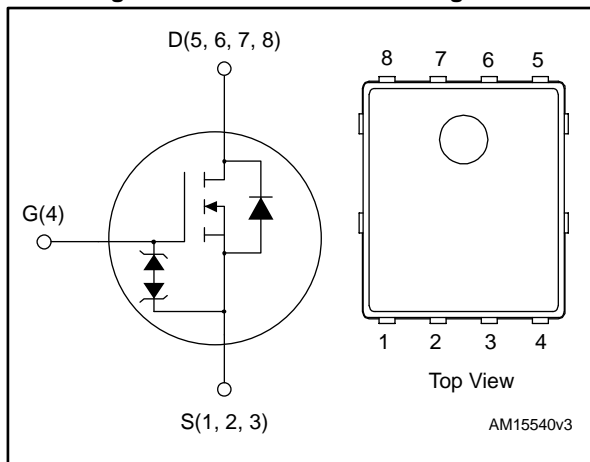


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub> @ T <sub>Jmax</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL16N60M2	650 V	0.355 $\Omega$	8 A

- Extremely low gate charge
- Excellent output capacitance (C<sub>oss</sub>) profile
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance and optimized switching characteristics, rendering it suitable for the most demanding high efficiency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STL16N60M2	16N60M2	PowerFLAT™ 5x6 HV	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	8 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	5	A
$I_{DM}$ <sup>(2)</sup>	Drain current (pulsed)	32	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	52	W
$dv/dt$ <sup>(3)</sup>	Peak diode recovery voltage slope	15	V/ns
$dv/dt$ <sup>(4)</sup>	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	°C
$T_j$	Max. operating junction temperature	150	

**Notes:**

<sup>(1)</sup>The value is limited by package.

<sup>(2)</sup>Pulse width limited by safe operating area.

<sup>(3)</sup> $I_{SD} \leq 8\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

<sup>(4)</sup> $V_{DS} \leq 480\text{ V}$

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.40	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max <sup>(1)</sup>	59	°C/W

**Notes:**

<sup>(1)</sup>When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	130	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5: On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 4\text{ A}$		0.290	0.355	$\Omega$

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	704	-	pF
$C_{oss}$	Output capacitance		-	38	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1.2	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ V to } 480\text{ V}$ , $V_{GS} = 0\text{ V}$	-	140	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.3	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 12\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15: "Gate charge test circuit"</a> )	-	19	-	nC
$Q_{gs}$	Gate-source charge		-	3.3	-	nC
$Q_{gd}$	Gate-drain charge		-	9.5	-	nC

**Notes:**

<sup>(1)</sup> $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 6\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14: "Switching times test circuit for resistive load"</a> and <a href="#">Figure 19: "Switching time waveform"</a> )	-	10.5	-	ns
$t_r$	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	58	-	ns
$t_f$	Fall time		-	18.5	-	ns

Table 8: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		8	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		32	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}, I_{SD} = 8 \text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 12 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	316		ns
$Q_{rr}$	Reverse recovery charge		-	3.25		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	20.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 12 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}, V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	455		ns
$Q_{rr}$	Reverse recovery charge		-	4.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	21		A

**Notes:**

<sup>(1)</sup>Pulse width is limited by safe operating area

<sup>(2)</sup>Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}, I_D = 0 \text{ A}$	30	-	-	V

## 2.1 Electrical characteristics (curves)

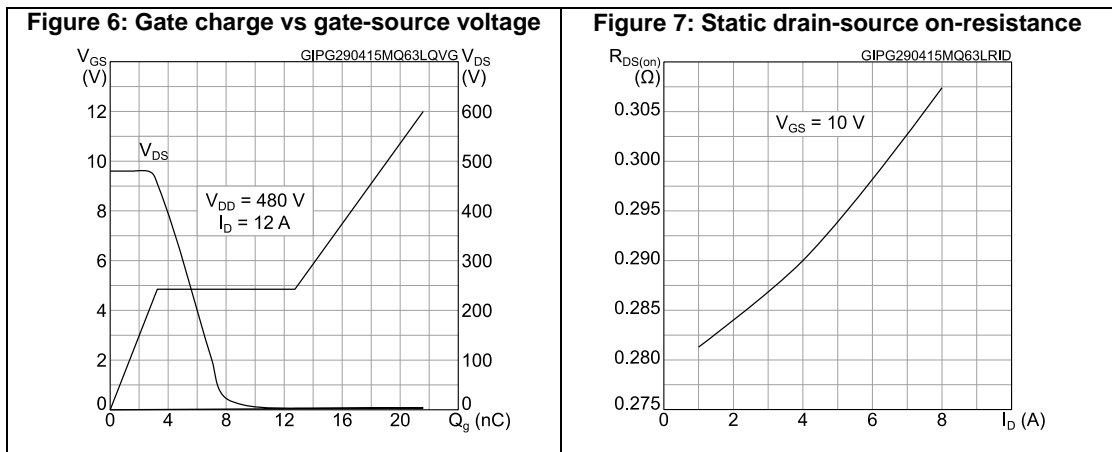
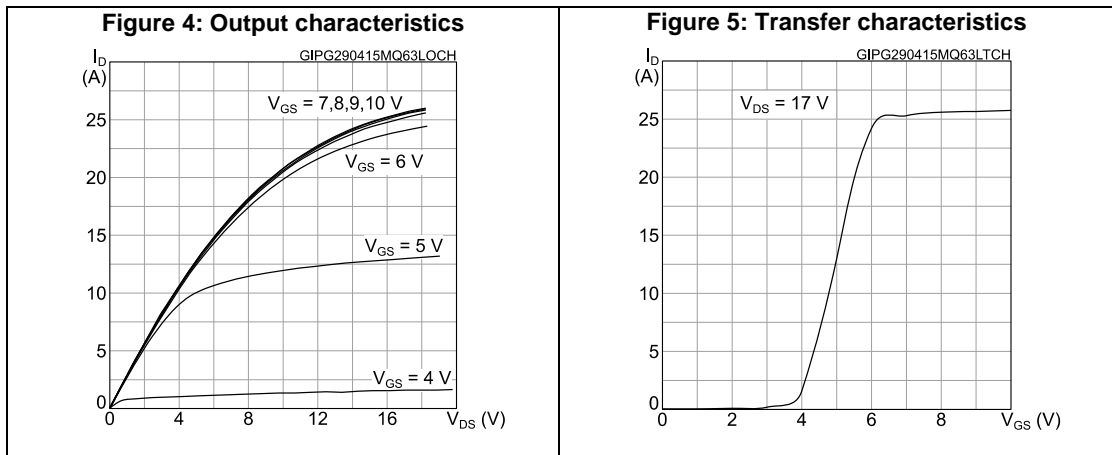
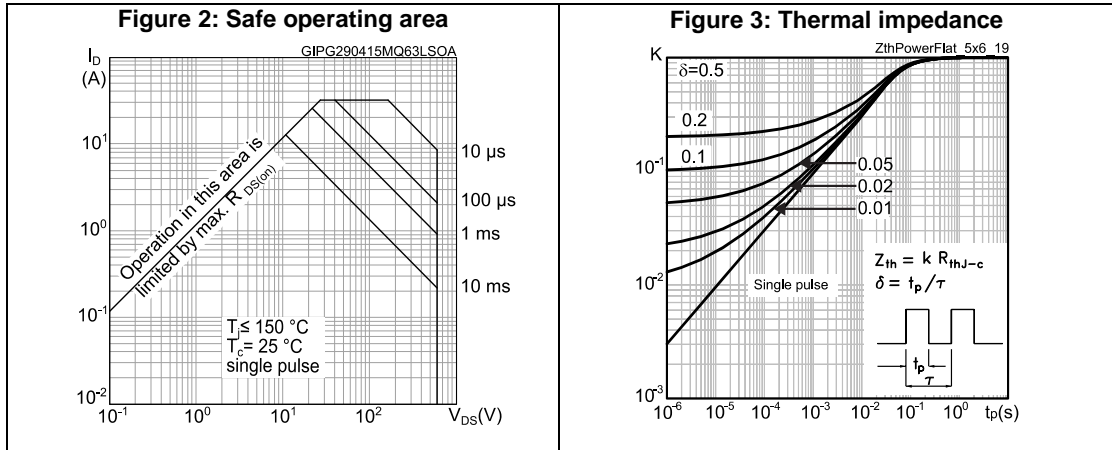


Figure 8: Capacitance variations

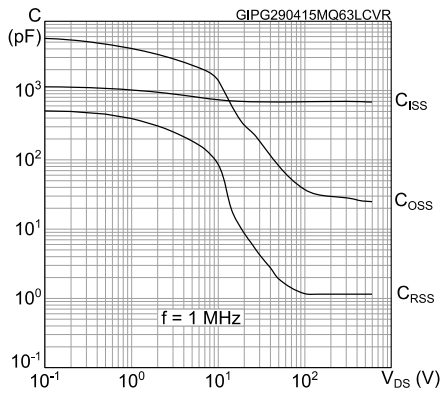


Figure 9: Normalized gate threshold voltage vs temperature

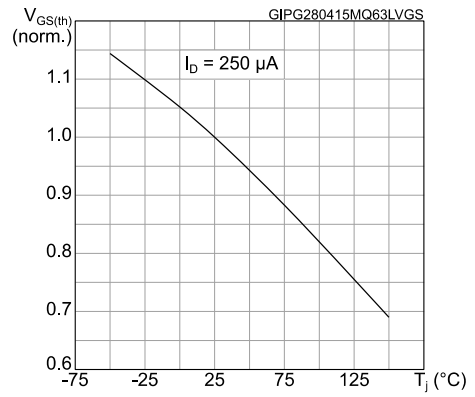


Figure 10: Normalized on-resistance vs temperature

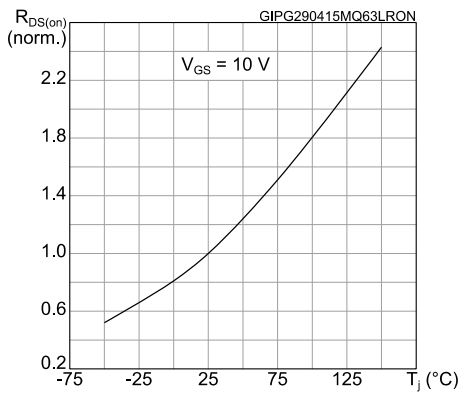


Figure 11: Normalized V(BR)DSS vs temperature

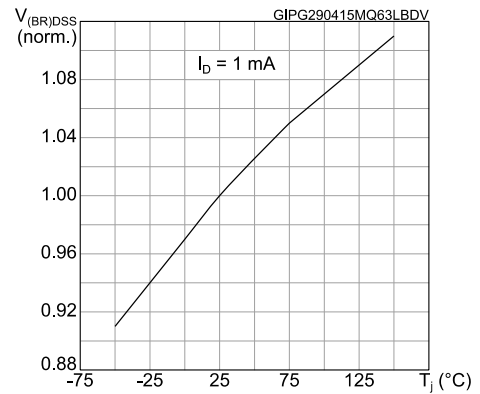


Figure 12: Source-drain diode forward characteristics

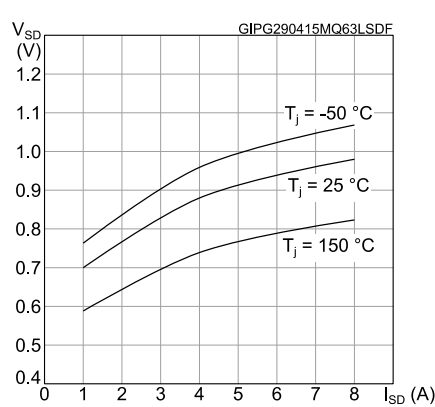
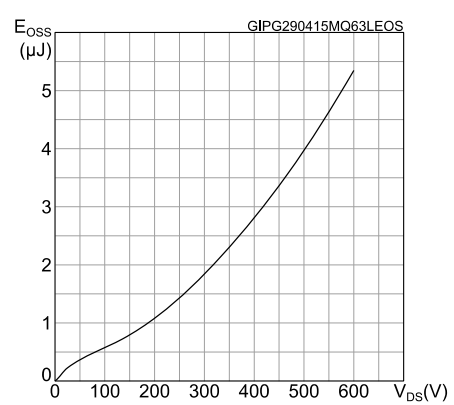
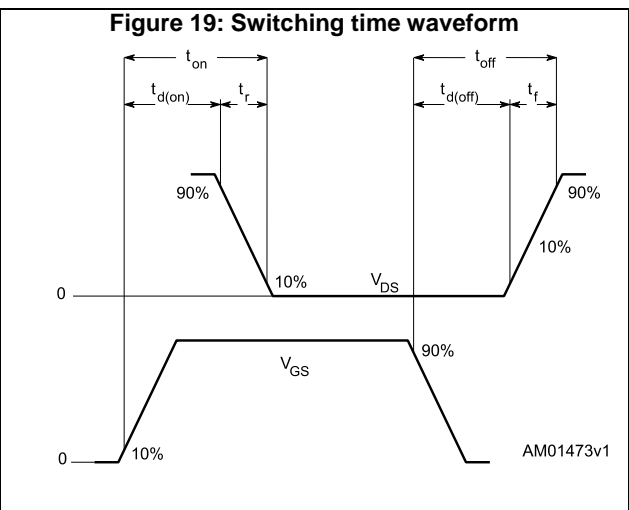
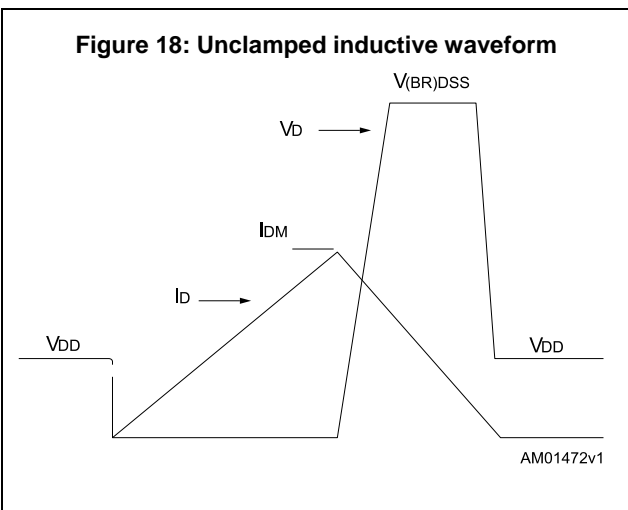
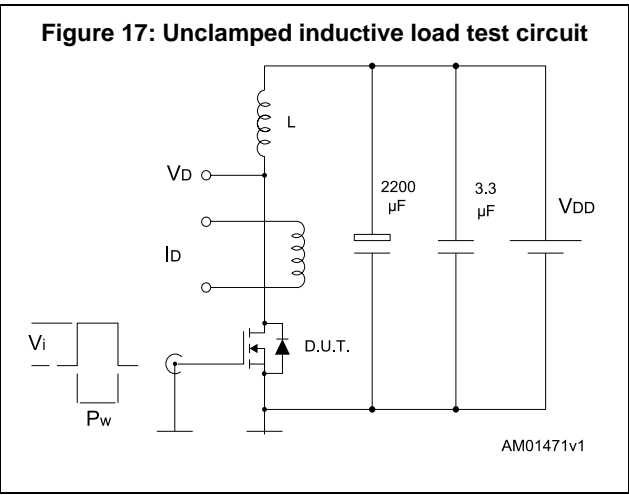
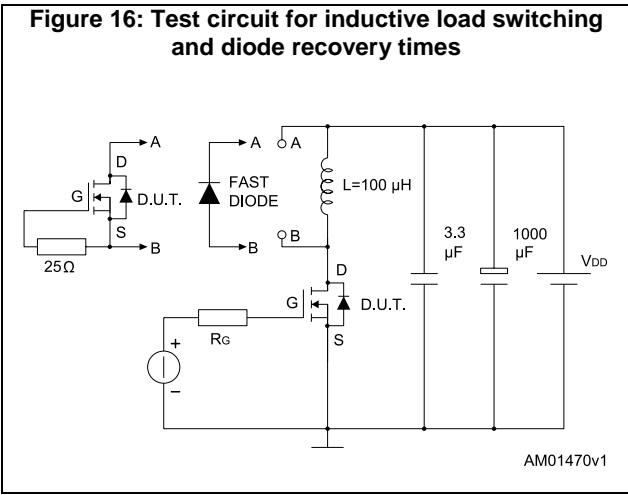
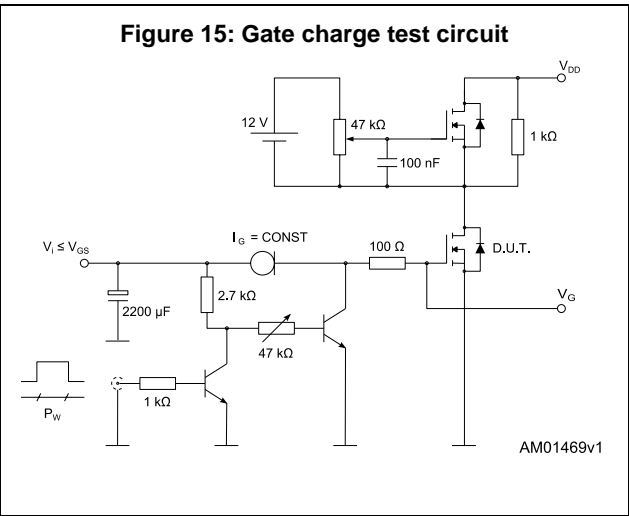
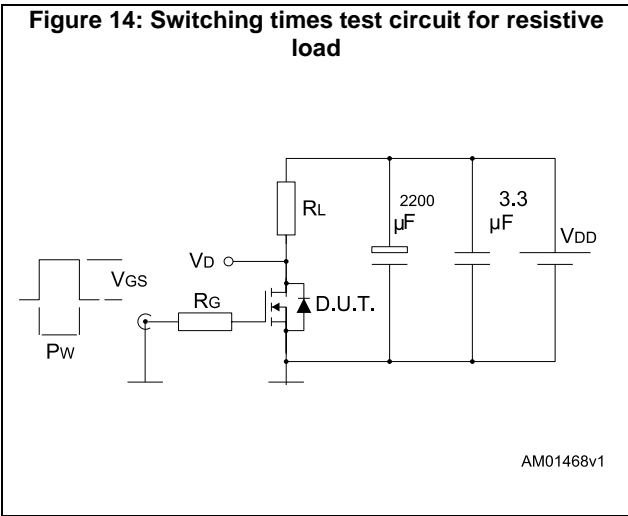


Figure 13: Output capacitance stored energy



### 3 Test circuits





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 PowerFLAT™ 5x6 HV package information

Figure 20: PowerFLAT™ 5x6 HV package outline

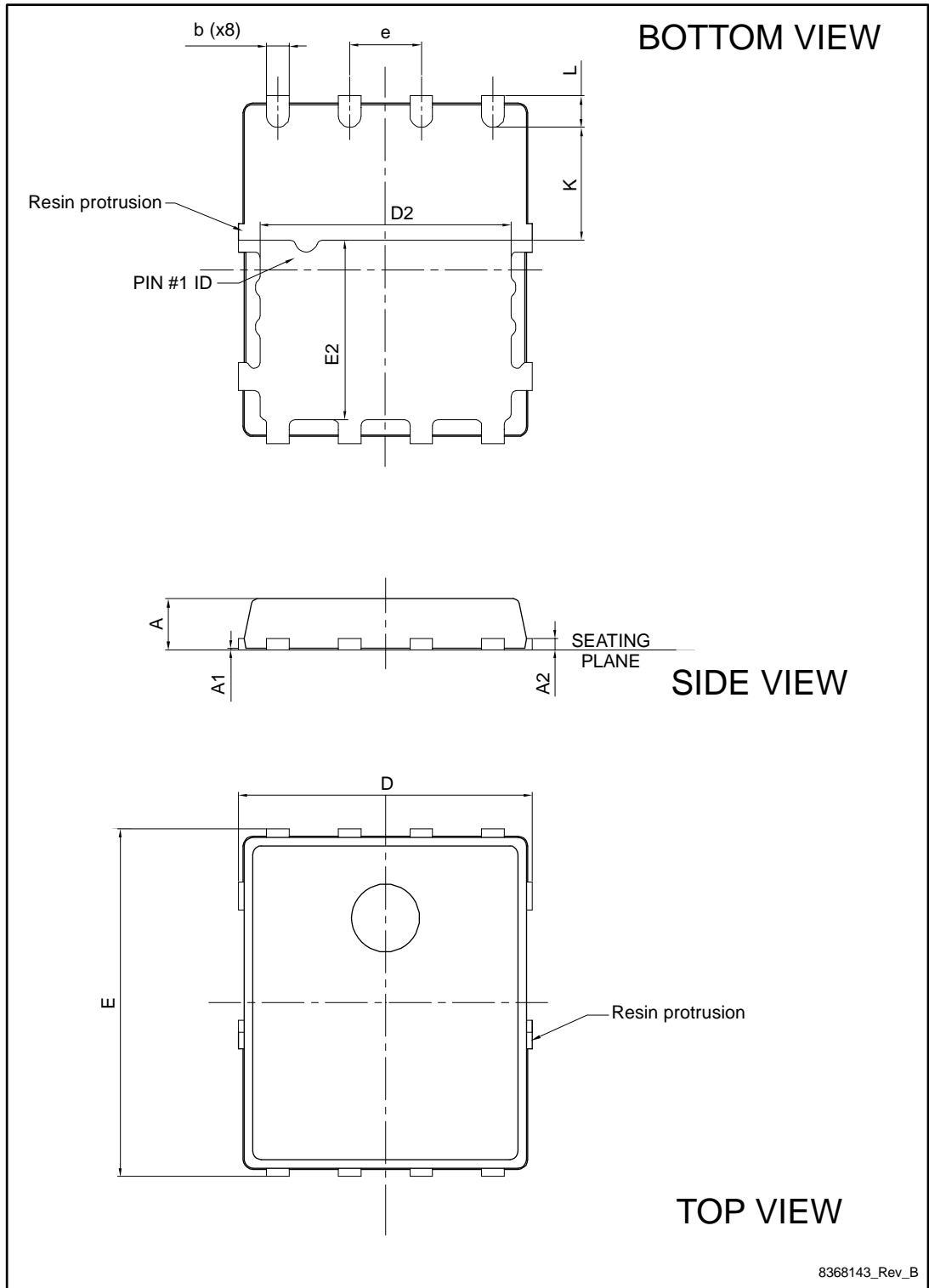
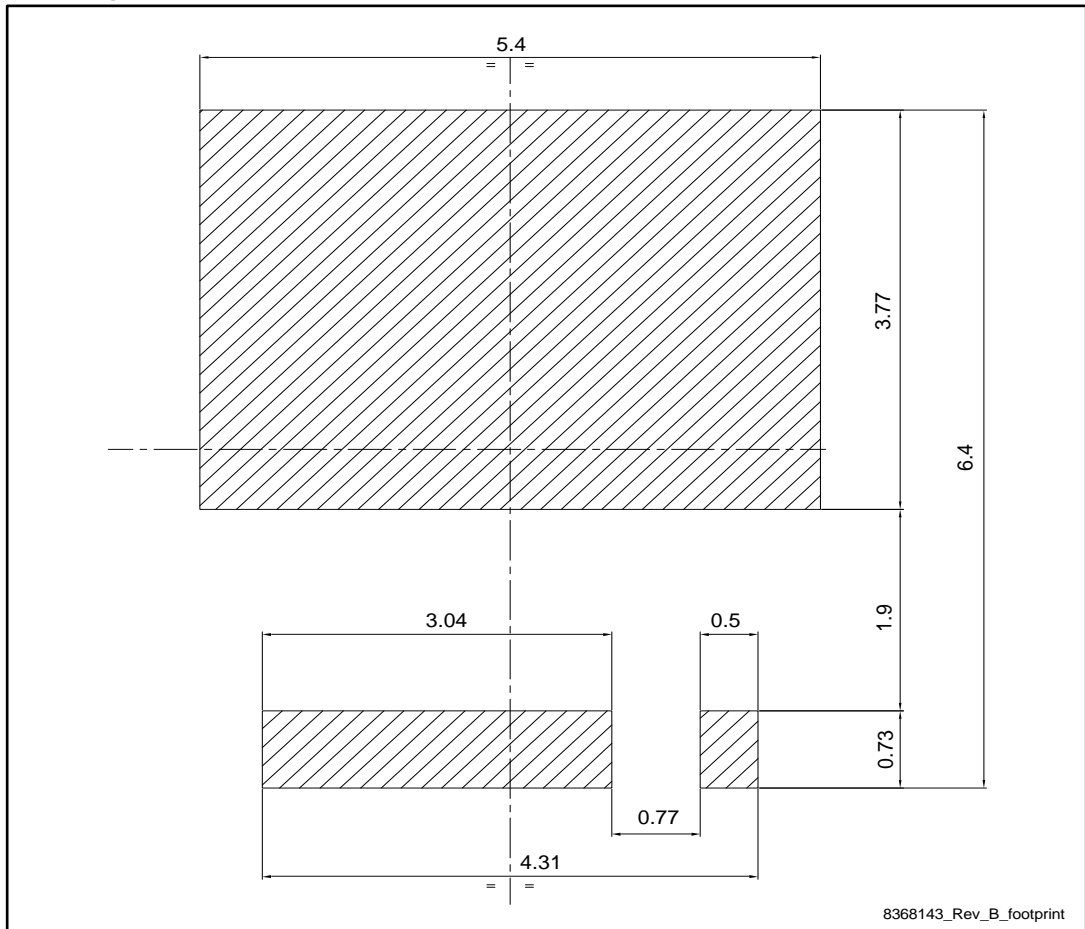


Table 10: PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21: PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



## 4.2 Packing information

Figure 22: PowerFLAT™ 5x6 tape (dimensions are in mm)

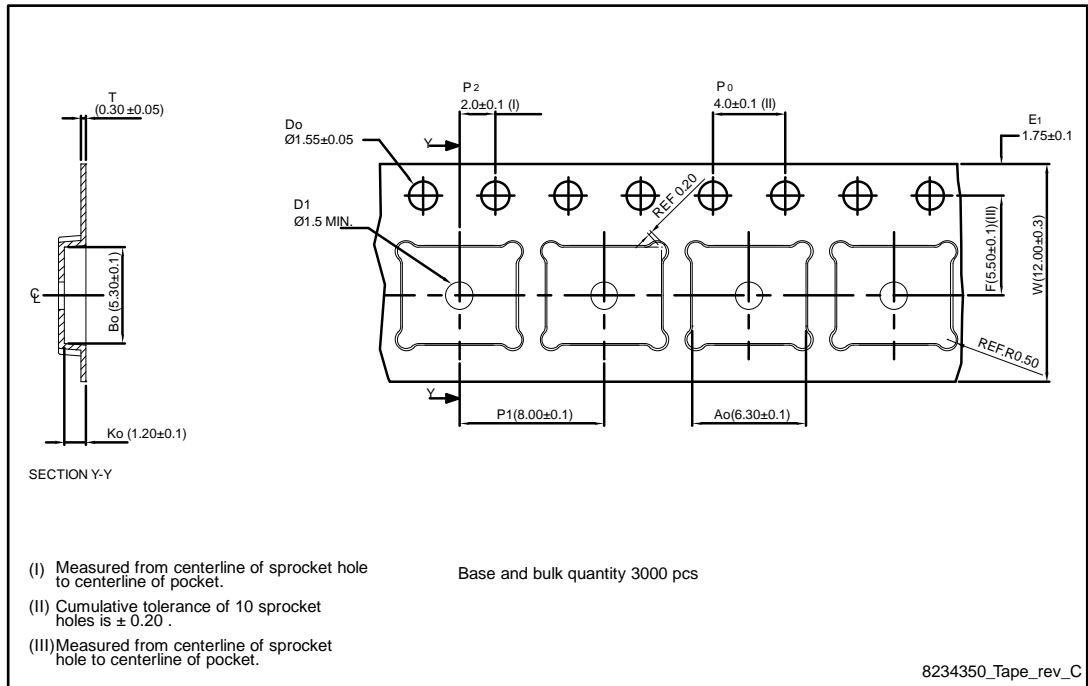


Figure 23: PowerFLAT™ 5x6 package orientation in carrier tape

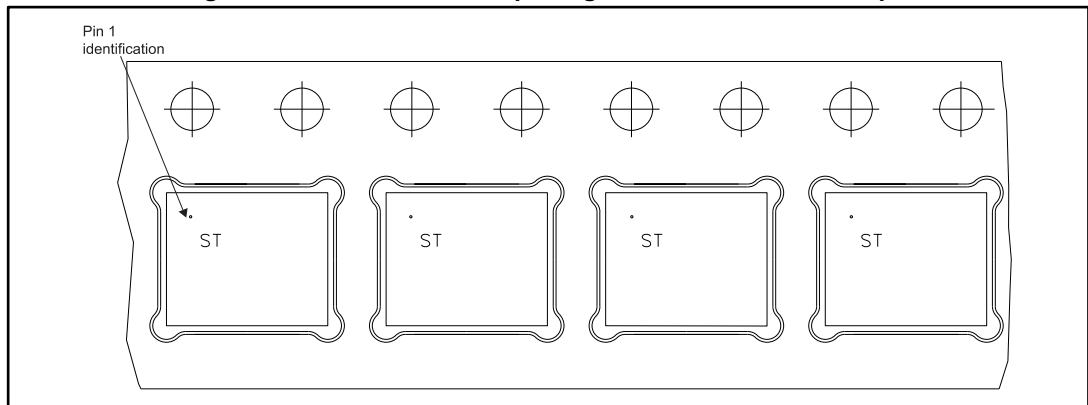
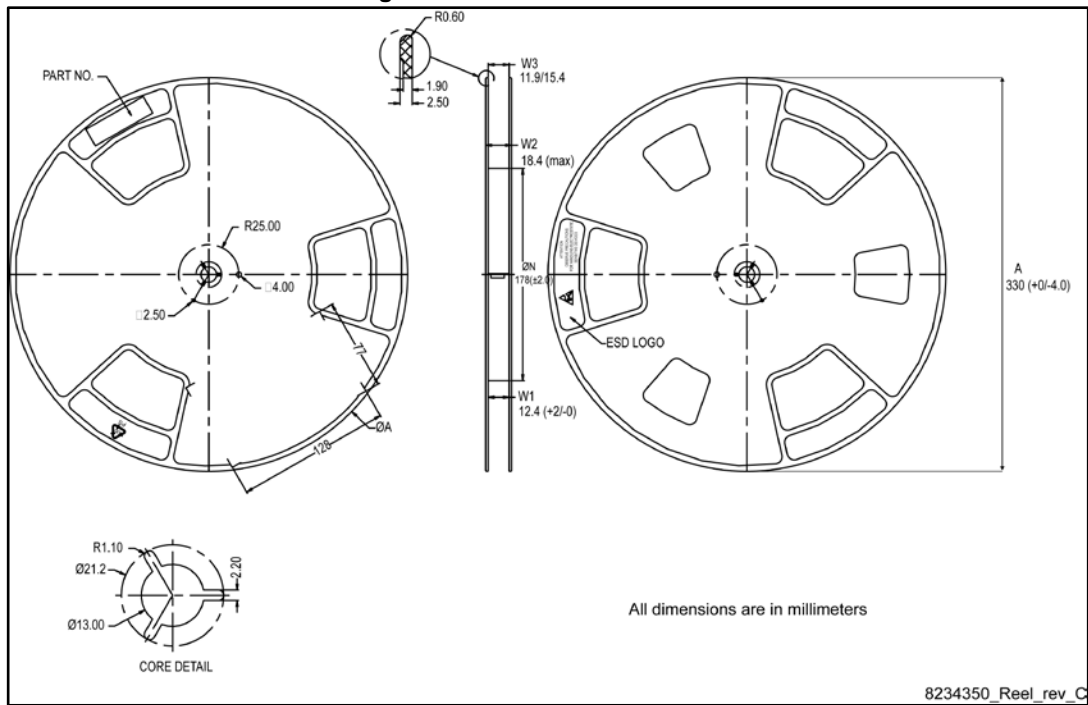


Figure 24: PowerFLAT™ 5x6 reel



## 5 Revision history

Table 11: Document revision history

Date	Revision	Changes
18-May-2015	1	First release.

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