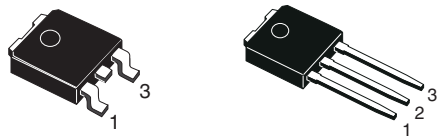
STD12NF06
STD12NF06T4

N-channel 60 V, 0.08Ω 12 A, DPAK, IPAK
STripFET™ II Power MOSFET

Features

Type	V_{DSSS}	$R_{DS(on)}$	I_D
STD12NF06	60V	<0.1Ω	12A
STD12NF06T4	60V	<0.1Ω	12A

- Exceptional dv/dt capability
- Low gate charge



DPAK IPAK

Applications

- Switching application

Description

This Power MOSFET is the latest development of STMicroelectronics unique "single feature size" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Figure 1. Internal schematic diagram

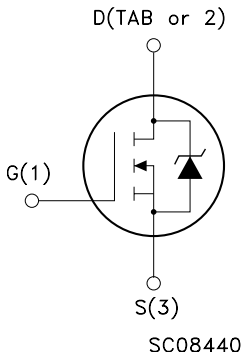


Table 1. Device summary

Order codes	Marking	Package	Packaging
STD12NF06T4T4	D12NF06	DPAK	Tape and reel
STD12NF06T4-1	D12NF06	IPAK	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20KΩ)	60	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25°C	12	A
I_D	Drain current (continuous) at T_C=100°C	8.5	A
I_{DM} (1)	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at T_C = 25°C	30	W
	Derating factor	0.2	W/°C
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
E_{AS} (3)	Single pulse avalanche energy	140	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_J	Max. operating junction temperature		

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 12$ A, di/dt ≤200 A/µs, $V_{DS} \leq V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
3. Starting T_J = 25 °C, I_D = 6 A, V_{DD} = 30 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case Max	5	°C/W
R_{thJA}	Thermal resistance junction-ambient Max	100	°C/W
T_l	Maximum lead temperature for soldering purpose	275	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 25mA, V_{GS} = 0	60			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C = 125°C			1 10	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ±20V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS}= V_{GS}, I_D = 250µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 6A		0.08	0.1	W

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 6A	-	5		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0	-	315 70 30		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 48V, I_D = 12A V_{GS} = 10V	-	10 3.0 3.5	12	nC nC nC

1. Pulsed: pulse duration=300 µs, duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 30V, I_D = 6A, R_G = 4.7Ω, V_{GS} = 10V *Figure 14 on page 8*	-	7 18 17 6	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD}	Source-drain current		-		12	A
I_{SDM}	Source-drain current (pulsed)		-		48	A
V_{SD} (1)	Forward on voltage	I_{SD} = 12A, V_{GS} = 0	-		1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 12A, di/dt = 100A/µs, V_{DD} = 30V, T_J = 150°C *Figure 16 on page 8*	-	50 65 3.5		ns nC A

1. Pulsed: pulse duration= 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

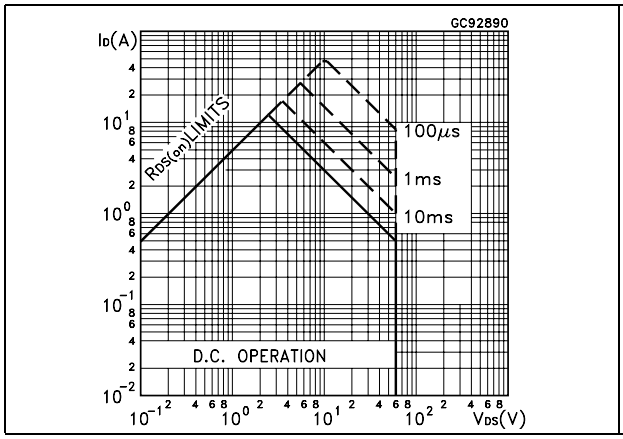


Figure 3. Thermal impedance

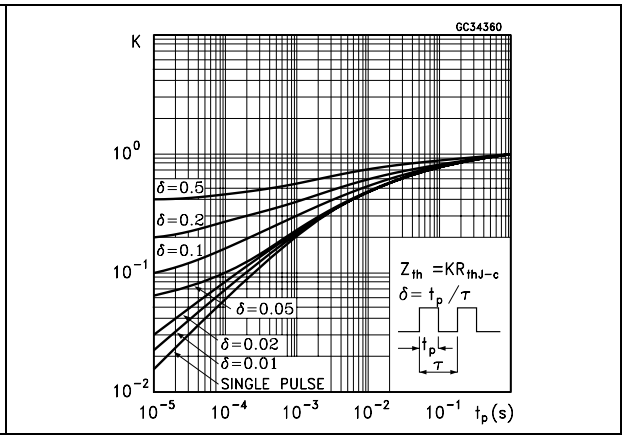


Figure 4. Output characteristics

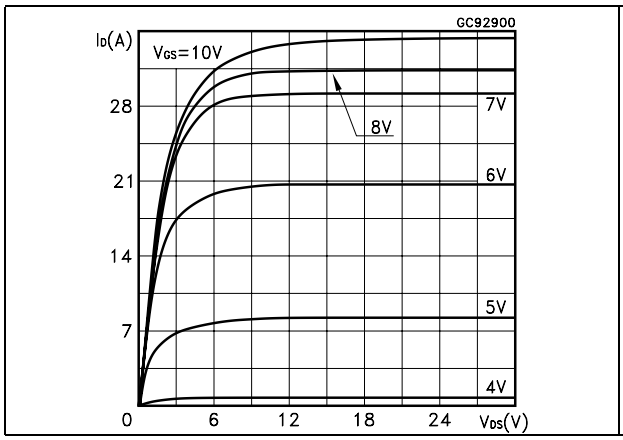


Figure 5. Transfer characteristics

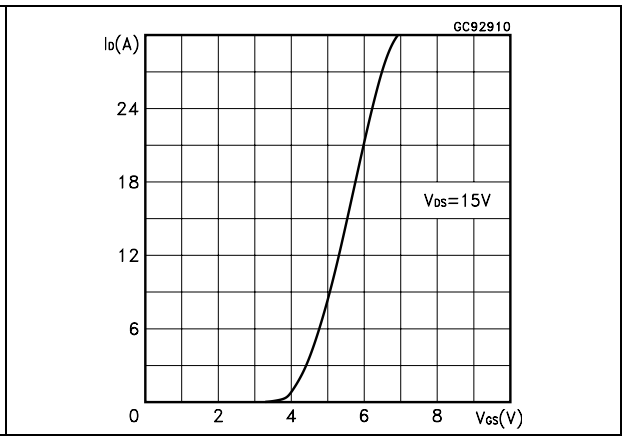


Figure 6. Transconductance

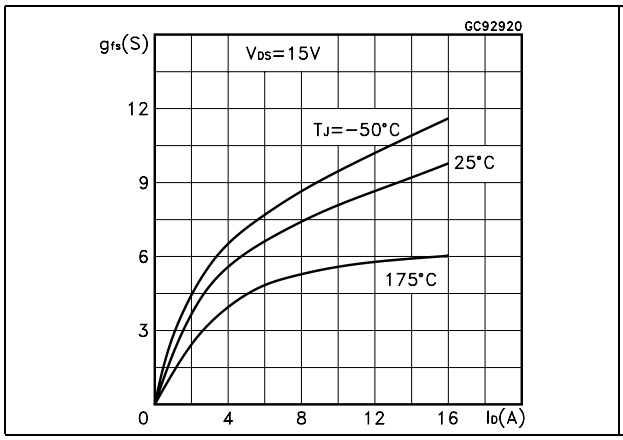


Figure 7. Static drain-source on resistance

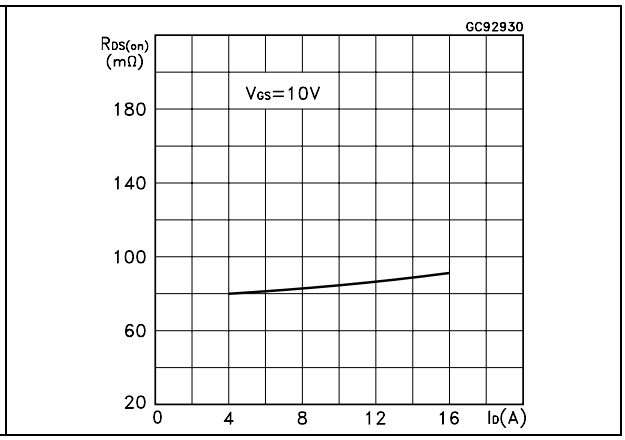


Figure 8. Gate charge vs. gate-source voltage

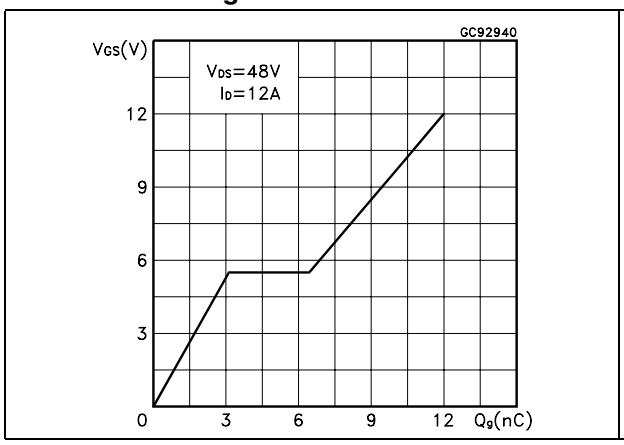


Figure 9. Capacitance variations

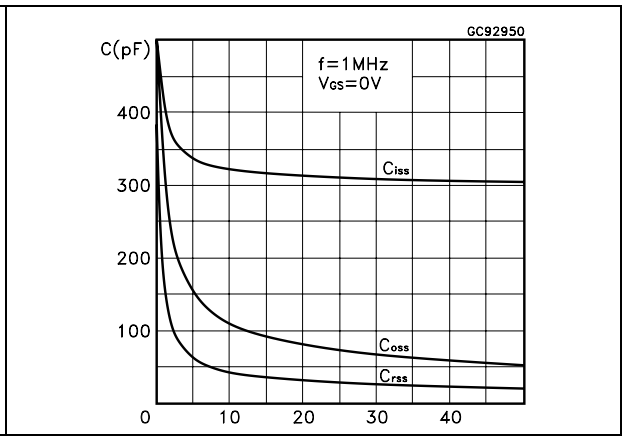


Figure 10. Normalized gate threshold voltage vs. temperature

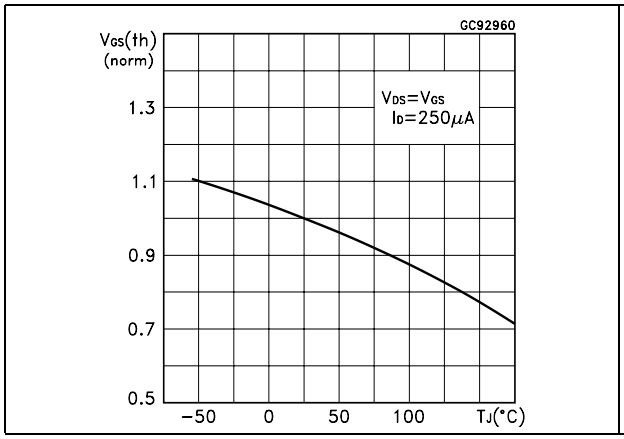


Figure 11. Normalized on resistance vs. temperature

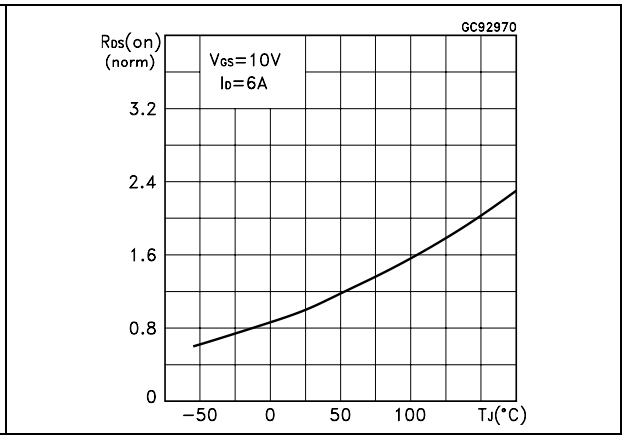


Figure 12. Source-drain diode forward characteristics

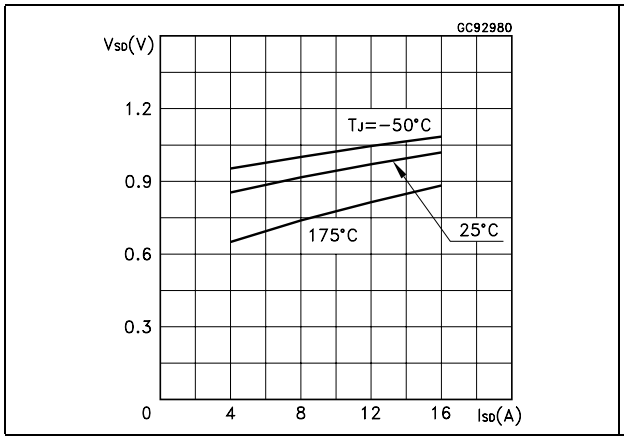
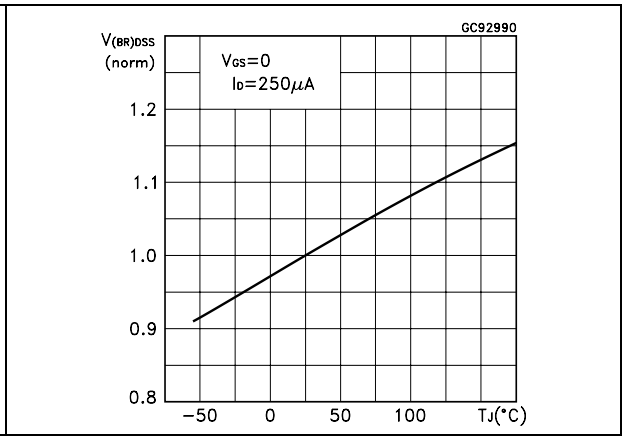


Figure 13. Normalized breakdown voltage vs. temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

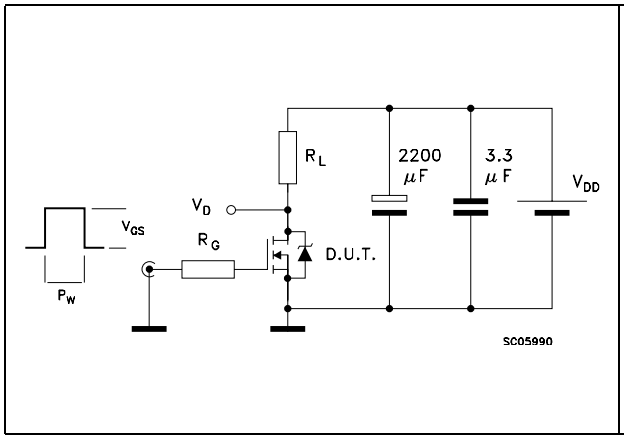


Figure 15. Gate charge test circuit

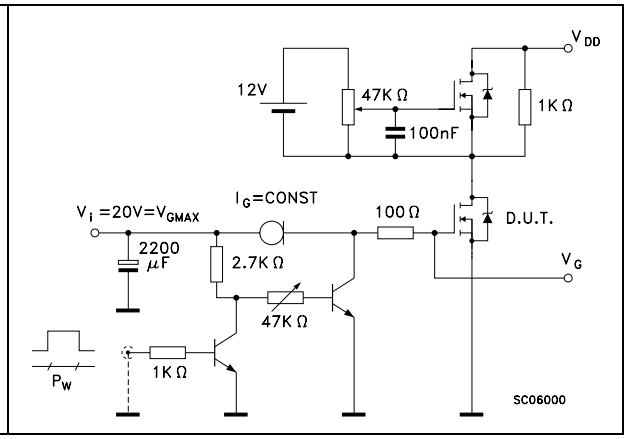


Figure 16. Test circuit for inductive load switching and diode recovery times

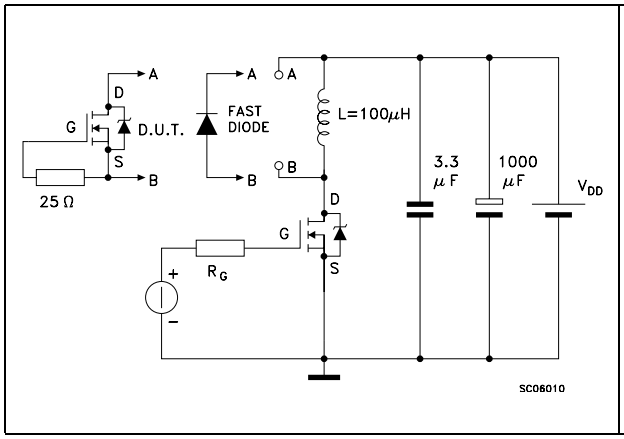


Figure 17. Unclamped inductive load test circuit

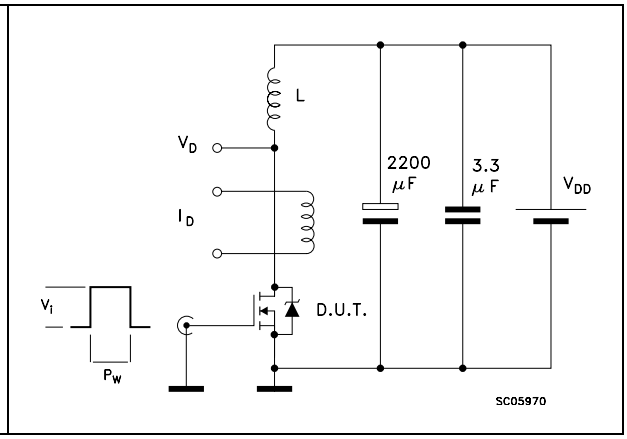
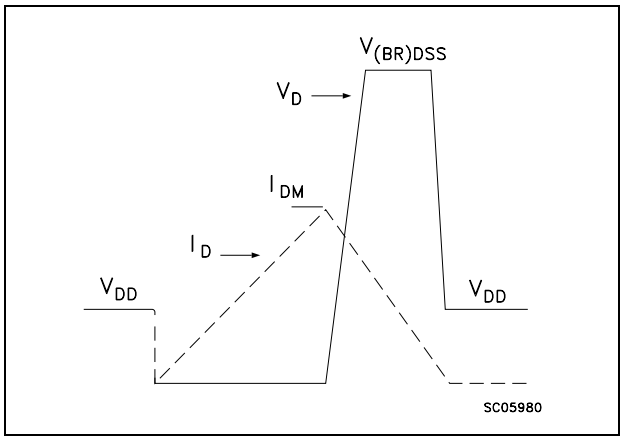


Figure 18. Unclamped inductive waveform

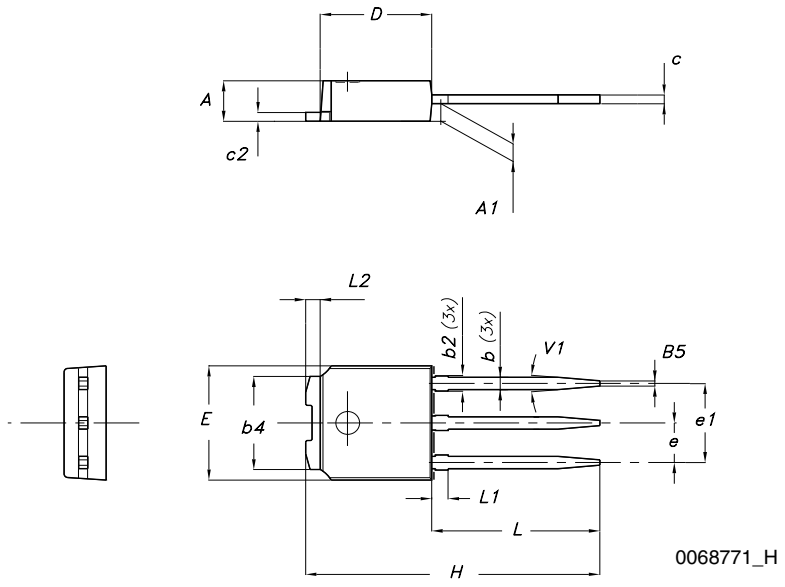


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

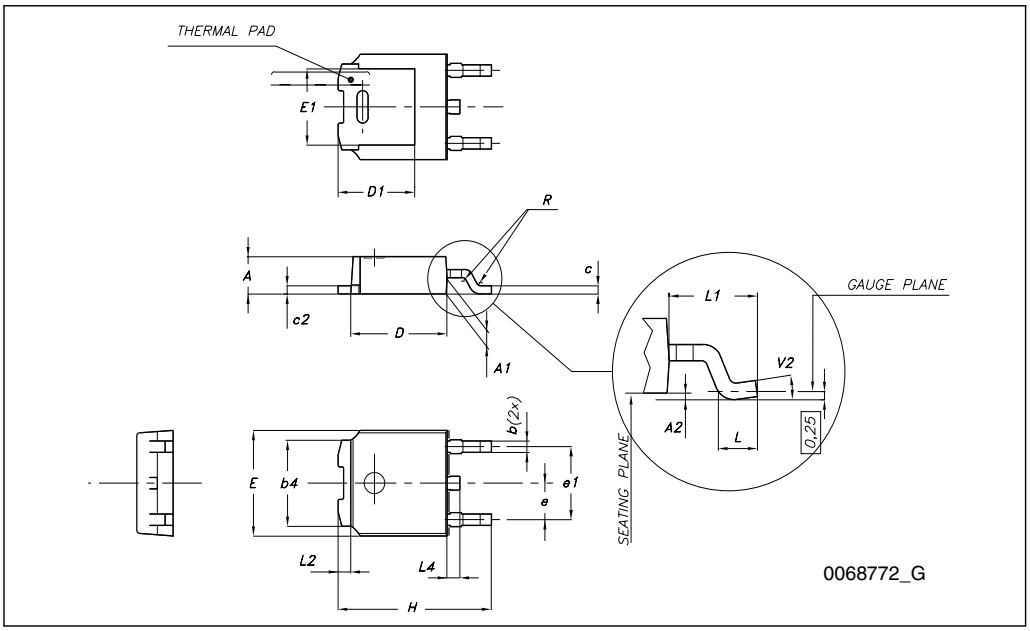
TO-251 (IPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
(L1)	0.80		1.20
L2		0.80	
V1		10 ^{o}	



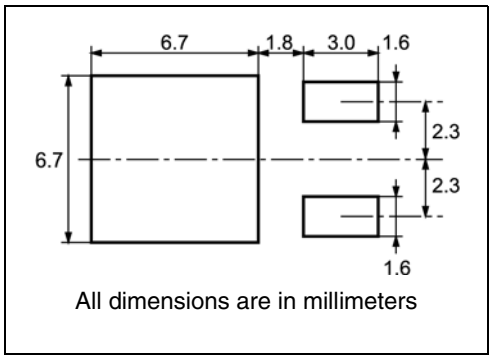
TO-252 (DPAK) mechanical data

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0 °		8 °



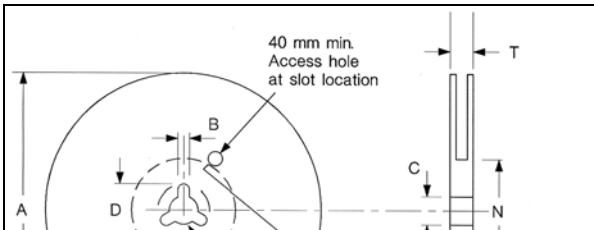
5 Packaging mechanical data

DPAK FOOTPRINT



All dimensions are in millimeters

TAPE AND REEL SHIPMENT



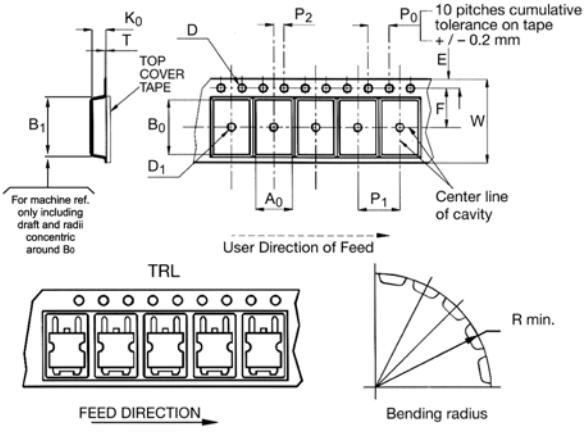
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
09-Sep-2004	3	Complete document
07-Aug-2006	4	The document has been reformatted
19-Feb-2007	5	Typo mistake on page 1
15-Apr-2009	6	*Table 1: Device summary* has been updated Mechanical data updated
26-Nov-2009	7	Updated Q_{rr} in *Table 7: Source drain diode*.