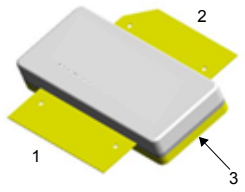
RF5L05750CF2

Datasheet

750 W, 50 V, HF to 500 MHz RF power LDMOS transistor



C2

Pin connection	
Pin	**Connection**
1	Gate
2	Drain
3	Source (bottom side)

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
RF5L05750CF2(1)	108 MHz	50 V	1500 W	20 dB	78%

1. *Measured on 88-108 MHz wideband test board with two RF5L05750CF2 devices connected in push-pull.*

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- Excellent thermal stability, low HCI drift
- In compliance with the european directive 2002/95/EC

Applications

- 30-88 MHz/136-174 MHz ground communication
- 1.6-30 MHz HF transceiver
- Plasma generator
- Particle accelerator
- FM and VHF TV broadcast

Description

The RF5L05750CF2 is a 750 W, 50 V, high performance, unmatched LDMOS FET, designed for wideband commercial and industrial applications in the frequency range from HF to 500 MHz. It can be used for both CW and pulse application. It is featured for high power and high ruggedness, suitable for industrial, scientific and medical application, as well as FM radio, VHF TV and aerospace applications.

Product status link
RF5L05750CF2

Product summary	
Order code	RF5L05750CF2
Marking	5L05750
Package	C2
Packing	Tape and reel 13"
Base/bulk quantity	100/100

1 Electrical ratings

Table 1. Absolute maximum ratings (T_C = 25 °C)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	110	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	55	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}(1)	Thermal resistance, junction-to-case	0.08	°C/W

1. *T_C = 85 °C , P_{OUT} = 1500 W, pulsed CW output at 108 MHz, two RF5L05750CF2 devices connected in push-pull.*

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS-002-2014)	C3

2 Electrical characteristics

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 100 µA	110			V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 50 V			1	µA
		V_{GS} = 0 V, V_{DS} = 90 V				
I_{GSS}	Gate-source leakage current	V_{GS} = -8/10 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = 50 V, I_D = 600 µA	2.3		2.9	V
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 50 V, I_D = 230 mA	2		5	V
$V_{DS(on)}$	Static drain-source on-voltage	V_{GS} = 10 V, I_D = 6 A			1	V
$I_{DS(on)}$	Static drain-source on-current	V_{GS} = 10 V, V_{DS} = 100 mV			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	V_{GS} = 10 V, V_{DS} = 100 mV			1	Ω

Table 5. Dynamic

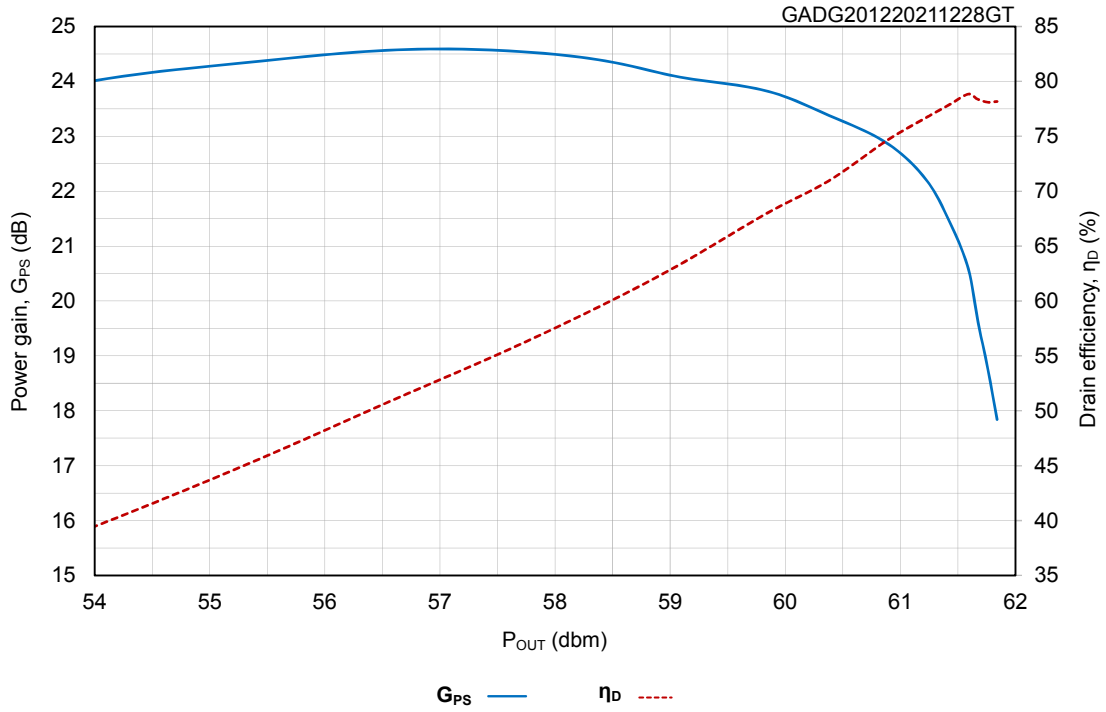
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
P_{OUT}	Output power	f = 108 MHz, pulsed CW, 3 dB compression	-	1500		W
G_{PS}	Power gain		-	20		dB
η_D	Drain efficiency		-	78		%
VSWR	Load mismatch	P_{OUT} = 1500 W, all phases	-		10:1	

Note: 1. *V_{DD} = 50 V, I_{DQ} = 200 mA, pulse width = 100 µs, duty cycle = 10%.*

2. *Measured on 88-108 MHz wideband test board with two RF5L05750CF2 devices connected in push-pull.*

3 Typical performances

Figure 1. Power gain and drain efficiency vs output power (f = 108 MHz)



Note: 1. *V_{DD} = 50 V, I_{DQ} = 200 mA, pulse width = 100 µs, duty cycle = 10%.*
2. *Measured on 88-108 MHz wideband test board with two RF5L05750CF2 devices connected in push-pull.*

4 Test circuits

Figure 2. **Test circuit layout (88–108 MHz frequency band)**

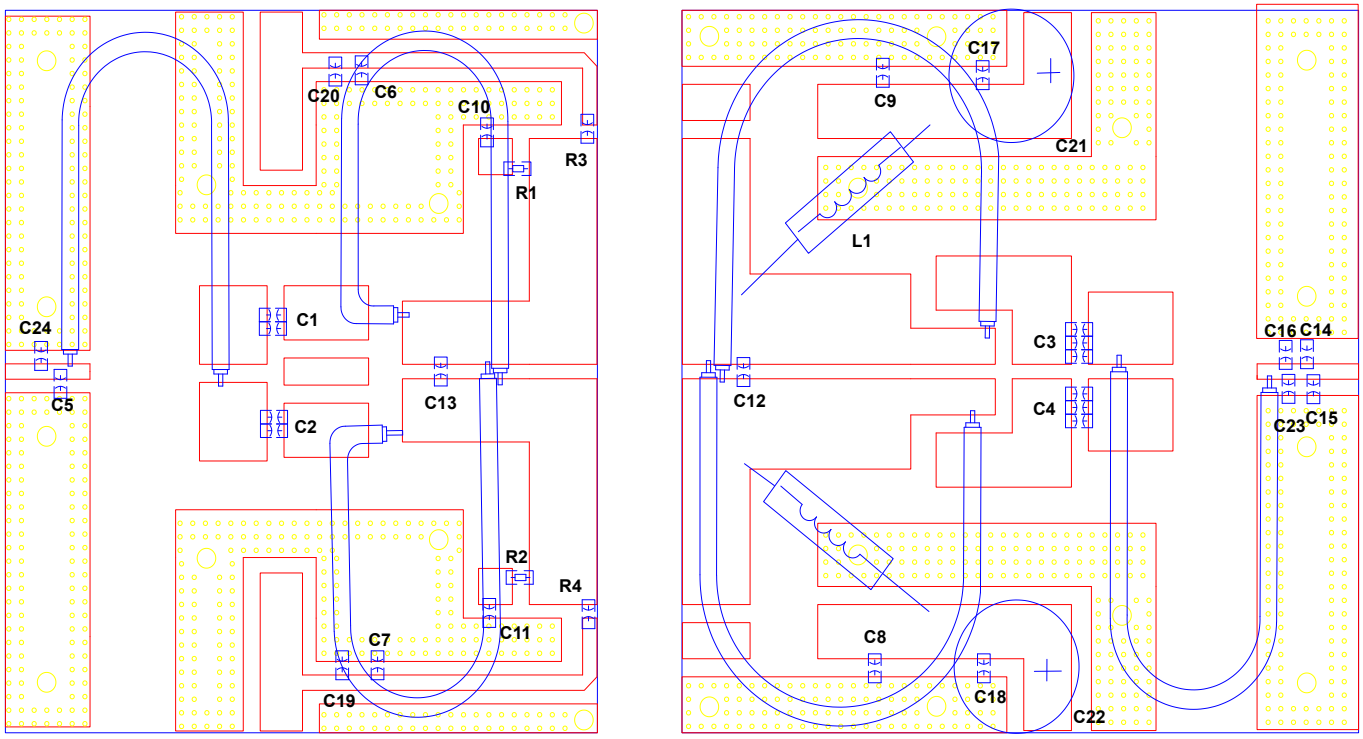


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Figure 3. **Test circuit photo**

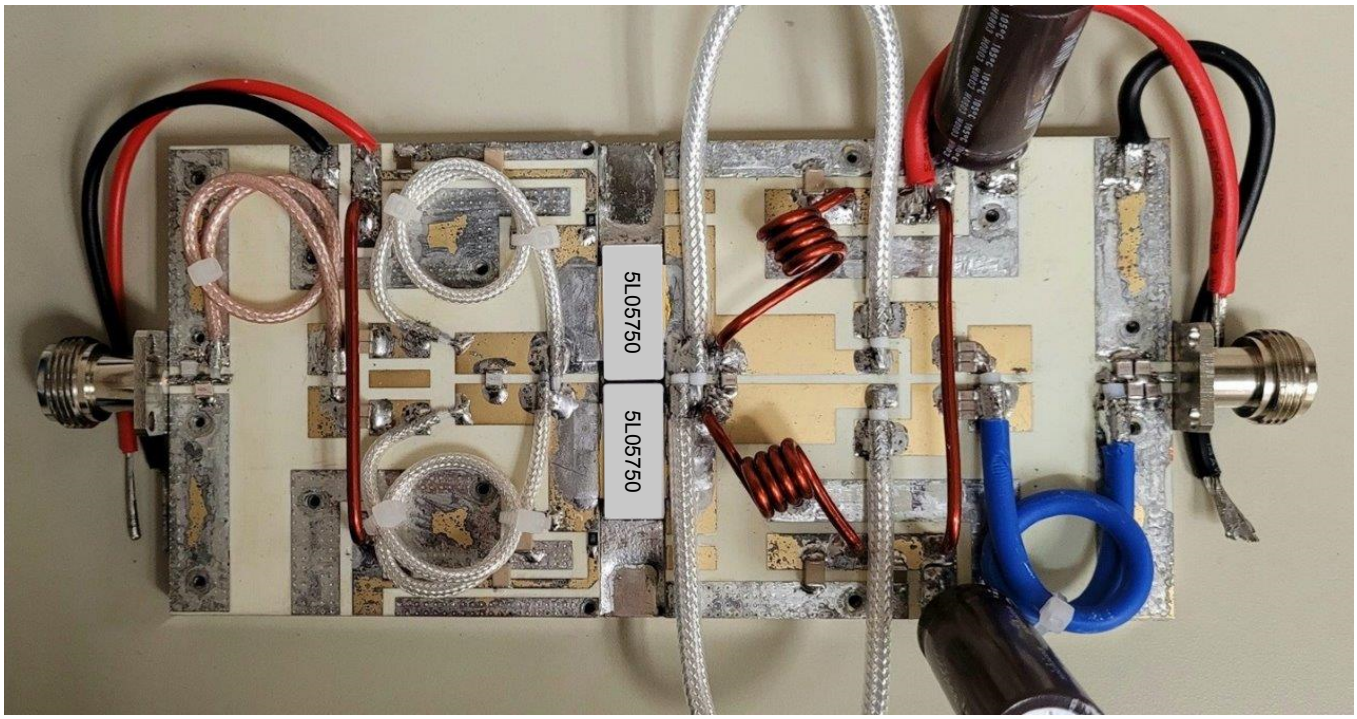

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Table 6. Components list

Component	Value	Reference
C1, C2	10 nF (2x)	C4532X7R3D103KT000N
C3, C4	470 pF (3x)	ATC800B
C5	27 pF	DLC70B
C6-C11	100 nF	C4532X7R3D103KT000N
C12	20 pF	DLC70B
C13	68 pF	ATC800B
C23, C14, C55, C16	3.9 pF	DLC70B
C17, C18, C19, C20	10 µF	100 V ceramic capacitor
C21, C22	2200 µF	63 V electrolitic capacitor
C24	10 pF	ATC800B
R1, R2	16 Ω	0805 chip resistor
R3, R4	470 Ω	0805 chip resistor
T1	50 Ω 150 mm	SFF-50-1.5
T2, T3	25 Ω line length =150 mm 9:1	SFF-25-1.5
T4, T5	12.5 Ω line length = 150 mm 9:1	SFF-12.5-1.5
T6	50 Ω 150 mm	RG402-3
L1, L2	4tums Φ1 mm	
PCB	0.762 mm (0.030") thick, εr = 3.48, Rogers RO4350B	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 C2 package information

Figure 4. **C2 package outline**

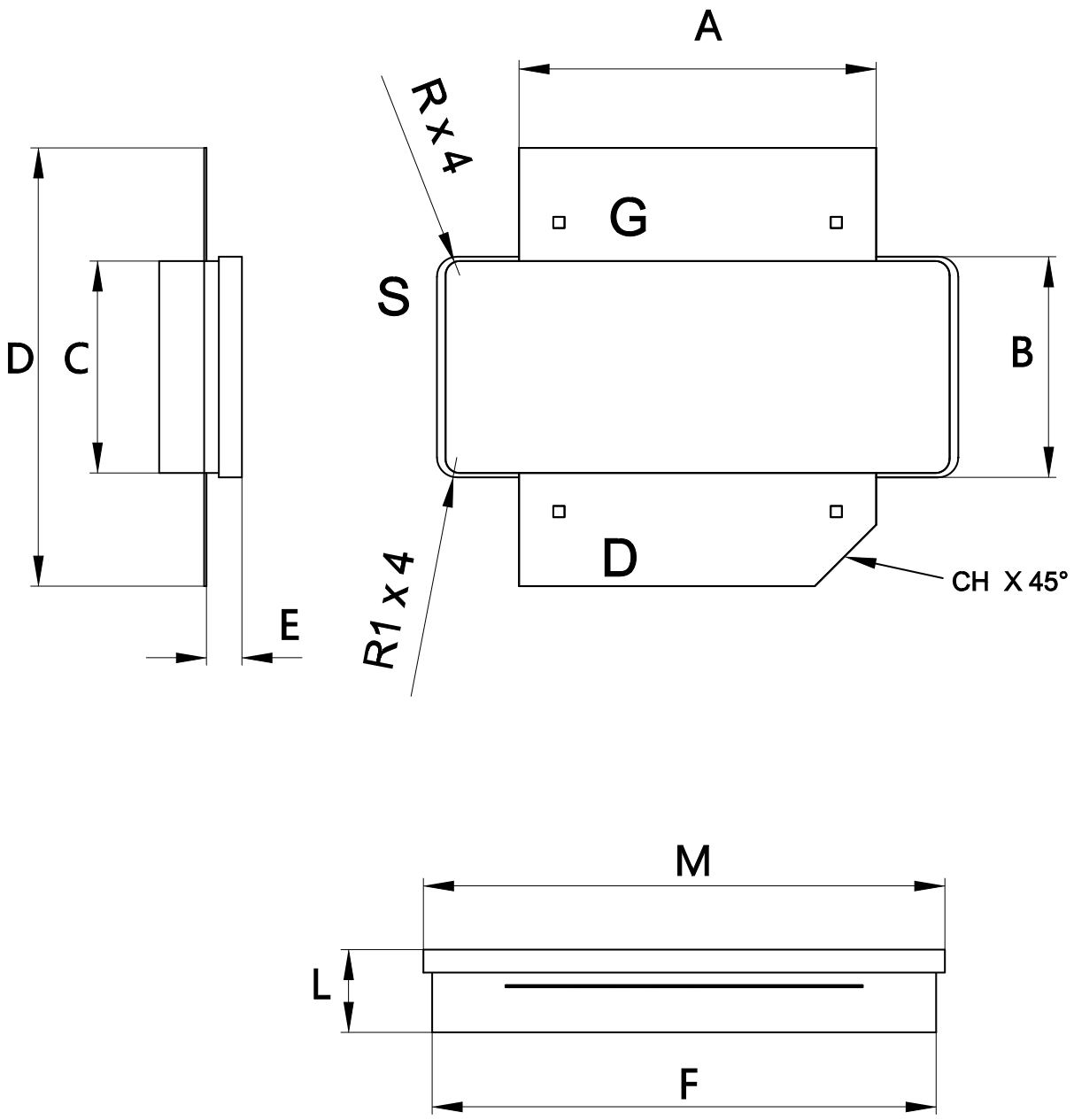

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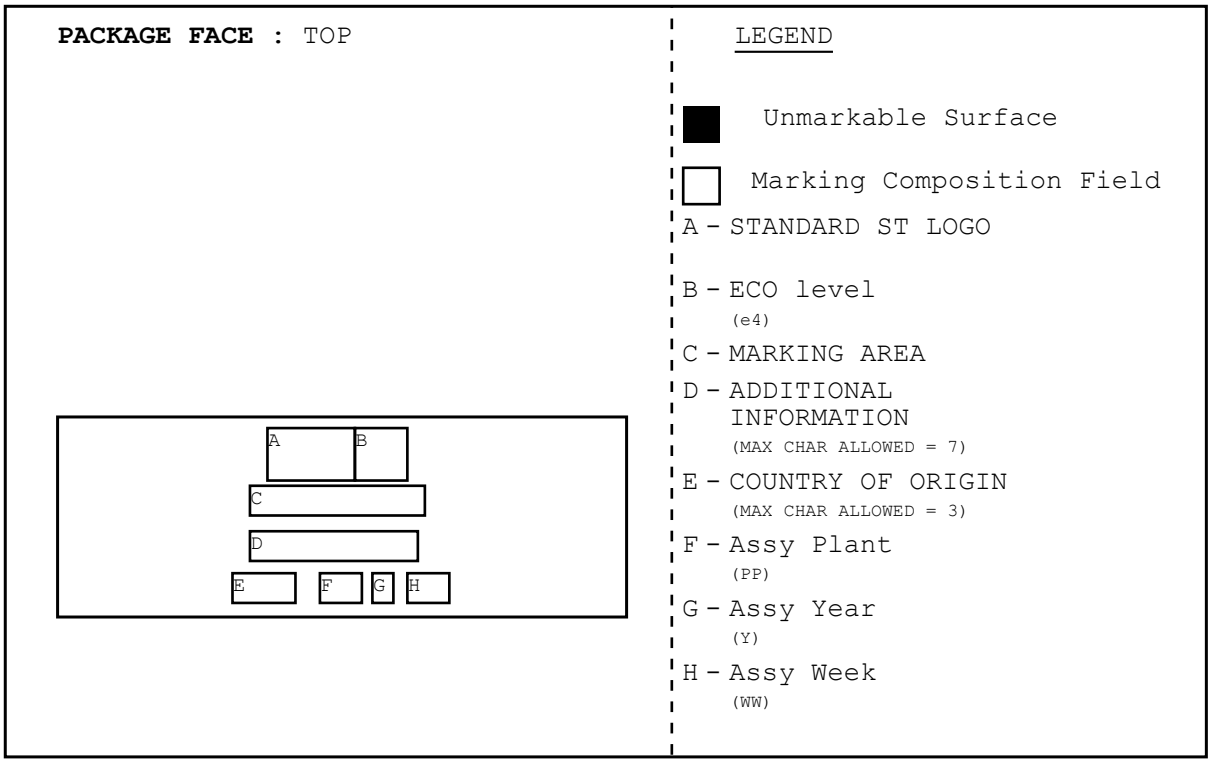
Table 7. **C2 package mechanical data**

Symbol	Millimeters		
	Min.	Typ.	Max.
A	15.713	15.840	15.967
B	9.653	9.780	9.907
C	9.273	9.400	9.527
D	19.303	19.430	19.557
E	1.443	1.570	1.697
F	22.223	22.350	22.477
L	3.543	3.670	3.797
M	22.993	23.120	23.247
CH		2.720	
R		0.630	
R1		0.880	

5.2 Marking information

Figure 5. **Marking composition**



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Revision history

Table 8. **Document revision history**

Date	Version	Changes
24-May-2021	1	First release.
22-Dec-2021	2	Updated Features and Description on cover page. Updated Table 1. Absolute maximum ratings (T_C = 25 °C) and Table 2. Thermal data. Updated Section 2 Electrical characteristics. Added Section 3 Typical performances and Section 4 Test circuits.

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