MJW3281A (NPN)
MJW1302A (PNP)

Complementary NPN-PNP Silicon Power Bipolar Transistors

The MJW3281A and MJW1302A are PowerBase™ power transistors for high power audio, disk head positioners and other linear applications.

Features

- Designed for 100 W Audio Frequency
- Gain Complementary:
  Gain Linearity from 100 mA to 7 A
  h_{FE} = 45 (Min) @ I_C = 8 A
- Low Harmonic Distortion
- High Safe Operation Area – 1 A/100 V @ 1 Second
- High f_T – 30 MHz Typical
- Pb–Free Packages are Available*

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	230	Vdc
Collector–Base Voltage	V_{CBO}	230	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector–Emitter Voltage – 1.5 V	V_{CEX}	230	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C	15 25	Adc
Base Current – Continuous	I_B	1.5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	200 1.43	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction–to–Case	$R_{\theta JC}$	0.625	°C/W
Thermal Resistance, Junction–to–Ambient	$R_{\theta JA}$	40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

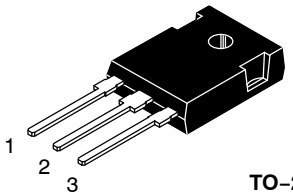
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

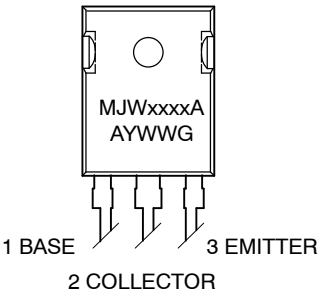
http://onsemi.com

15 AMPERES COMPLEMENTARY SILICON POWER TRANSISTORS 230 VOLTS 200 WATTS



TO–247
CASE 340L

MARKING DIAGRAM



xxxx = 3281 or 1302
A = Assembly Location
Y = Year
WW = Work Week
G = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJW3281A	TO–247	30 Units/Rail
MJW3281AG	TO–247 (Pb–Free)	30 Units/Rail
MJW1302A	TO–247	30 Units/Rail
MJW1302AG	TO–247 (Pb–Free)	30 Units/Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	230	–	–	Vdc
Collector Cutoff Current (V_{CB} = 230 Vdc, I_E = 0)	I_{CBO}	–	–	50	μAdc
Emitter Cutoff Current (V_{EB} = 5 Vdc, I_C = 0)	I_{EBO}	–	–	5	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector with Base Forward Biased (V_{CE} = 50 Vdc, t = 1 s (non−repetitive) (V_{CE} = 100 Vdc, t = 1 s (non−repetitive)	$I_{S/b}$	 4 1	 – –	 – –	Adc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{CE} = 5 Vdc) (I_C = 1 Adc, V_{CE} = 5 Vdc) (I_C = 3 Adc, V_{CE} = 5 Vdc) (I_C = 5 Adc, V_{CE} = 5 Vdc) (I_C = 7 Adc, V_{CE} = 5 Vdc) (I_C = 8 Adc, V_{CE} = 5 Vdc) (I_C = 15 Adc, V_{CE} = 5 Vdc)	h_{FE}	 50 50 50 50 50 45 12	 125 – – – 115 – 35	 200 200 200 200 200 – –	–
Collector−Emitter Saturation Voltage (I_C = 10 Adc, I_B = 1 Adc)	$V_{CE(sat)}$	–	0.4	2	Vdc
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	–	–	2	Vdc
DYNAMIC CHARACTERISTICS					
Current−Gain − Bandwidth Product (I_C = 1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)	f_T	–	30	–	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	–	–	600	pF

TYPICAL CHARACTERISTICS

PNP MJW1302A

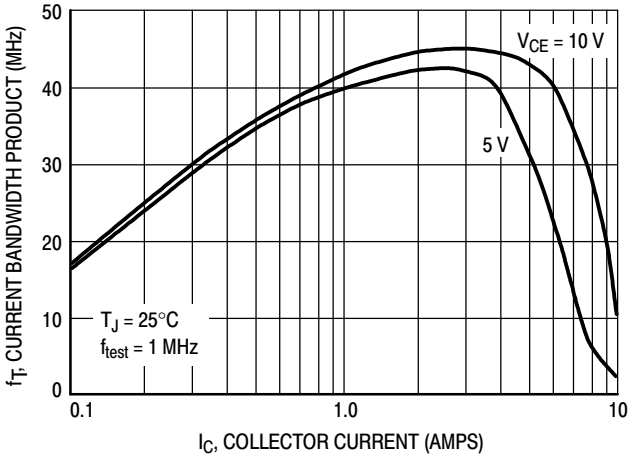


Figure 1. Typical Current Gain Bandwidth Product

NPN MJW3281A

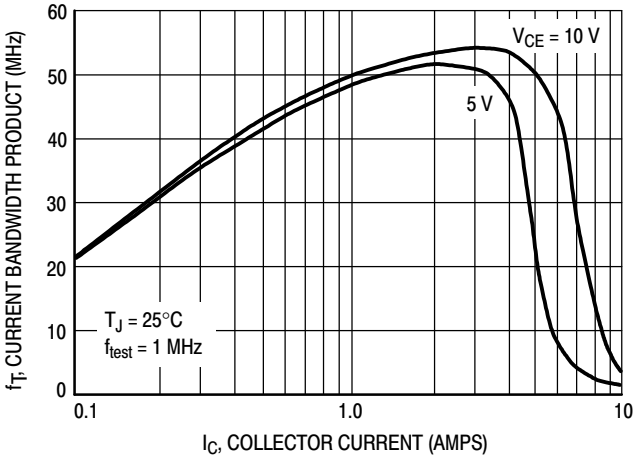


Figure 2. Typical Current Gain Bandwidth Product

PNP MJW1302A

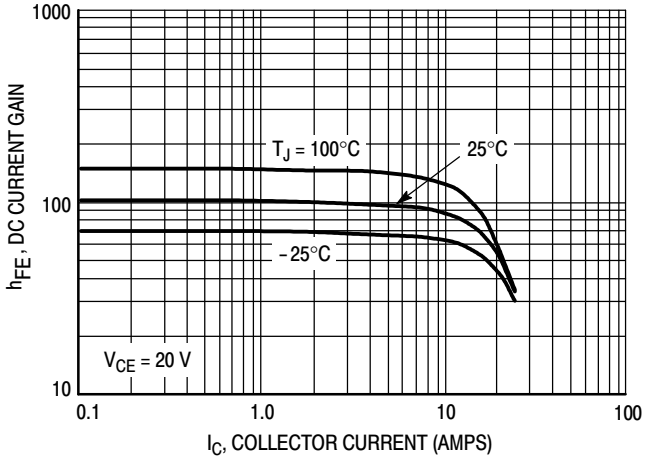


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJW3281A

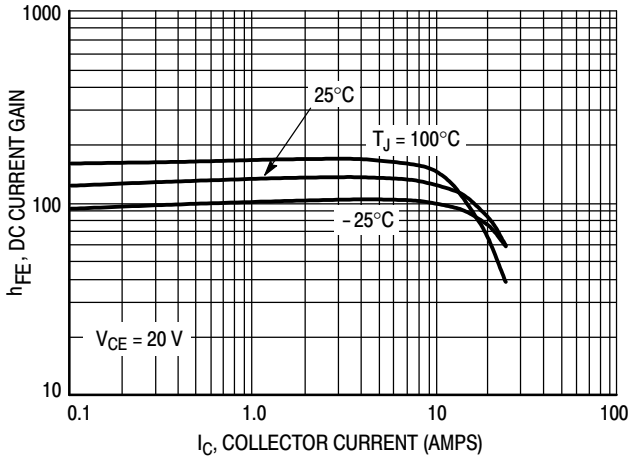


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJW1302A

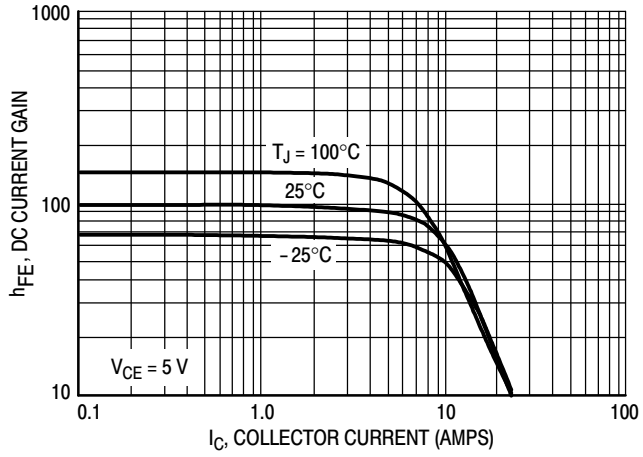


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJW3281A

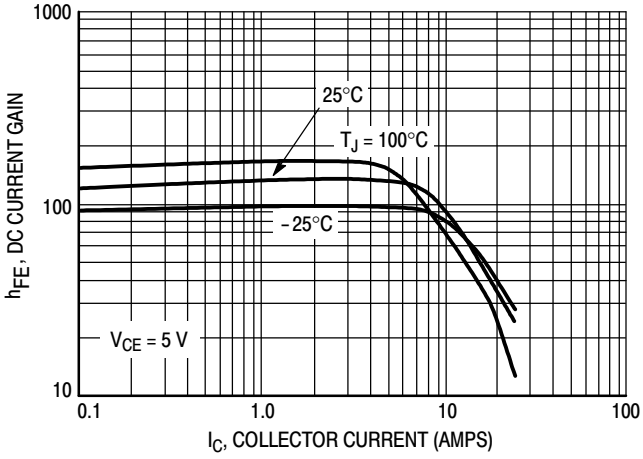


Figure 6. DC Current Gain, V_{CE} = 5 V

TYPICAL CHARACTERISTICS

PNP MJW1302A

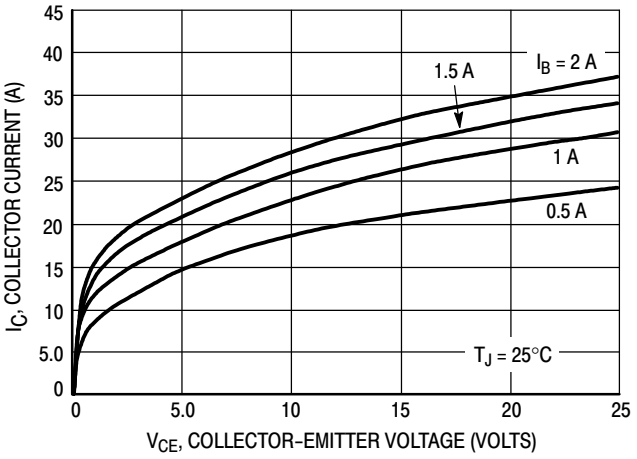


Figure 7. Typical Output Characteristics

NPN MJW3281A

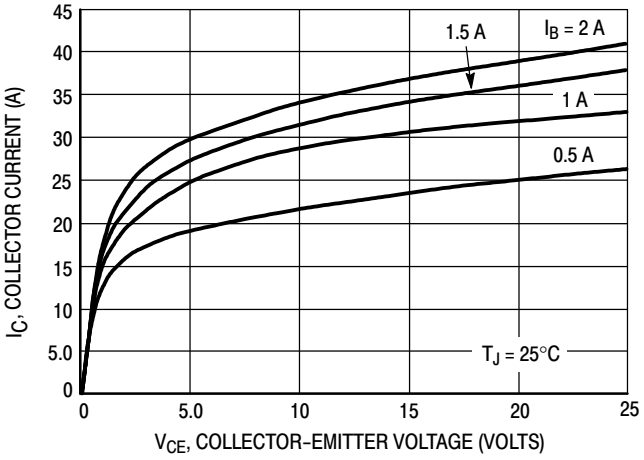


Figure 8. Typical Output Characteristics

PNP MJW1302A

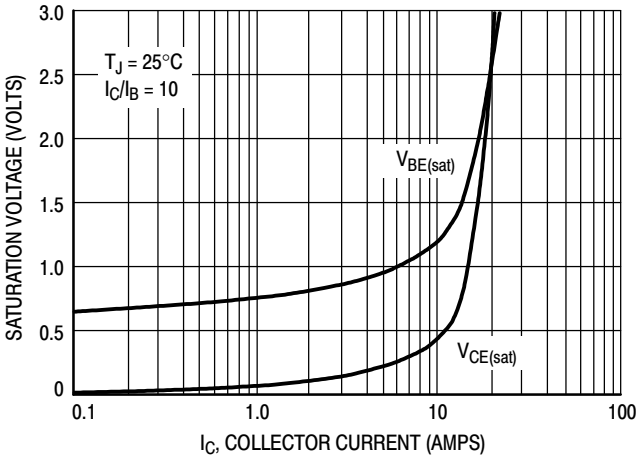


Figure 9. Typical Saturation Voltages

NPN MJW3281A

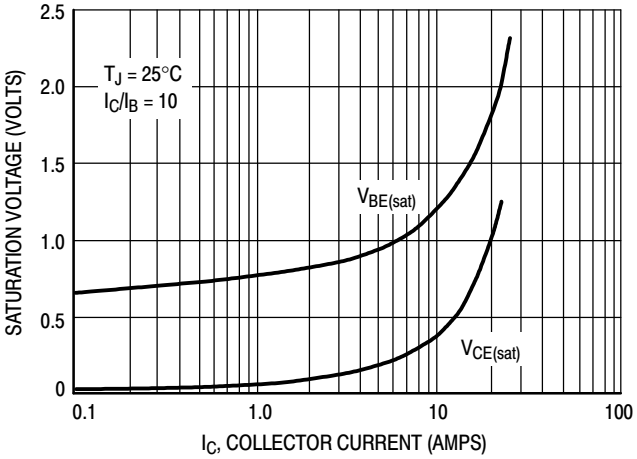


Figure 10. Typical Saturation Voltages

PNP MJW1302A

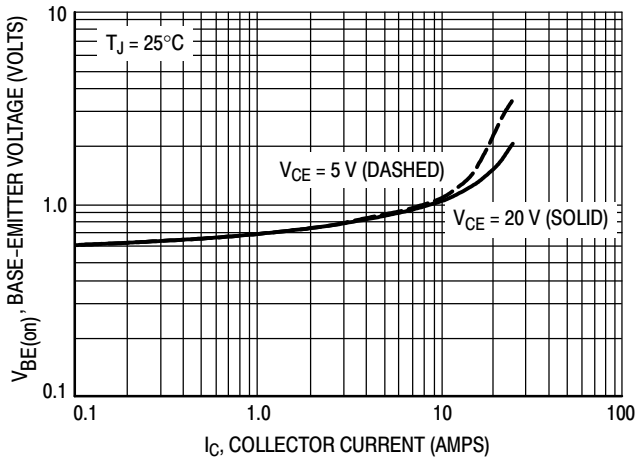


Figure 11. Typical Base−Emitter Voltage

NPN MJW3281A

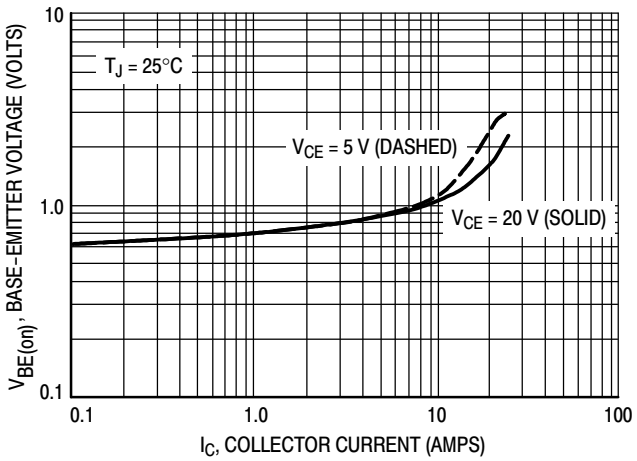


Figure 12. Typical Base−Emitter Voltage

PNP MJW1302A

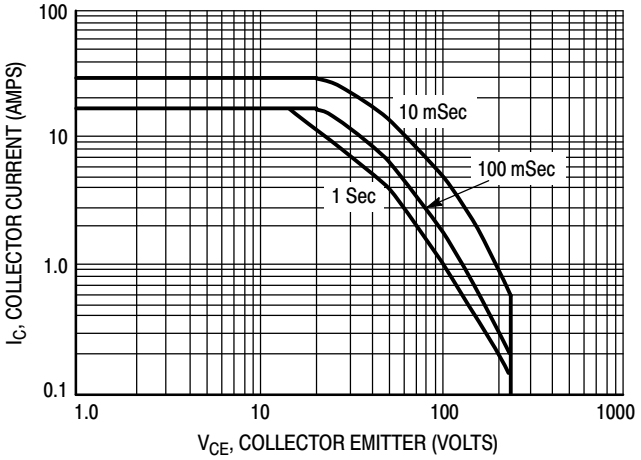


Figure 13. Active Region Safe Operating Area

NPN MJW3281A

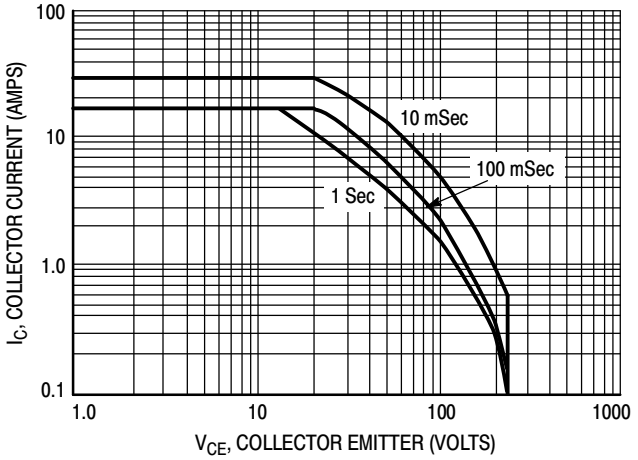


Figure 14. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 13 and 14 is based on $T_{J(pk)} = 150°C$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

PNP MJW1302A

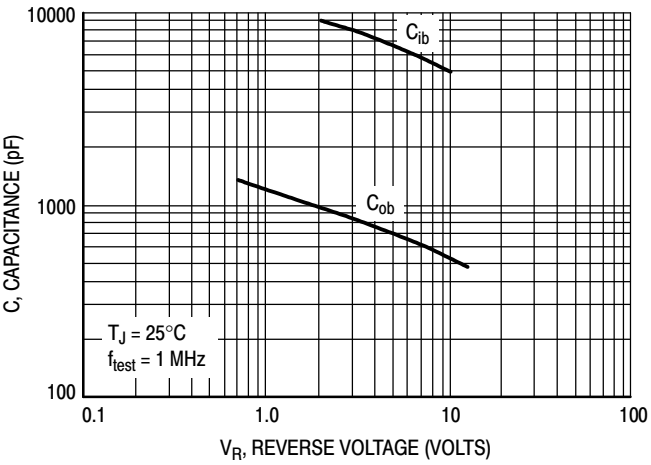


Figure 15. MJW1302A Typical Capacitance

NPN MJW3281A

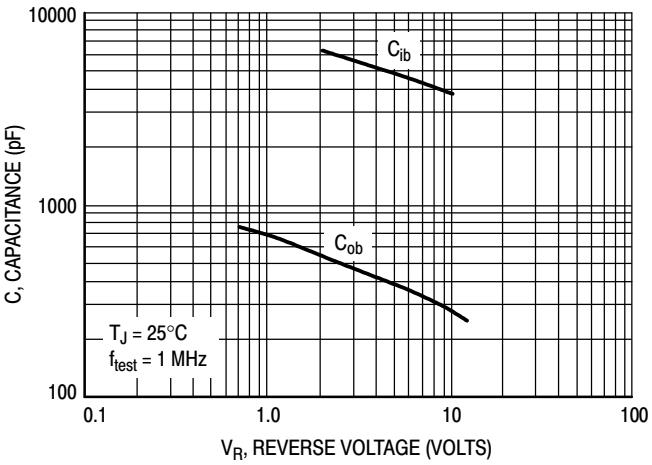


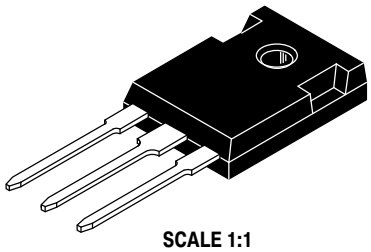
Figure 16. MJW3281A Typical Capacitance

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

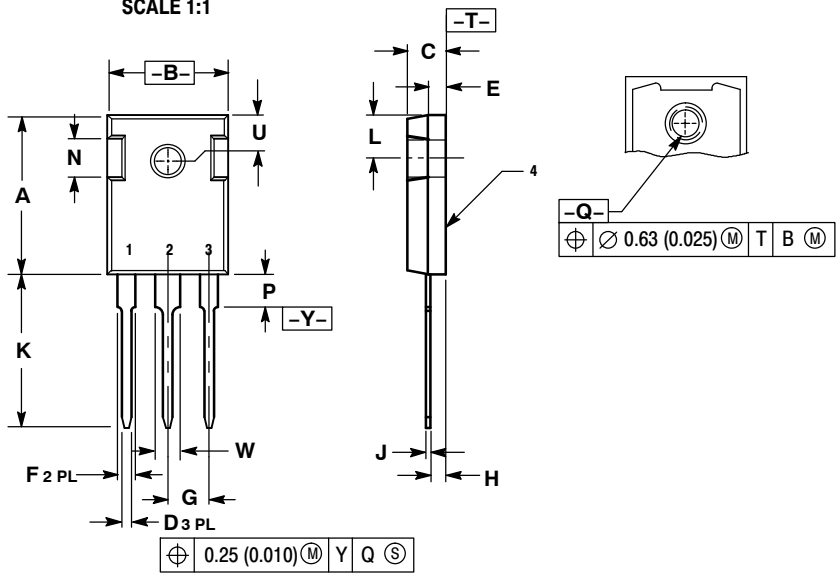
ON Semiconductor®

TO−247
CASE 340L−02
ISSUE F

DATE 26 OCT 2011



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

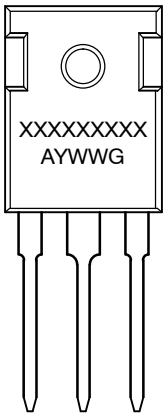
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB15080C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TO−247	PAGE 1 OF 2

ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80–21.46/0.819–0.845. DIM K WAS 19.81–20.32/0.780–0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊