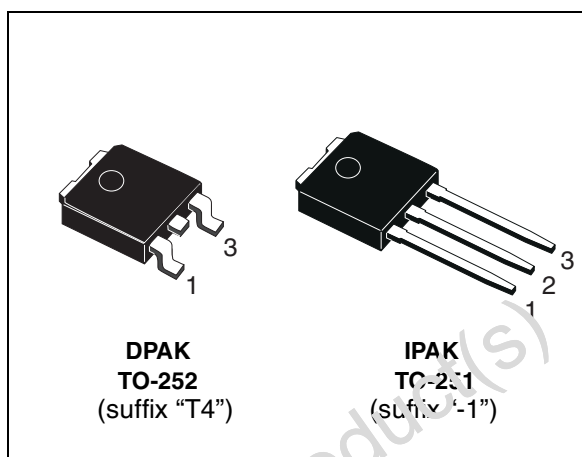


## High voltage fast-switching NPN power transistor

### Features

- High voltage capability
- Low spread of dynamic parameters
- Minimum lot-to-lot spread for reliable operation
- Very high switching speed
- Large RBSOA
- Through hole TO-251 (IPAK) power package in tube (suffix "-1")
- Surface mounting TO-252 (DPAK) power package in tape & reel (suffix "T4")
- Integrated antiparallel collector-emitter diode



### Applications

- Electronic ballast for fluorescent lighting
- Flyback and forward single transistor low power converters

### Description

The device is manufactured using high voltage Multi Epitaxial Planar technology for high switching speeds and medium voltage capability. It uses a cellular emitter structure with planar edge termination to enhance switching speeds while maintaining the wide RBSOA. The device is designed for use in lighting applications and low cost switch-mode power supplies.

Figure 1. Internal schematic diagram

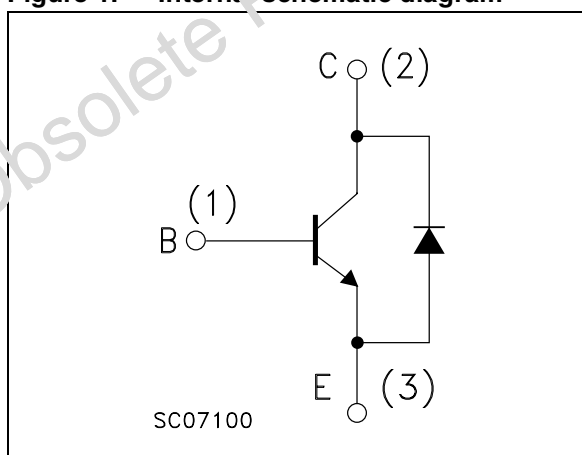


Table 1. Device summary

Order code	Marking	Package	Packaging
STLD128DNT4	LD128DN	TO-252 (DPAK)	Tape and reel
STLD128DN-1	LD128DN	TO-251 (IPAK)	Tube

# Content

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{CES}$	Collector-emitter voltage ( $V_{BE} = 0$ )	700	V
$V_{CEO}$	Collector-emitter voltage ( $I_B = 0$ )	400	V
$V_{EBO}$	Base-emitter voltage ( $I_C = 0$ , $I_B = 2A$ , $t_p < 10 \mu s$ )	$V_{(BR)EBO}$	V
$I_C$	Collector current	3	A
$I_{CM}$	Collector peak current ( $t_p < 5ms$ )	6	A
$I_B$	Base current	1.5	A
$I_{BM}$	Base peak current ( $t_p < 5ms$ )	3	A
$P_{TOT}$	Total dissipation at $T_c = 25 \text{ }^\circ\text{C}$	20	W
$T_{stg}$	Storage temperature	-65 to 150	$^\circ\text{C}$
$T_J$	Max. operating junction temperature	150	$^\circ\text{C}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	6.25	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C/W}$

## 2 Electrical characteristics

(T<sub>case</sub> = 25°C unless otherwise specified)

**Table 4. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{CES}$	Collector cut-off current ( $V_{BE} = 0$ )	$V_{CE} = 700\text{ V}$			100	$\mu\text{A}$
		$V_{CE} = 700\text{ V}$ $T_c = 125\text{ }^\circ\text{C}$			500	$\mu\text{A}$
$I_{CEO}$	Collector cut-off current ( $I_B = 0$ )	$V_{CE} = 400\text{ V}$			250	$\mu\text{A}$
$V_{(BR)EBO}$	Emitter-base breakdown voltage ( $I_C = 0$ )	$I_E = 10\text{ mA}$	9		18	V
$V_{CEO(sus)}^{(1)}$	Collector-emitter sustaining voltage ( $I_C = 0$ )	$I_C = 10\text{ mA}$	400			V
$V_{CE(sat)}^{(1)}$	Collector-emitter saturation voltage	$I_C = 1\text{ A}$ $I_B = 0.2\text{ A}$			1	V
		$I_C = 2\text{ A}$ $I_B = 0.4\text{ A}$			1.5	V
$V_{BE(sat)}^{(1)}$	Base-emitter saturation voltage	$I_C = 1\text{ A}$ $I_B = 0.2\text{ A}$			1.2	V
		$I_C = 2\text{ A}$ $I_B = 0.4\text{ A}$			1.3	V
$h_{FE}^{(1)}$	DC current gain	$I_C = 10\text{ mA}$ $V_{CE} = 5\text{ V}$	10			
		$I_C = 2\text{ A}$ $V_{CE} = 5\text{ V}$	8			
$V_f$	Diode forward voltage	$I_C = 1\text{ A}$			2.5	V
$t_s$ $t_f$	Resistive load Storage time	$I_C = 1\text{ A}$ $I_{B1} = -I_{B2} = 0.2\text{ A}$ $V_{CC} = 125\text{ V}$ $t_p = 20\text{ }\mu\text{s}$			4.5	$\mu\text{s}$
	Fall time				0.4	$\mu\text{s}$

1. Pulsed duration = 300 ms, duty cycle  $\leq 1.5\%$ .

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

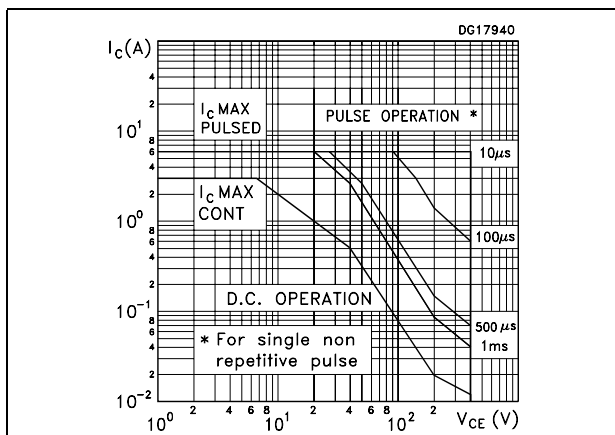


Figure 3. Derating curve

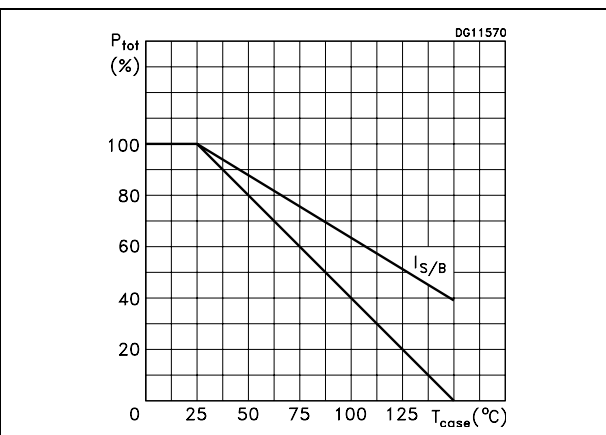


Figure 4. DC current gain

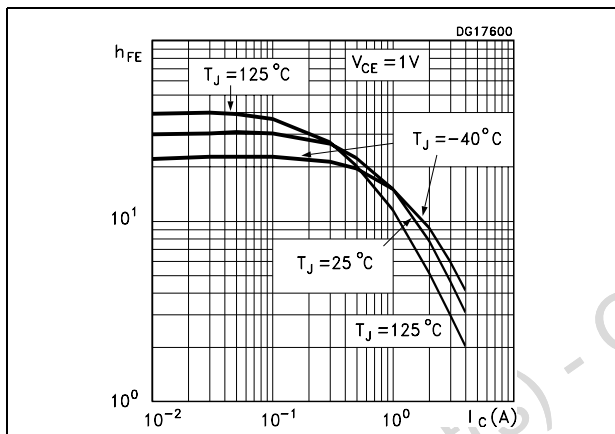


Figure 5. DC current gain

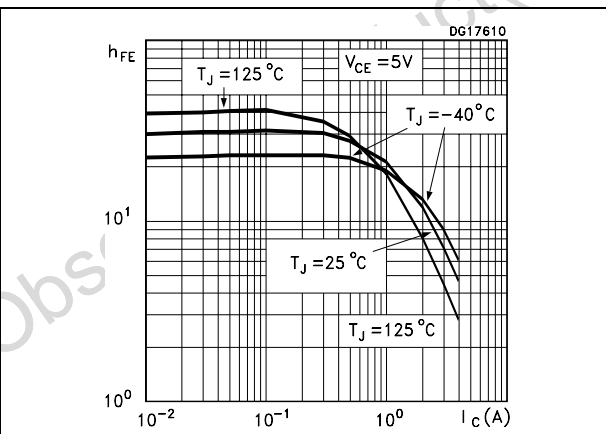


Figure 6. Collector-emitter saturation voltage

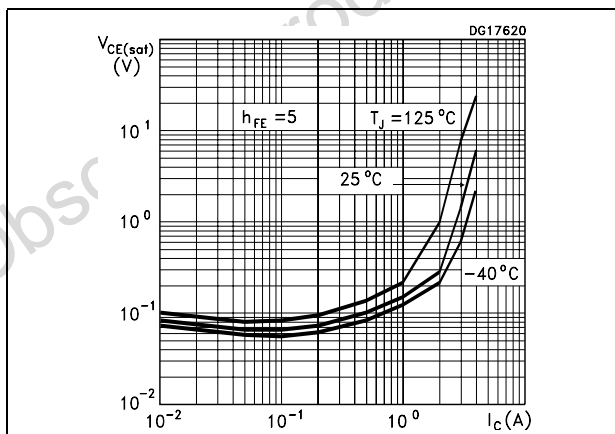


Figure 7. Base-emitter saturation voltage

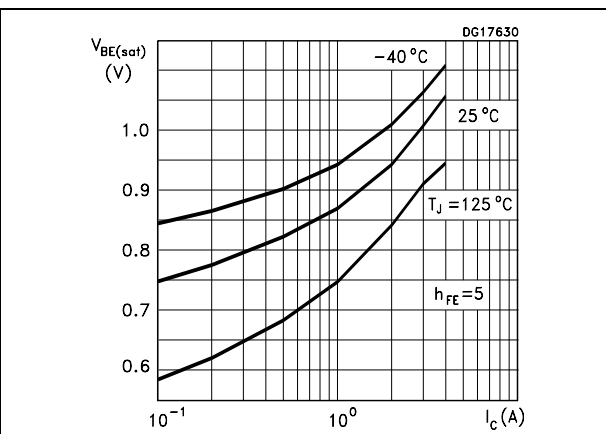


Figure 8. Freewheel diode forward voltage

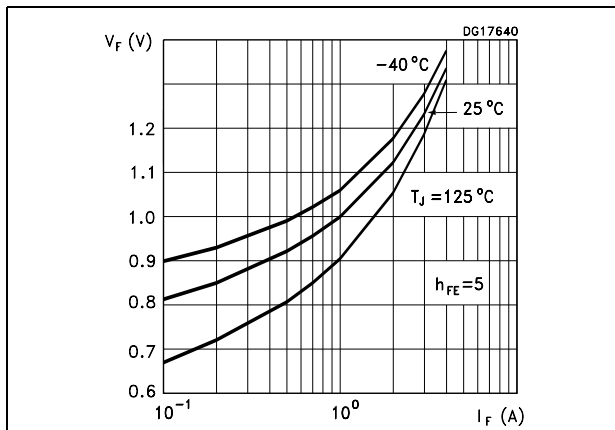


Figure 9. Resistive load switching time

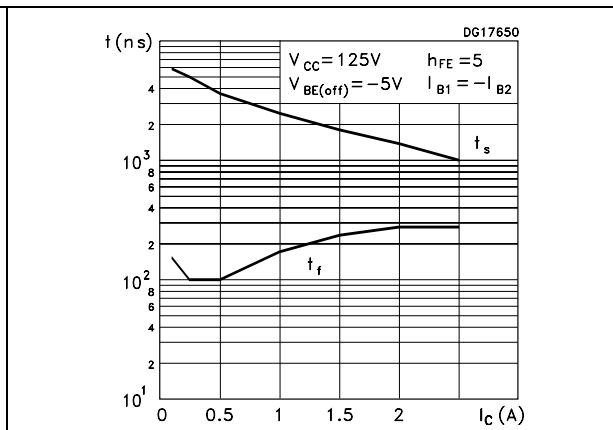
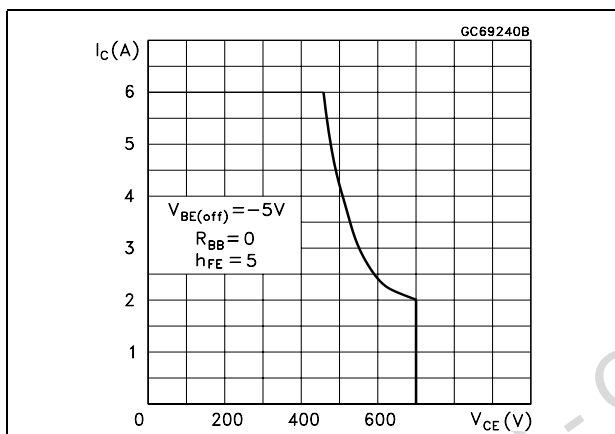


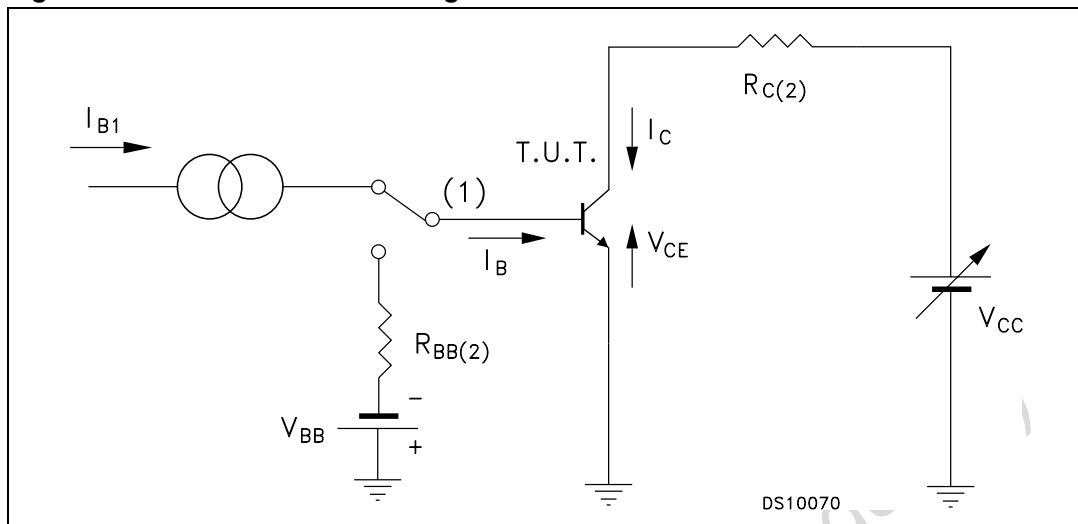
Figure 10. Reverse biased safe operating area



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### 3 Test circuit

Figure 11. Resistive load switching test circuit



- 1. Fast electronic switch
- 2. Non-inductive resistor

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## 4 Package mechanical data

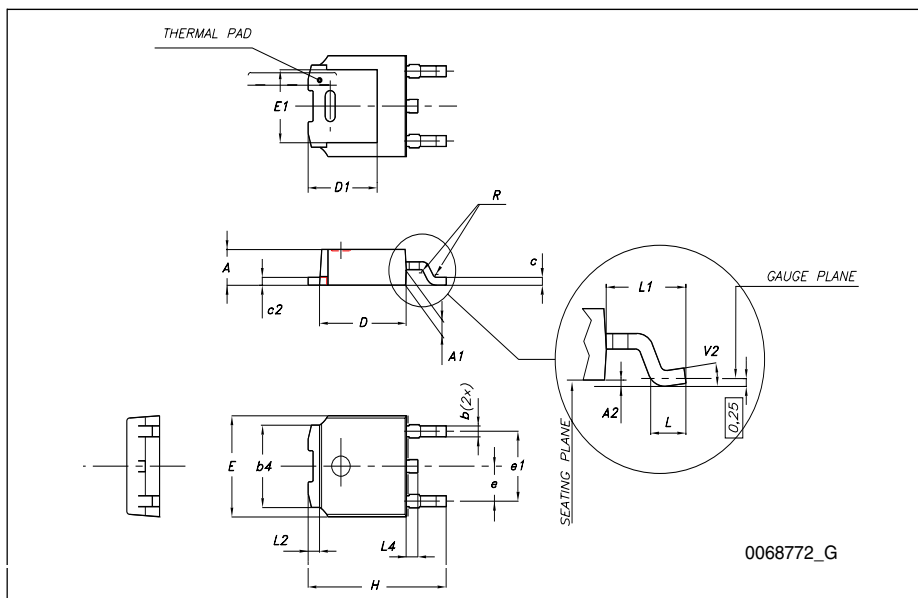
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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TO-252 (DPAK) mechanical data

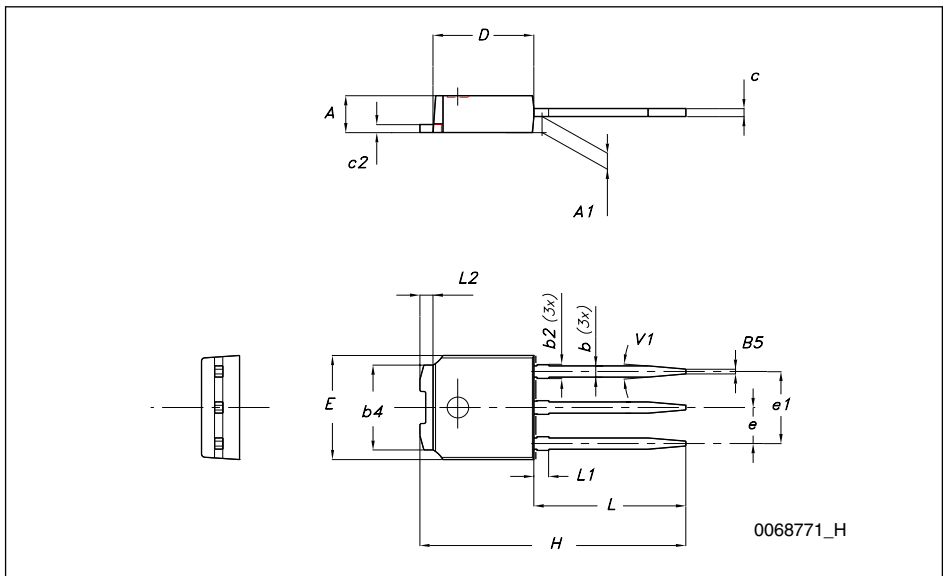
DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°



Obsolete

**TO-251 (IPAK) mechanical data**

DIM.	mm.		
	min.	typ	max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	



Obsole

## 5 Revision history

Table 5. Document revision history

Date	Revision	Changes
24-Jan-2008	1	Initial release

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