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October 2014

# FDMS86322

## N-Channel Shielded Gate PowerTrench® MOSFET
### 80 V, 60 A, 7.65 mΩ

## Features

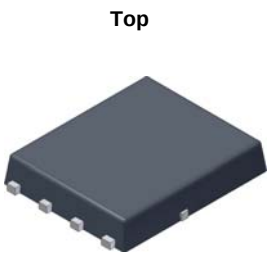
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 7.65 mΩ at $V_{GS}$ = 10 V, $I_D$ = 13 A
- Max $r_{DS(on)}$ = 12 mΩ at $V_{GS}$ = 6 V, $I_D$ = 7.2 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- RoHS Compliant

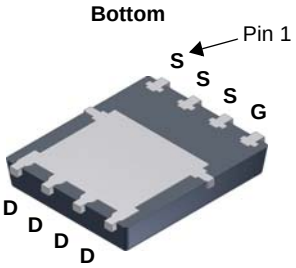
## General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

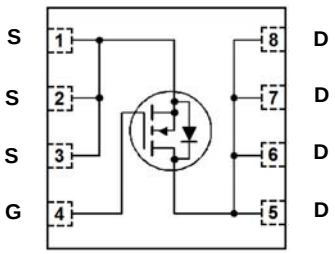
## Application

- DC-DC Conversion




Power 56




## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | | Ratings | Units |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 80 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current -Continuous | $T_C$ = 25 °C | | 60 | A |
| | -Continuous | $T_A$ = 25 °C | (Note 1a) | 13 | |
| | -Pulsed | | | 200 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | | (Note 3) | 135 | mJ |
| $P_D$ | Power Dissipation | $T_C$ = 25 °C | | 104 | W |
| | Power Dissipation | $T_A$ = 25 °C | (Note 1a) | 2.5 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | -55 to +150 | °C |

### Thermal Characteristics

| | | | |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 1.2 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 50 | |

### Package Marking and Ordering Information

| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FDMS86322 | FDMS86322 | Power 56 | 13 ” | 12 mm | 3000 units |

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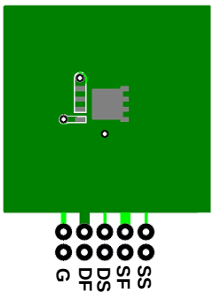
## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

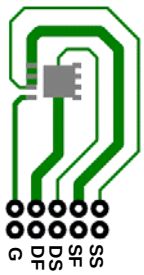
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 80 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 66 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 64 V, $V_{GS}$ = 0 V | | | 800 | nA |
| $I_{GSS}$ | Gate to Source Leakage Current, Forward | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | 100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2.0 | 2.9 | 4.0 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -9 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 13 A | | 6.1 | 7.65 | mΩ |
| | | $V_{GS}$ = 6 V, $I_D$ = 7.2 A | | 8.2 | 12 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 13 A, $T_J$ = 125 °C | | 10.7 | 14 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 13 A | | 45 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | | 2255 | 3000 | pF |
| $C_{oss}$ | Output Capacitance | | | 460 | 610 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 30 | 45 | pF |
| $R_g$ | Gate Resistance | | | 1.0 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 13 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 15 | 27 | ns |
| $t_r$ | Rise Time | | | 11 | 20 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 27 | 44 | ns |
| $t_f$ | Fall Time | | | 7 | 13 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 50 V, $I_D$ = 13 A | | 39 | 55 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 5 V; $V_{DD}$ = 50 V, $I_D$ = 13 A | | 22 | 31 | nC |
| $Q_{gs}$ | Gate to Source Charge | $V_{DD}$ = 50 V, $I_D$ = 13 A | | 9.5 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 50 V, $I_D$ = 13 A | | 10.8 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 2.1 A (Note 2) | | 0.7 | 1.2 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 13 A (Note 2) | | 0.8 | 1.3 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 13 A, di/dt = 100 A/μs | | 56 | 90 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 61 | 98 | nC |

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.




a. 50 °C/W when mounted on a 1 in$^2$ pad of 2 oz copper.




b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25 °C, L = 0.3 mH, $I_{AS}$ = 30 A, $V_{DD}$ = 75 V, $V_{GS}$ = 10 V



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## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

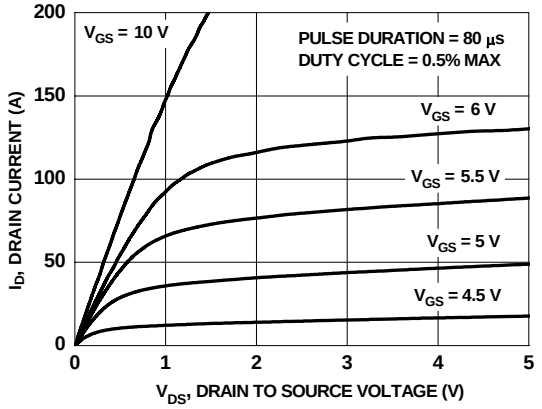


**Figure 1. On Region Characteristics**

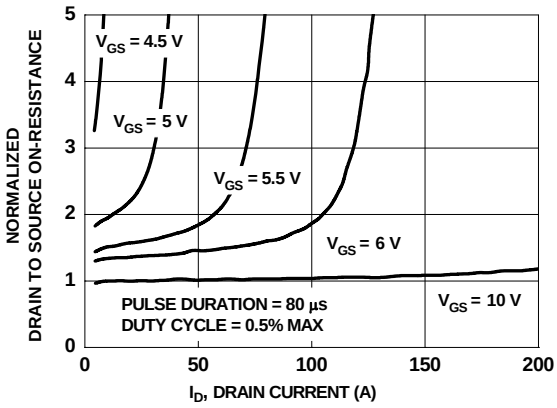


**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

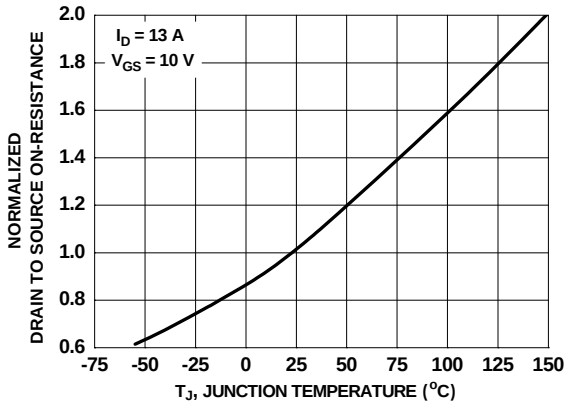


**Figure 3. Normalized On Resistance vs Junction Temperature**

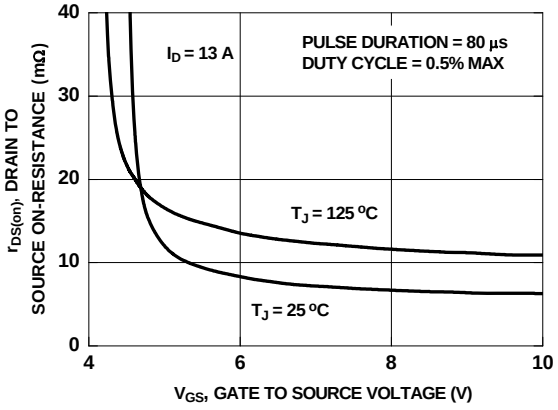


**Figure 4. On-Resistance vs Gate to Source Voltage**

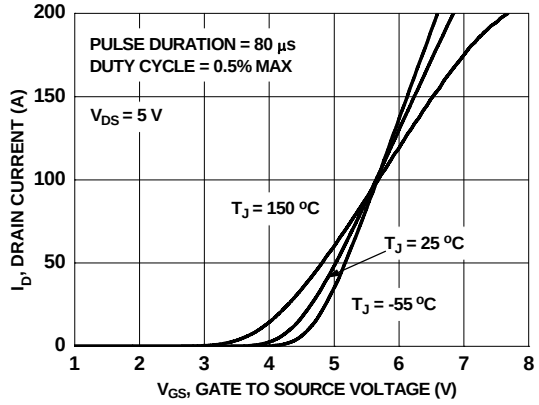


**Figure 5. Transfer Characteristics**

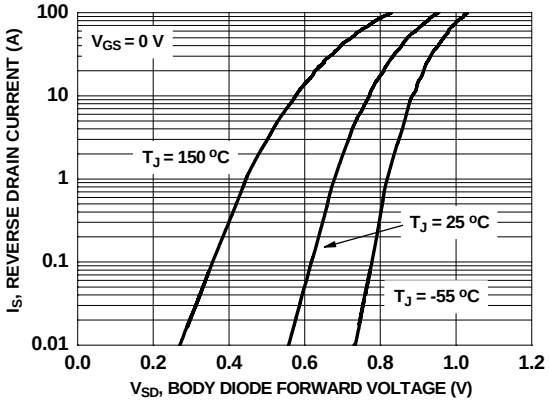


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**



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## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

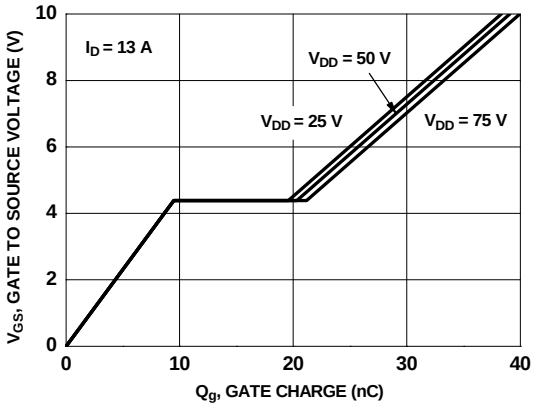


**Figure 7. Gate Charge Characteristics**

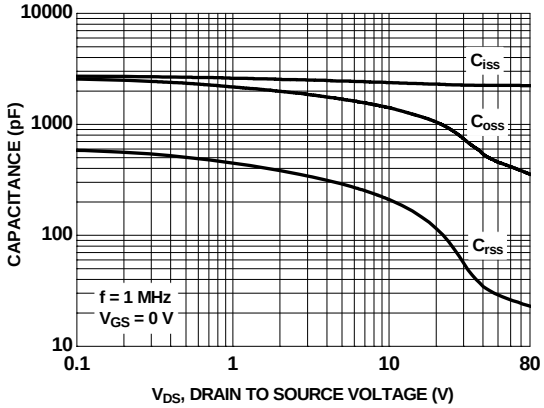


**Figure 8. Capacitance vs Drain to Source Voltage**

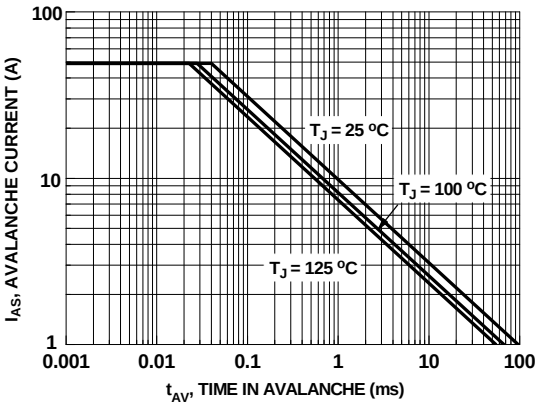


**Figure 9. Unclamped Inductive Switching Capability**

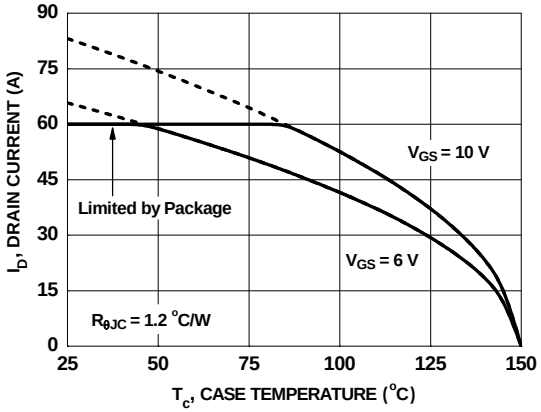


**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

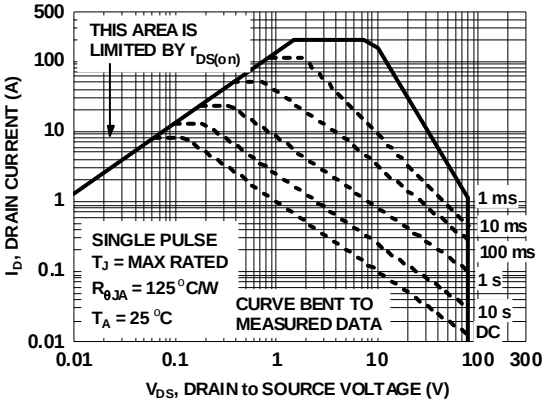


**Figure 11. Forward Bias Safe Operating Area**

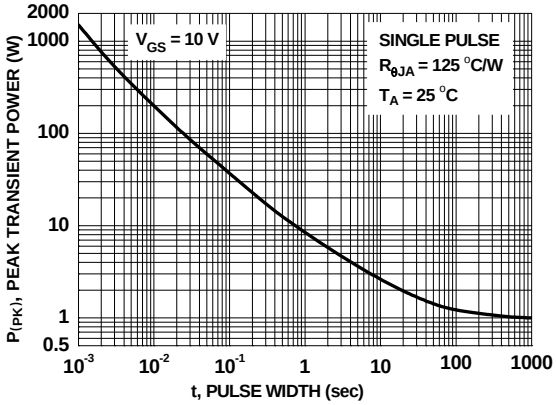


**Figure 12. Single Pulse Maximum Power Dissipation**



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## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

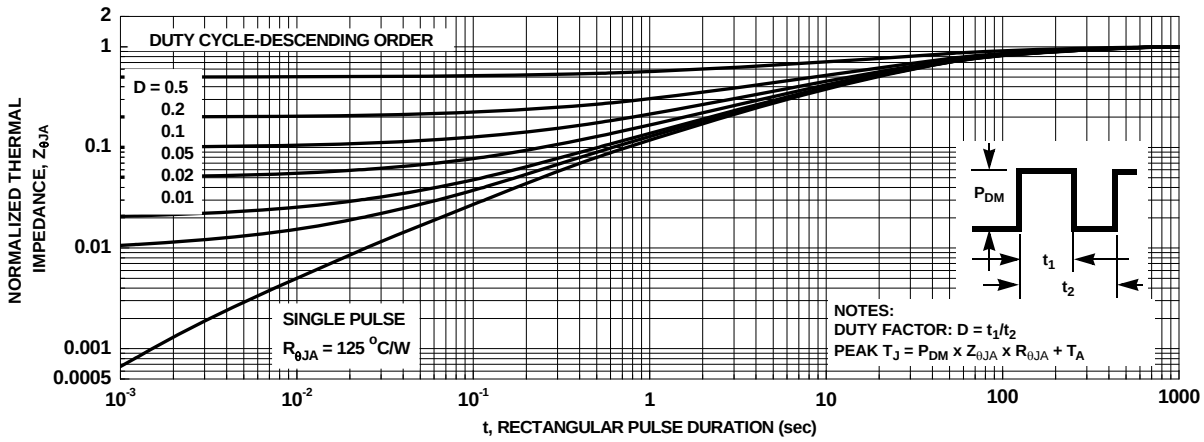


**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



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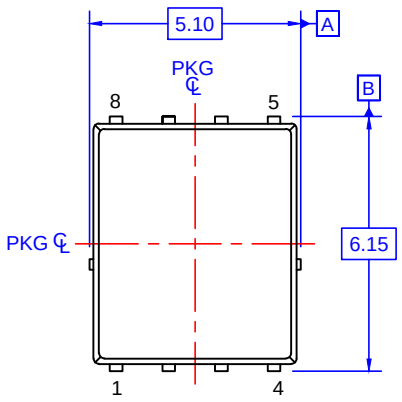
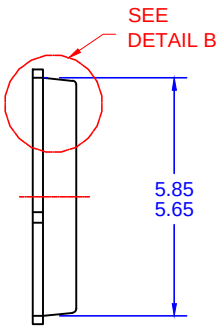
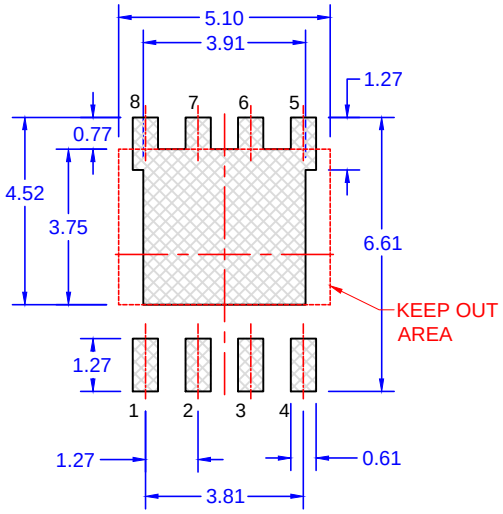
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE A




TOP VIEW




LAND PATTERN
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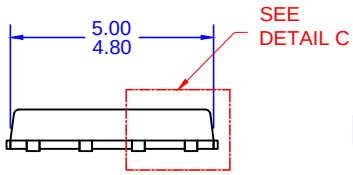
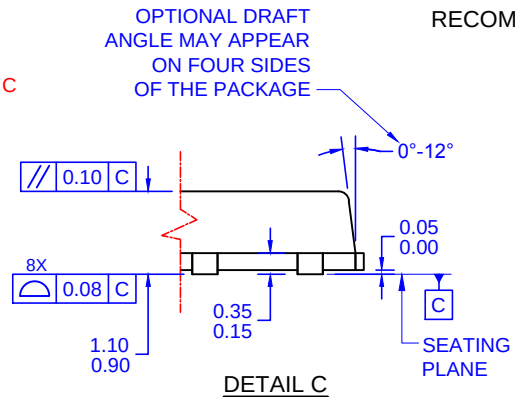



SIDE VIEW




DETAIL C
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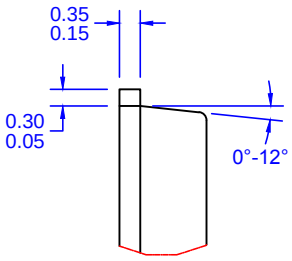


DETAIL B
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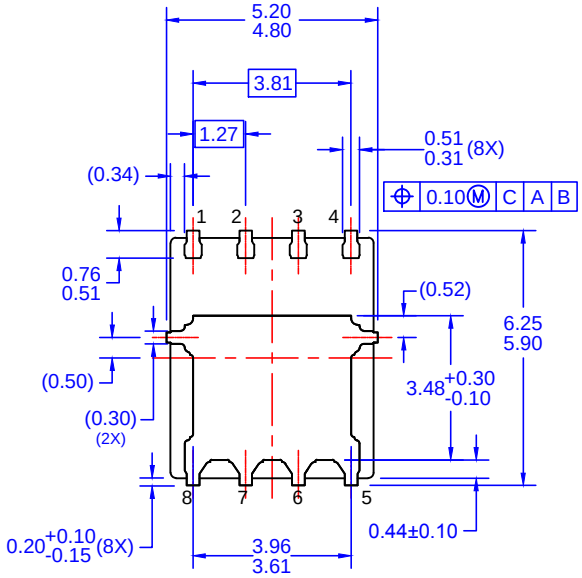


BOTTOM VIEW

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