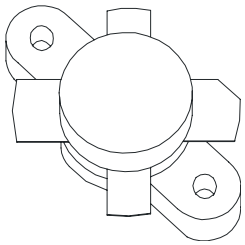
SD2941-10

RF power transistors
HF/VHF/UHF N-channel MOSFETs

General features

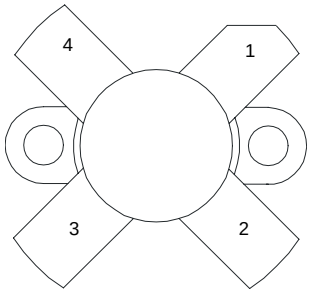
- Gold metallization
- Excellent thermal stability
- Common source configuration
- P_{OUT} = 175W min. with 15dB gain @ 175MHz
- Low $R_{DS(on)}$
- Thermally enhanced packaging for lower junction temperatures



M174 Epoxy sealed

Pin connection

1. Drain
2. Source
3. Gate
4. Source



Description

The SD2941-10 is a gold metallized N-Channel MOS field-effect RF power transistor, intended for use in 50 V dc large signal applications up to 230 MHz. It is offering 25% lower $R_{DS(ON)}$ than industry standard, with 20% higher P_{SAT} than ST SD2931-10.

The SD2941-10 is housed in the low thermal non-pedestal package, offering 25 % lower thermal resistance than industry standard, thus representing the best-in-class transistors for ISM applications, where reliability and ruggedness are critical factors.

Order codes

Part number	Marking	Package	Packaging
SD2941-10	SD2941-10	M174	Plastic tray

Contents

1 Electrical data

1.1 Maximum rating

Table 1. Absolute maximum rating (T_{CASE} = 25°C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$(1)	Drain Source Voltage	130	V
V_{DGR}(1)	Drain-Gate Voltage (R_{GS} = 1MΩ)	130	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current	20	A
P_{DISS}	Power Dissipation	389	W
T_J	Max. Operating Junction Temperature	200	°C
T_{STG}	Storage Temperature	-65 to +150	°C

1. T_J = 150 °C

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Junction to Case thermal resistance	0.45	°C/W

1.3 Electrical characteristics (T_{CASE} = 25°C)

Table 3. Static

Symbol	Test Conditions			Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$ (1)	V_{GS} = 0 V	I_{DS} = 100 mA		130			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 50 V				50	µA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				250	nA
$V_{GS(Q)}$ (2)	V_{DS} = 10 V	I_D = 250 mA			*Table 5.*		V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 10 A				2.0	V
G_{FS}	V_{DS} = 10 V	I_D = 5 A		5	6		mho
C_{ISS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		415		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		236		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		17		pF

1. T_J= 150°C
2. $V_{GS(Q)}$ sorted with alpha/numeric code marked on unit

Table 4. Dynamic

Symbol	Test Conditions				Min.	Typ.	Max.	Unit
P_{OUT}	V_{DD} = 50 V	I_{DQ} = 250 mA		f = 175MHz	175	200		W
G_{PS}	V_{DD} = 50 V	I_{DQ} = 250 mA	P_{OUT} = 175 W	f = 175MHz	14	15.8		dB
h_D	V_{DD} = 50 V	I_{DQ} = 250 mA	P_{OUT} = 175 W	f = 175MHz	55	65		%
Load Mismatch	V_{DD} = 50 V All Phase Angles	I_{DQ} = 250 mA	P_{OUT} = 175W	f = 175MHz	10:1			VSWR

Table 5. V_{GS} Sorts

Symbol	Value	Symbol	Value	Symbol	Value
AA	1.5 - 1.6	E	2.4 - 2.5	P	3.3 - 3.4
BB	1.6 - 1.7	F	2.5 - 2.6	Q	3.4 - 3.5
CC	1.7 - 1.8	G	2.6 - 2.7	R	3.5 - 3.6
DD	1.8 - 1.9	H	2.7 - 2.8	S	3.6 - 3.7
EE	1.9 - 2.0	J	2.8 - 2.9	T	3.7 - 3.8
A	2.0 - 2.1	K	2.9 - 3.0	U	3.8 - 3.9
B	2.1 - 2.2	L	3.0 - 3.1	V	3.9 - 4.0
C	2.2 - 2.3	M	3.1 - 3.2		
D	2.3 - 2.4	N	3.2 - 3.3		

2 Impedance

Figure 1. Impedance data schematic

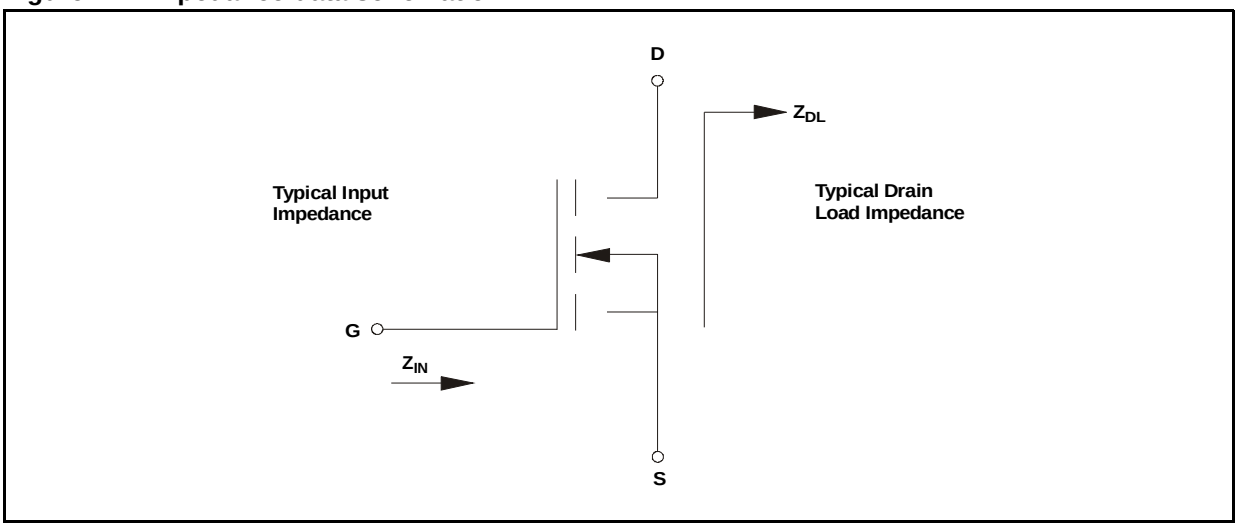


Table 6. Impedance data

f	Z_{IN} (Ω)	Z_{DL} (Ω)
30 MHz	1.7 - j 5.7	6.8 + j 0.9
175 MHz	1.2 - j 2.0	2.0 + j 2.4

3 Typical performance

Figure 2. Capacitance Vs Drain Voltage

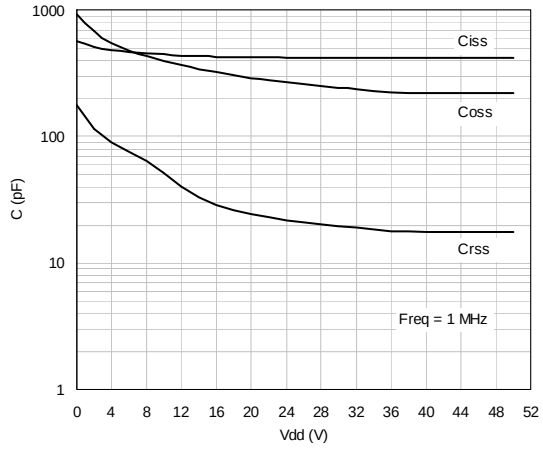


Figure 3. Drain Current Vs Gate Voltage

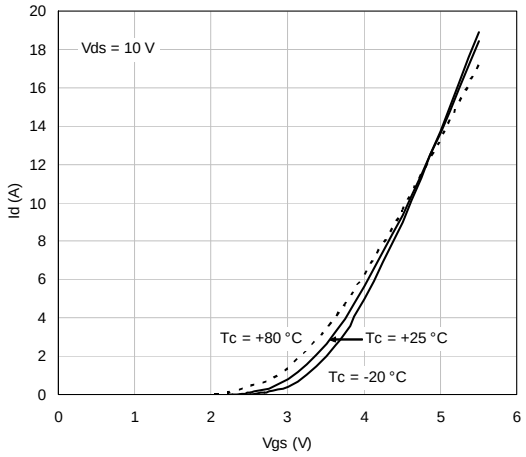


Figure 4. Max. Thermal Resist.Vs Case Temp.

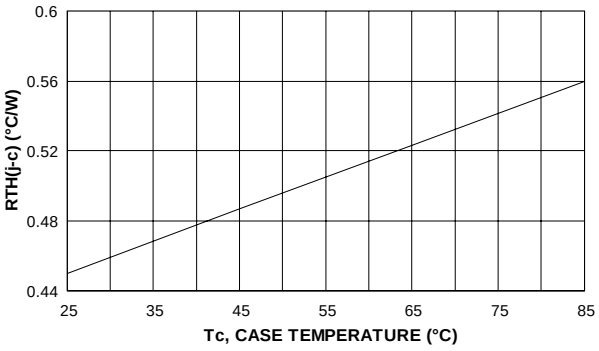
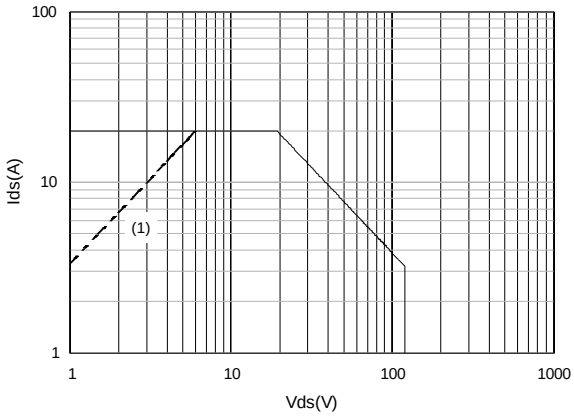


Figure 5. Safe Operating Area



(1) Current in this area may be limited by $R_{ds(on)}$

Figure 6. Power Gain Vs Output Power

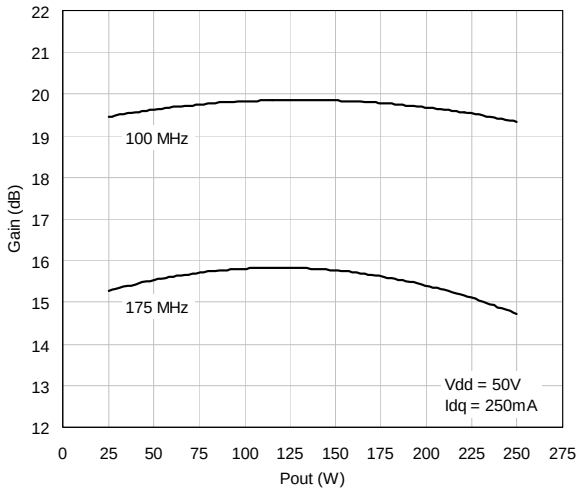


Figure 7. Efficiency Vs Output Power

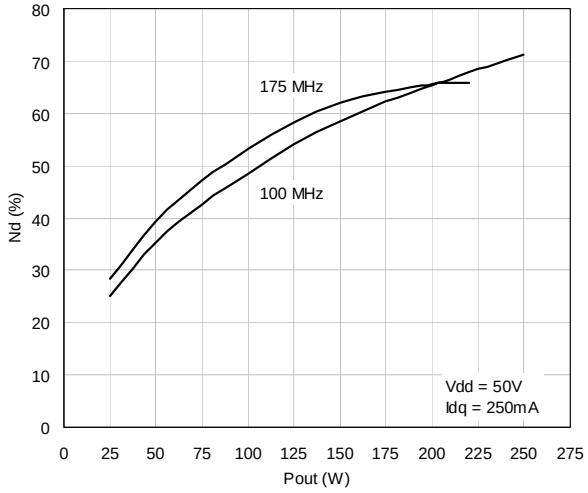
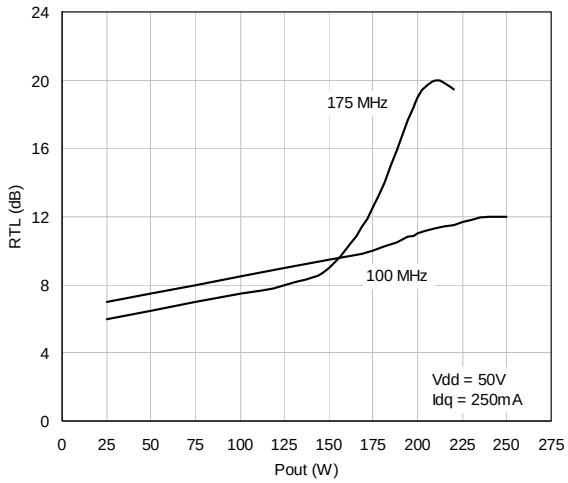
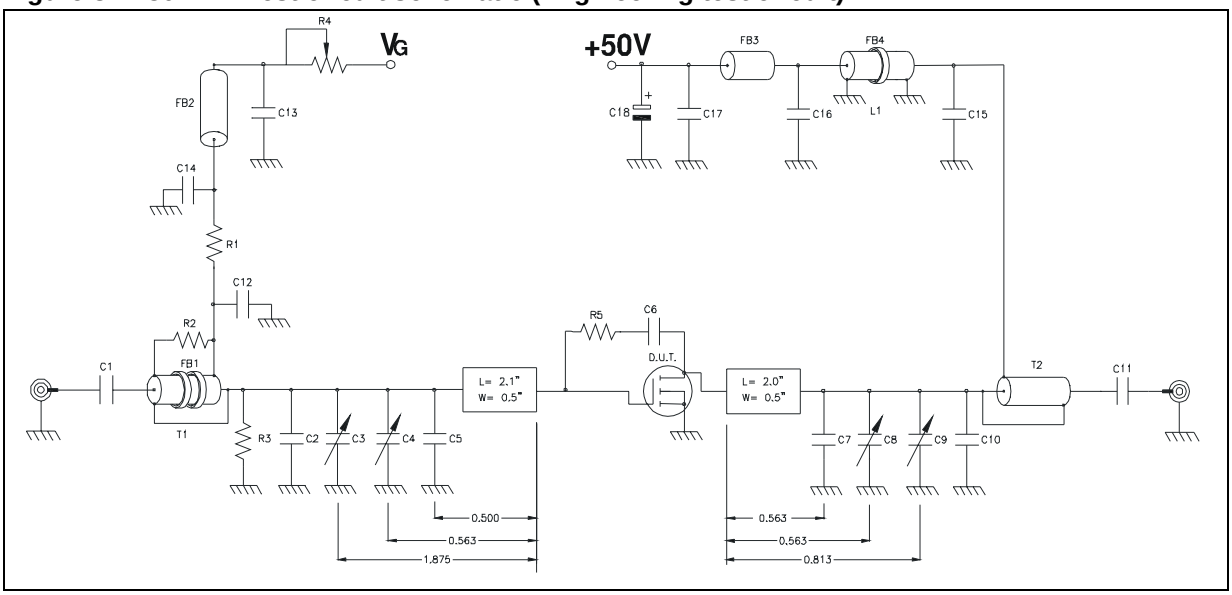


Table 7. Input Return Loss Vs Output Power



4 Test circuit

Figure 8. 30 MHz Test circuit schematic (Engineering test circuit)



Note: All dimension are in inches.

Table 8. 30 MHz test circuit component part list

Simbol	Description
T2	1:4 Transformer, 25Ω Semi-Rigid Coax .141 OD 6” Long
FB1	Toroid X 2, 0.5” OD .312” ID 850µ 2 Turns
FB2, FB3	VK200
FB4	Shield Bead, 1” OD 0.5” ID 850µ 3 Turns
L1	1/4 Wave Choke, 50Ω Semi-Rigid Coax .141 OD 12” Long
PCB	0.62” Woven Fiberglass, 1 oz. Copper, 2 Sides, εr = 2.55
R1, R3	470Ω 1 W Chip Resistor
R2	360Ω 1/2 W Resistor
R4	20 KΩ 10 Turn Potentiometer
R5	560Ω 1 W Resistor
C1, C11	470 pF ATC Chip Cap
C2	43 pF ATC Chip Cap
C3, C8, C9	Arco 404, 12-65 pF
C4	Arco 423, 16-100 pF
C5	120 pF ATC Chip Cap
C6	0.01 µF ATC Chip Cap
C7	30 pF ATC Chip Cap
C10	91 pF ATC Chip Cap
C12, C15	1200 pF ATC Chip Cap
C13, C14,C16, C17	0.01 µF / 500 V Chip Cap
C18	10 µF 63 V Electrolytic Capacitor

Figure 9. 175 MHz test circuit pPhotomaster

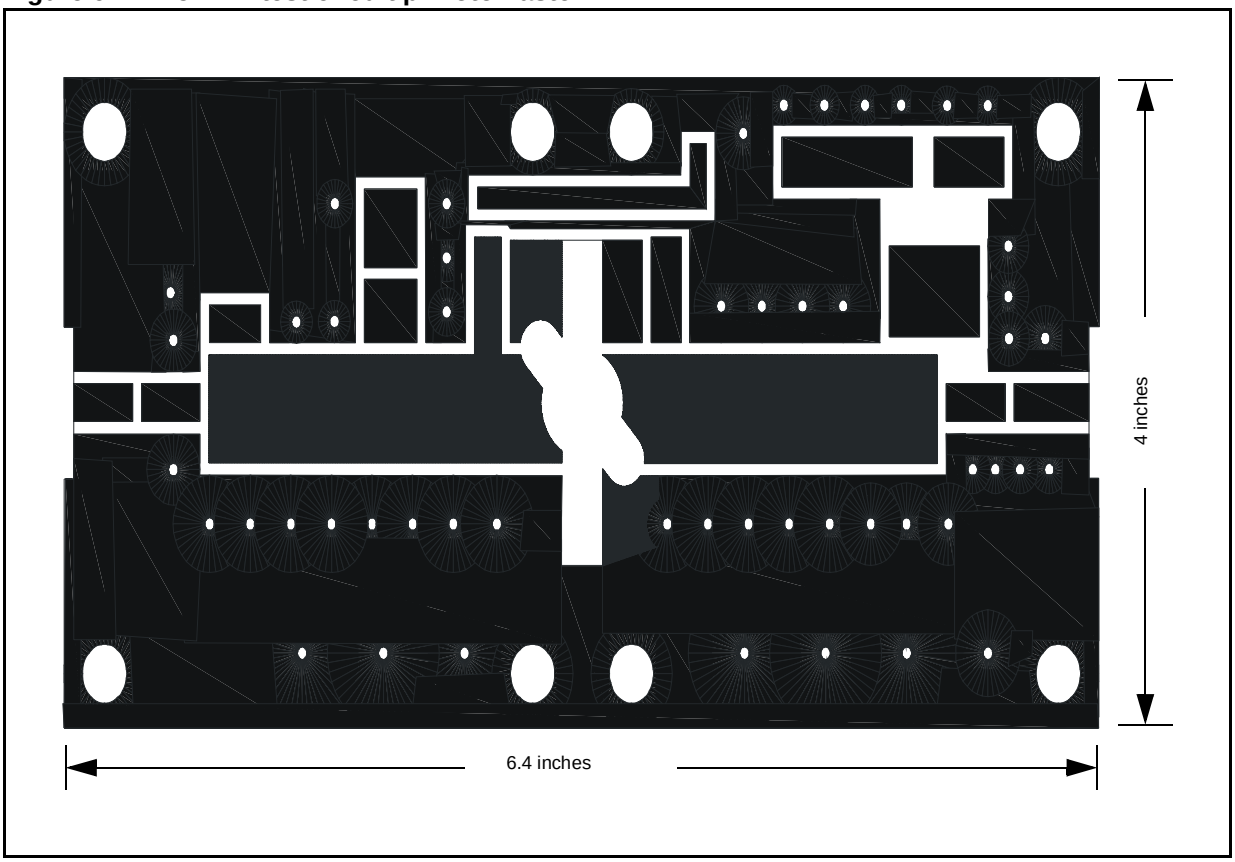
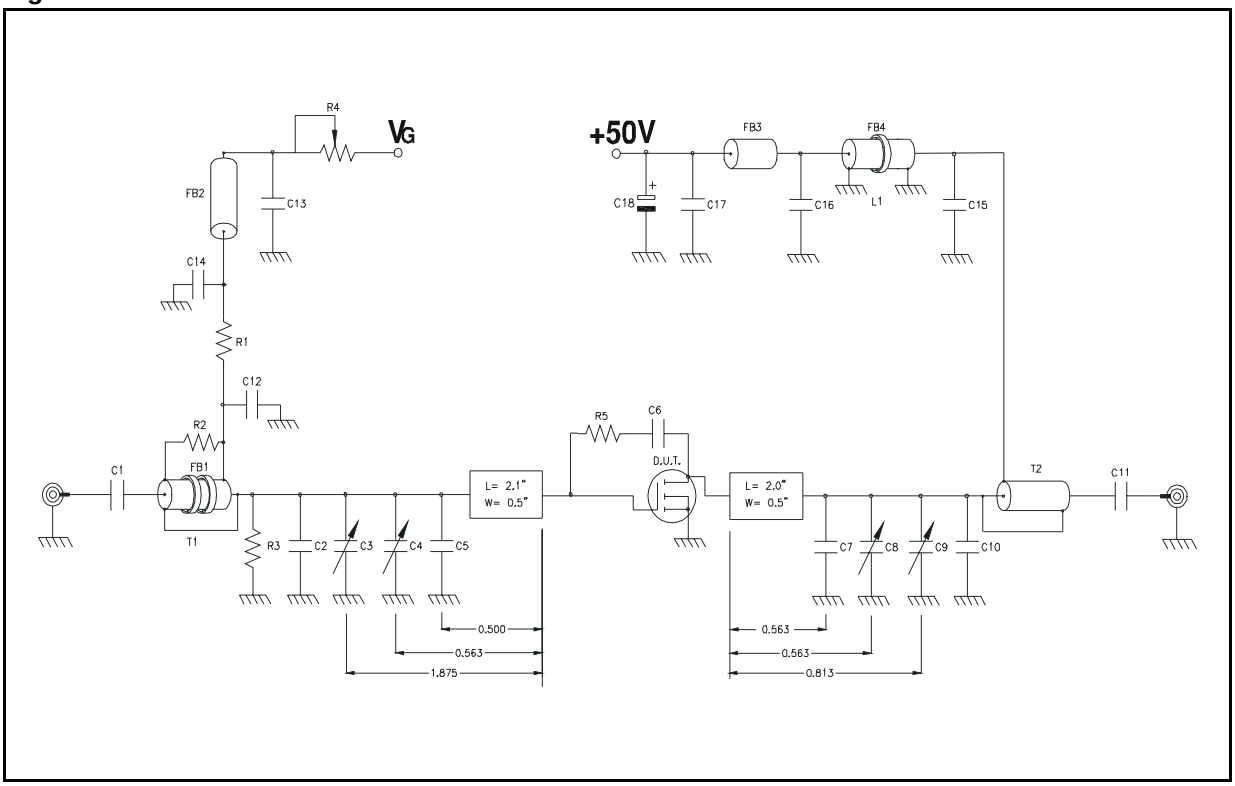


Figure 10. 175 MHz test circuit

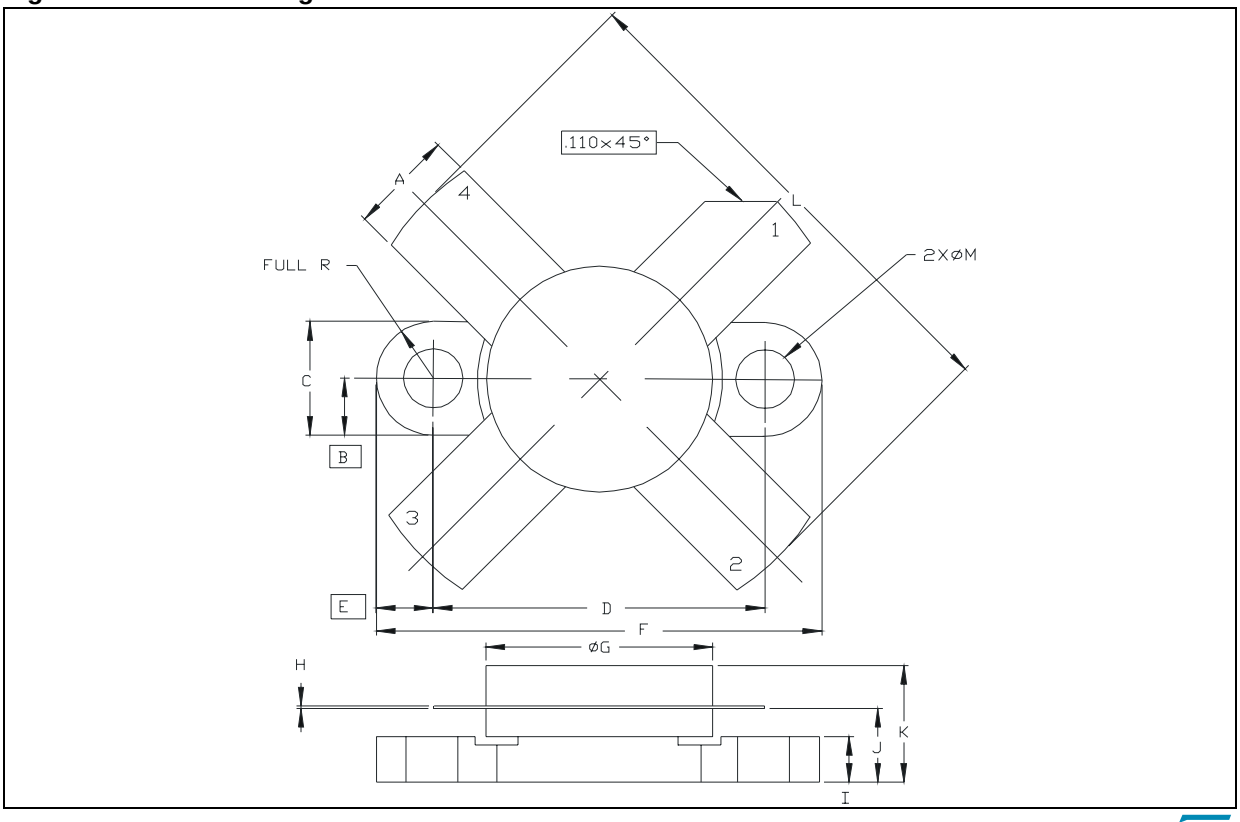


5 Mechanical data

Table 9. M174 (.500 DIA 4/L N/HERM W/FLG)

DIM.	mm.			inch		
	MIN.	TYP.	MAX	MIN.	TYP.	MAX
A						
B	5.56		5.584	0.219		0.230
C		3.18			0.125	
D	6.22		6.48	0.245		0.255
E	18.28		18.54	0.720		0.730
F		3.18			0.125	
G	24.64		24.89	0.970		0.980
H	12.57		12.83	0.495		0.505
I	0.08		0.18	0.003		0.007
J	2.11		3.00	0.083		0.118
K	3.81		4.45	0.150		0.175
L			7.11			0.280
M	25.53		26.67	1.005		1.050

Figure 11. M174 Package dimensions



6 Revision history

Table 10. Revision history

Date	Revision	Changes
15-Nov-2005	1	First Issue
06-Apr-2006	2	Complete version
13-Apr-2006	3	$V_{DS(ON)}$ updated

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