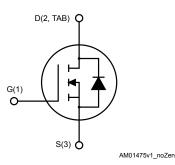




Datasheet

N-channel 200 V, 290 mΩ typ., 7 A, STripFET™ Power MOSFET in a DPAK package





Features

Order code	V _{DS}	R _{DS(on)} max.	۱ _D	
STD7NS20T4	200 V	400 mΩ	7 A	

- Extremely high dv/dt capability
- Very low intrinsic capacitance

Gate charge minimized

Applications

Switching applications

Description

This Power MOSFET series realized with STMicroelectronics unique STripFET[™] process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.



Product status link STD7NS20T4

Product summary		
Order code	STD7NS20T4	
Marking	D7NS20	
Package	DPAK	
Packing	Tape and reel	

1 Electrical ratings

Symbol	Parameter	Value	Unit
V _{DSS}	Drain-source voltage (V_{GS} = 0 V)	200	V
V _{DGR}	Drain-gate voltage (R_{GS} = 20 k Ω)	200	V
V _{GS}	Gate-source voltage	±20	V
1_	Drain current (continuous) at T _C = 25 °C	7	Α
ID	Drain current (continuous) at T _C = 100 °C	4.4	Α
I _{DM} ⁽¹⁾	Drain current (pulsed)	28	Α
P _{TOT}	Total power dissipation at T_C = 25 °C	86	W
E _{AS} ⁽²⁾	Single pulse avalanche energy	110	mJ
dv/dt ⁽³⁾	Drain-body diode dynamic dv/dt ruggedness	5.8	V/ns
T _{stg}	Storage temperature range	-65 to 175	ာိ
TJ	Operating junction temperature range	-00 10 17 0	

Table 1. Absolute maximum ratings

1. Pulse width is limited by safe operating area.

2. Starting $T_J = 25 \ ^{\circ}C, I_D = 4.5 \ A$

3. I_{SD} = 7 A, di/dt = 520 A/µs, V_{DD} = 50 V, $T_J < T_{Jmax}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thj-case}	Thermal resistance junction-case	1.74	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	50	°C/W

1. When mounted on an 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

 T_{CASE} = 25 °C unless otherwise specified

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_{\rm D}$ = 250 μ A, $V_{\rm GS}$ = 0 V	200			V
		V_{DS} = 200 V, V_{GS} = 0 V			1	μA
I _{DSS}	Zero gate voltage drain current	V_{DS} = 200 V, V_{GS} = 0 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate body leakage current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V_{DS} = V_{GS} , I_D = 250 μ A	2	3	4	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 3.5 A		290	400	mΩ

Table 3. On/off states

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance	$V_{1} = 25 V_{1} f = 1 M H_{2}$	-	370	-	pF
C _{oss}	Output capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V		77	-	pF
C _{rss}	Reverse transfer capacitance	VGS - 0 V	-	14	-	pF
Qg	Total gate charge	V _{DD} = 160 V, I _D = 7 A	-	11.6	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 0 to 10 V	-	2.2	-	nC
Q _{gd}	Gate-drain charge	(see Figure 13. Test circuit for gate charge behavior)	-	5.4	-	nC

Table 5. Switching times

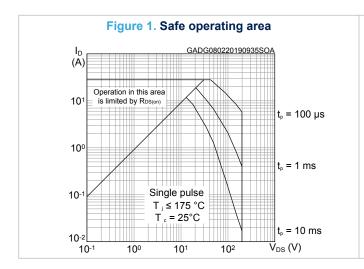
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 100 V, I _D = 4.5 A,	-	5.6	-	ns
		R_G = 4.7 Ω , V_{GS} = 10 V				
tr	Rise time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	2.6	-	ns

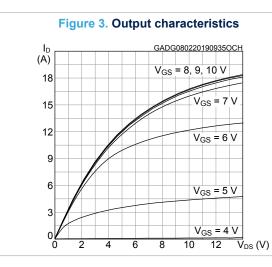
Table 6. Source-drain diode

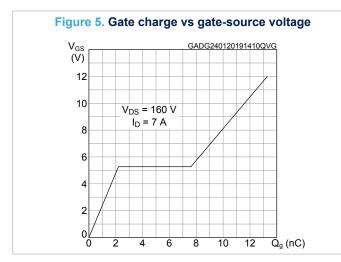
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{SD} ⁽¹⁾	Forward on voltage	I_{SD} = 7 A, V_{GS} = 0 V	-		1.5	V
t _{rr}	Reverse recovery time	I _{SD} = 7 A, di/dt = 100 A/μs,	-	118.5		ns
Q _{rr}	Reverse recovery charge	$V_{DD} = 50 V$	-	393		nC
I _{RRM}	Reverse recovery current	(see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	6.6		A

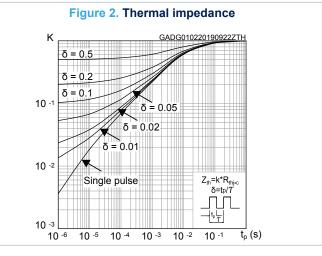
1. Pulsed: pulse duration = $300 \ \mu$ s, duty cycle 1.5%

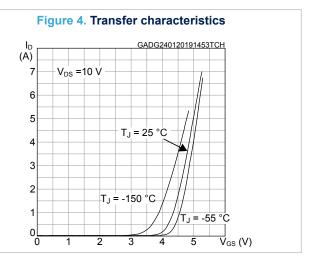
2.1 Electrical characteristics (curves)

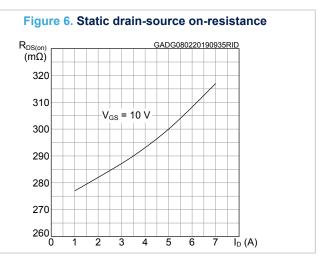




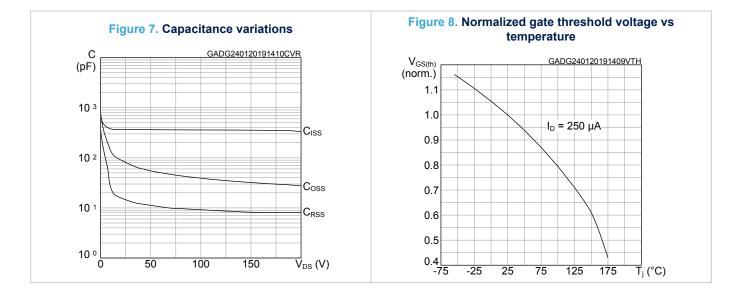












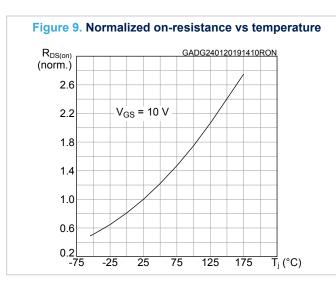
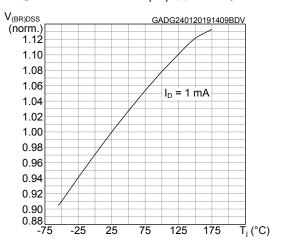
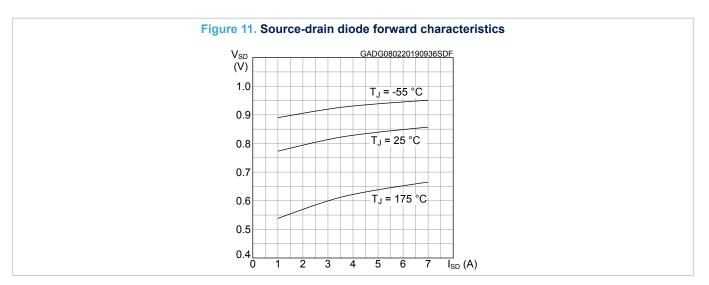


Figure 10. Normalized V_{(BR)DSS} vs temperature

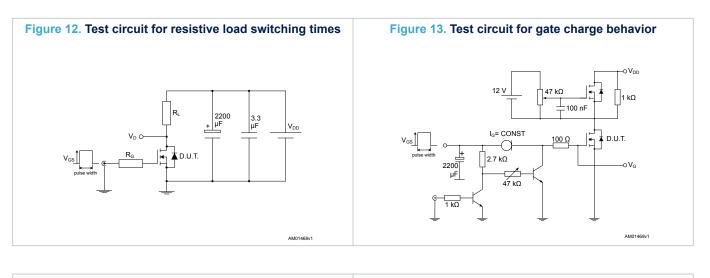


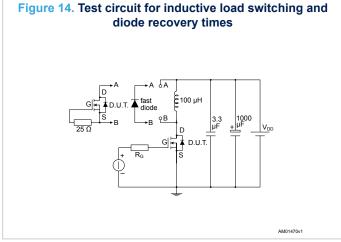


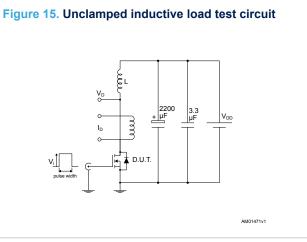
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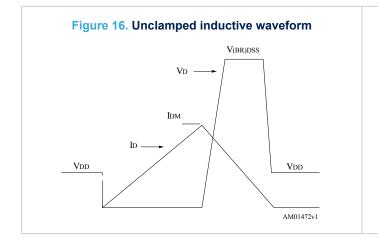


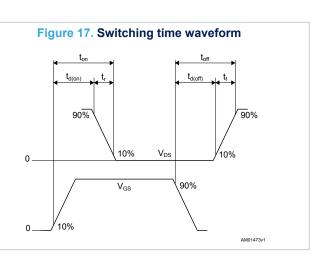
3 Test circuits











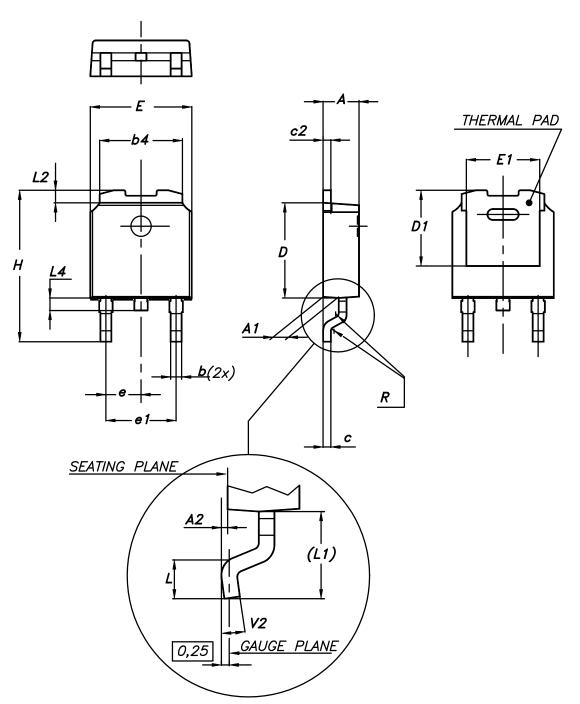
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 DPAK (TO-252) type A package information

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Figure 18. DPAK (TO-252) type A package outline



0068772_A_26

Dim.		mm	
Dim.	Min.	Тур.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00	0 6.20	
D1	4.95	4.95 5.10	
E	6.40		6.60
E1	4.60	4.70	4.80
е	2.159	2.286	2.413
e1	4.445	4.572	4.699
Н	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Table 7. DPAK (TO-252) type A mechanical data

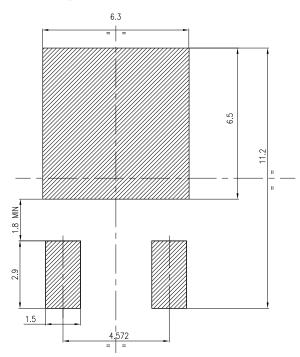
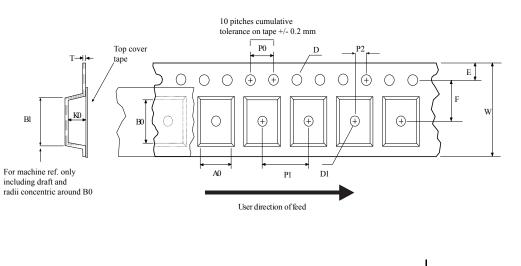


Figure 19. DPAK (TO-252) type A recommended footprint (dimensions are in mm)

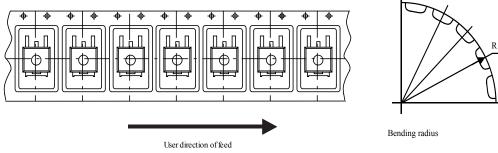
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4.2 DPAK (TO-252) packing information

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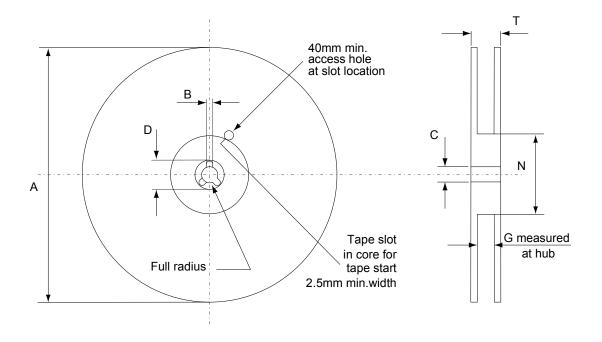




AM08852v1







AM06038v1

	Таре			Reel	
Dim.	n	mm			mm
Dim.	Min.	Max.	Dim.	Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base	e qty.	2500
P1	7.9	8.1	Bull	k qty.	2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

Table 8. DPAK (TO-252) tape and reel mechanical data

Revision history

Table 9. Document revision history

Date	Version	Changes
11-Feb-2019	1	First release.

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Rev	Revision history		



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